PM6344

EQUAD

ANSWERS TO FREQUENTLY ASKED QUESTIONS REGARDING THE EQUAD

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CONTENTS

REFERENCES

- ETSI, ETS 300 011 (April 1992), “ISDN; Primary Rate User-Network Interface Layer 1 Specification and Test Principles”
- ETSI, ETS 300 011 Amendment 1 (December 1994), “ISDN; Primary Rate User-Network Interface Layer 1 Specification and Test Principles”
- ITU-T Recommendation G.704, Blue Book Vol. III, Fascicle III.4 (November 1988), “Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels”
- ITU-T Recommendation G.706, Blue Book Vol. III, Fascicle III.4 (November 1988), “Frame Alignment and CRC Procedures Relating to Basic Frame Structures Defined in Recommendation G.704”
- ITU-T Recommendation I.431 (03/93), "Primary Rate User-Network Interface — Layer 1 Specification"
- PMC-Sierra, PMC-951013P2, Issue 2, Data Book for PM6344 EQUAD Quadruple E1 Framer.

DEFINITIONS AND TERM GLOSSARY

AIS — Alarm Indication Signal. This is a signal consisting of unframed all-ones serial digital data. It is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. This signal can be detected and transmitted by the EQUAD.

AMI — Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse which is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).

CDRC — Clock and Data Recovery unit. This is PMC-Sierra's mnemonic to refer to the functional block in the EQUAD which recovers the timing of the received signal, then uses that timing to sample the received data.

CRC — Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload.

DJAT — Digital Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the EQUAD which attenuates phase jitter on the transmit timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.

E1 — European transmission format level 1. This term is used to describe systems signals conforming to the ITU-T 2048 kbit/s format and interface specifications.

ELST — Elastic Store. This is PMC-Sierra's mnemonic for the functional block within the EQUAD which provides the elastic store function. The ELST is used for adapting the received data to the system backplane rate. Since these signals are not necessarily synchronized, they may slip with respect to each other. The function of the ELST is to control the slips such that they occur on the frame boundaries indicated on the backplane. For example, if the received data is faster than the system backplane then the ELST will drop full frames of data while maintaining the timeslot alignment on the backplane.

EQUAD — Quadruple E1 Framer. This is PMC-Sierra's mnemonic for the PM6344 EQUAD device.

FIFO — First-In First-Out buffer. This term refers to a digital buffer which outputs data in the same order as it was input.

HDB3 — High-Density Bipolar of order 3. This is a zero suppression scheme which uses the intentional insertion of AMI LCVs to maintain a minimum transition density in the E1 signal. This function is important since it provides clear channel capability — the payload content is not restricted by the capabilities of the remote receiver's clock recovery unit.

ISDN — Integrated Services Digital Network. This is a world-wide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.

ITU-T — International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is “to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony.” Its primary objective is end-to-end compatibility of international telecommunications connections.

LCV — Line Code Violation. This term denotes a received bipolar pulse which violates the AMI or HDB3 ternary coding scheme. LCV events are detected and accumulated by the EQUAD.

LIU — Line Interface Unit. A device or circuit which implements the electrical requirements for a telecommunications transmission interface.

LOS — Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since E1 uses a zero code suppression scheme (HDB3), the EQUAD monitors for LOS by monitoring the number of consecutive spaces (zeros) received.

NRZ — Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data which has an associated clock signal.

OOF — Out-Of-Frame alignment. This is the state an E1 framer is in if it cannot find the frame alignment pattern within the received serial 2048kbit/s data.

PCM — Pulse-Coded Modulation. Digital serial data representing analog signals on telephone subscriber loops.

PLL — Phase-Locked Loop. The generic term for a feed-back system which generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.

RZ — Return-to-Zero. This refers to an electrical coding scheme for serial digital data. Logical ones are represented as a pulse which is high for half the bit period then returns to low (zero) for the remainder of the bit period. Logical zeros are represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.

SIGX — Signaling Extractor. This is PMC-Sierra's mnemonic for the functional block of the EQUAD which extracts and stores the received robbed-bit (channel-associated) signaling information. It also provides some per-channel functions on the received PCM data and signaling data, before passing to the receive backplane.

TPSC — Transmit Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the EQUAD which allows per-channel functions to be performed on the PCM and signaling data from the transmit backplane, before transmission.

TRAN — Transmitter. This is PMC-Sierra's mnemonic for the functional block of the EQUAD which inserts the E1 framing overhead into Timeslots 0 and 16 of the E1 frame. The TRAN can be configured to transparently pass either Timeslot 0 or 16 (or both) from the transmit backplane.

BACKGROUND AND OVERVIEW

PMC-Sierra's PM6344 Quadruple E1 Framer is a full-featured device for 2048 kbit/s digital telecommunications links.

Due to the versatility of the EQUAD, the data book for that device is quite lengthy. In order to help customers quickly find the answers to their questions, the following list of answers to frequently asked questions has been compiled.

FREQUENTLY ASKED QUESTIONS

Q1) How should the EQUAD be initialized by software?

A1) The EQUAD will be in a known default state after hardware or software reset. However, additional configuration is usually required.

Table 1 shows the recommended register initialization for ISDN primary rate applications. Registers which are not included in Table 1 should be left in their default state.

For applications other than ISDN primary rate, the following information should be considered when initializing the EQUAD.

There are four major modes of the EQUAD corresponding to the two E1 framing format alternatives (basic and CRC-4) and the two signaling format alternatives (CAS and CCS). These four modes are standardized in ITU-T G.704.

The EQUAD is designed such that the transmit and receive functions are independent, so both directions need to be configured for each desired feature.

To control whether basic framing or CRC-4 multiframing is processed, there are the CRCEN bits in Register 020H, 0A0H, 120H, 1A0H and the GENCRC bits in Register 044H, 0C4H, 144H, 1C4H.

To control whether CAS or CCS is processed, there are the CASDIS bits in Register 20H, 0A0H, 120H, 1A0H and the SIGEN and DLEN bits in Register 44H, 0C4H, 144H, 1C4H. The appropriate settings for these bits is explained in the register descriptions in the EQUAD data book.

In addition to setting up the framing format, there is some additional initialization which should be done: setting the timing options, initializing the per-channel serial controllers (the TPSC, and SIGX functional blocks), and selecting internal versus external HDLC processing.

The timing options are configured using the Timing Options register (07H, 87H, 107H, and 187H) in the EQUAD. The appropriate timing option depends on the hardware connections used. The description of Timing Options register in the EQUAD data book explains which timing option is suited to particular hardware implementations.

Table 1. Recommended Register Initialization for ISDN PRI

Register Address (hex)	Recommended Configuration for ISDN Primary Rate Interfaces	
000, 080, 100, 180	TRKEN=1	This allows EQUAD to automatically propagate an AIS to the receive backplane while in an OOF condition.
006, 082, 102, 182	TXSA4EN=0	This disables the insertion of a datalink into the National Use bits of TS0.
007, 087, 107, 187	PLLREF1=1	This chooses the possible transmit timing reference to be either RCLKO[x] or TCLKI[x].
	PLLREF0=X	This bit should be set according to the desired transmit timing mode. (See Transmit Timing Options in the EQUAD databook)
009, 089, 109, 189	RXSA4EN=0	This allows TS16 to be extracted for D-Channel processing.
010, 090, 110, 190	ALGSEL=1	This chooses a clock and data recovery algorithm with best tolerance of high frequency jitter.
020, 0A0, 120, 1A0	CRCEN=1	This enables the MFAS alignment circuitry in the FRMR.
	CASDIS=1	This disables the CAS multiframe alignment circuitry in the FRMR.
021, 0A1, 121, 1A1	BIT2C=1	This enables the EQUAD to declare OOF if Bit 2 of TS0 of NFAS frames is received incorrectly for three consecutive times.
022, 0A2, 122, 1A2	OOFE=1	This enables changes in the status of the FAS alignment circuit to generate interrupt indications on the EQUAD's INTB output pin.
	OOCMFE=1	This enables changes in the status of the MFAS alignment circuit to generate interrupt indications on the EQUAD's INTB output pin.
023, 0A3, 123, 1A3	RRAE=1	This enables changes in the status of the RAI detection circuit to generate interrupt indications on the EQUAD's INTB output pin.
	AISDE=1	This enables changes in the status of the AIS fast detection circuit to generate interrupt indications on the EQUAD's INTB output pin.
030, 0B0, 130, 1B0	IND=1	This enables indirect accessing of the Transmit Per-Channel Serial Controller (TPSC) registers within the EQUAD. The indirect registers within the TPSC should be initialized as explained below.
044, 0C4, 144, 1C4	SIGEN=0	This disables the transmission of Channel-Associated Signaling in TS16.

The per-channel serial controllers use internal indirect registers for controlling the per-channel functions. These internal indirect registers do not come up in a known default state — they must be initialized if the per-channel serial controllers are enabled. The method of programming and initializing the per-channel serial controller indirect registers is explained in the section entitled "Using the Per-Channel Serial Controllers" in the EQUAD data book. The values to which these indirect registers should be initialized depends on the application.

The EQUAD provides the ability (with the RFDL and XFDL functional blocks) to process the HDLC (LAPD) information carried on the CCS or ISDN primary rate D-Channel (carried in Timeslot 16 of the E1 frame). It can be extracted to the RDLSIG[x] and inserted from the TDLSIG[x] pins. When the RFDL and XFDL are enabled, the HDLC payload and status information is available via registers. This information can either be accessed via the host microprocessor, or an external DMA controller can be dedicated to this task. To facilitate the use of an external DMA controller, the RDLSIG[x], RDLCLK[x], TDLSIG[x] and TDLCLK[x] pins can be configured to operate as interrupt signals RDLINT[x], RDLEOM[x], TDLINT[x] and TDLUDR[x] respectively. All of these options for HDLC processing are controlled in Register 002H, 082H, 102H, 182H. The XFDL and RFDL, are enabled with the EN bits in Registers 034H, 0B4H, 134H, 1B4H, and 038H, 0B8H, 138H, 1B8H respectively.

The EQUAD can be operated in a Fractional E1 mode where some subset of timeslots are extracted on the RDLSIG[x] and RDLCLK[x] pins and inserted with the TDLSIG[x] and TDLCLK[x] pins. The Fractional E1 channel is defined with the Channel Select Registers (014H, 015H, 016H, 017H, 094H, 095H, 096H, 097H, 114H, 115H, 116H, 117H, 194H, 195H, 196H, and 197H). The Fractional E1 channel is symmetric in both transmit and receive directions. The Fractional E1 mode is enabled when the RFRACE1 and TFRACE1 bits in the Datalink Options Register (002H, 082H, 102H, and 182H) are set to logic one.

Q2) How can the EQUAD be configured to operate its receiver in un-framed (transparent) mode?

A2) Receiving un-framed mode implies that the framer does not "care" if a framing pattern is present in the incoming data. Therefore, the frame alignment is unknown.

To receive un-framed data on the EQUAD, the TRKEN bit in Register 000H, 080H, 100H, 180H and the MTKC bit in Register 040H, 0C0H, 140H, 1C0H should both be cleared to a logic zero. This disables the ELST from overwriting the trouble code (contained in Register 01EH, 09EH, 11EH, 19EH) or trunk conditioning on the backplane receive data.

The SIGX per-channel functions should also be disabled by clearing the PCCE bit in Register 040H, 0C0H, 140H, 1C0H to logic zero.

Additionally, the REFRDIS bit in Register 020H, 0A0H, 120H, 1A0H should be set to logic one to disable the FRMR from searching for frame alignment. During the reception of un-framed data, the FRMR status and interrupt status information should be ignored although AIS can still be detected by the FRMR, as indicated by the AISI and AIS bits in Registers 025H, 0A5H, 125H, 1A5H and 027H, 0A7H, 127H, 1A7H respectively.

The CDRC functional block continues to operate in un-framed mode, so LOS and LCVs can still be detected.

Q3) How can the EQUAD be configured to operate its transmitter in un-framed (transparent) mode?

A3) Transmitting un-framed mode implies that the EQUAD does not overwrite any of the data from the transmit backplane (applies to the BTPCM input). Therefore, no framing overhead should be written, no signaling inserted, no AIS generated, no per-channel functions, and no National Use bits inserted.

To transmit un-framed data on the EQUAD:

- The framing overhead insertion by the TRAN functional block in Timeslot 0 should be disabled by setting the FDIS bit in Register 44H, 0C4H, 144H, 1C4H to logic one
- The signaling (CAS and CCS) should be disabled by clearing both the SIGEN and DLEN bits in Register 044H, 0C4H, 144H, 1C4H
- AIS generation should be disabled by clearing the AIS bit in Register 045H, 0C5H, 145H, 1C5H, and the TAISEN bit in Register 004H, 084H, 104H, 184H to logic 0
- The TPSC functional block should be disabled by clearing the PCCE bit in Register 030H, 0B0H, 130H, 1B0H to logic zero

- The National Use bits inserted from the TDLSIG[x] pin should be disabled by clearing the TSAxEN (x = 4 to 8) bits in Transmit Framing Options register(006H, 086H, 106H, 186H)

Note that it is allowable to enable HDB3 encoding (by clearing the AMI bit in Register 044H, 0C4H, 144H, 1C4H to logic zero) when transmitting un-framed data.

Q4) What is the difference between using a 49.152MHz and a 16.384MHz clock to drive the XCLK input of the EQUAD?

A4) Although the EQUAD allows the use of either a 49.152MHz or a 16.384MHz clock as the XCLK input, the 49.152MHz XCLK is recommended for most designs, especially those requiring jitter attenuation.

The DJAT functional block of the EQUAD requires a 49.152MHz oscillator to operate. Therefore, the 49.152MHz XCLK is necessary if jitter attenuation is desired; otherwise the 16.384MHz XCLK is acceptable.

PMC Sierra's PM4314 QDSX quadruple T1/E1 LIU usually operates with the 49.152MHz XCLK. Thus, in designs using both QDSX and EQUAD it is easiest to use a common XCLK.

Q5) What is the required frequency tolerance of the XCLK input?

A5) The XCLK frequency should be within ±50ppm of nominal frequency.

There are two digital phase-locked loops within the EQUAD (one in DJAT and one in CDRC). The XCLK input is used as the high-speed clock for both PLLs, and therefore sets the free-running frequency of these PLLs.

The frequency capture and lock ranges of a PLL is a function of the free-running frequency. Therefore, to ensure that the specified capture and lock ranges of the PLLs are met, it is important to use an XCLK input with a better than ±50ppm frequency tolerance. Oscillator manufacturers can provide ±50ppm and ±25ppm oscillators which are suitable.

Note that the frequency tolerance of the transmitted line rate will depend on the frequency tolerance of the transmit frequency reference (e.g. the BTCLK[x] or TCLKI[x] input), *not* the XCLK input.

Q6) What are some recommended oscillator manufacturers?

A6) Any reputable crystal oscillator manufacturer should be able to provide the 49.152MHz or 16.384MHz oscillator to source the EQUAD's XCLK input signal. Since this is a non-standard frequency, they will generally have to be custom cut. The 1100 series of custom-cut crystal oscillators is suitable and available from most manufacturers. The oscillator should output TTL (or TTL-compatible) levels.

Some manufacturers which PMC-Sierra has used in-house with the EQUAD are: Champion Technologies, Connor-Winfeld, Ecliptek Corporation, and Fox Corporation. These should be available from most electronics components distributors.

Custom cut oscillators can have very long lead times (16 weeks typical) so they should be ordered well in advance of when they will be needed.

Q7) Are there any application notes or reference designs for the EQUAD?

A7) Yes. There is a document (PMC-960911) available which describes, including schematics, the EQUAD used in conjunction with PMC-Sierra's PM4314 QDSX quadruple T1/E1 LIU device.

Additionally, an E1XC application note (PMC-951128) is available which explains the functional considerations necessary for ensuring that an E1XC design is compatible with ETS 300 011 ISDN primary rate Layer 1 requirements. Some information in this application note applies to the EQUAD. Engineers designing with the EQUAD should review this application note.

PMC-Sierra Sales Representatives have copies of these documents available for distribution. It is suggested that customers periodically query their PMC-Sierra Sales Representative for the latest application notes for the EQUAD. Also, most documents can be downloaded from PMC-Sierra's Web site (http://www.pmc-sierra.com).

Q8 What is the relationship between the BRFPI input and the BRFPO[x] output of the EQUAD?

A8 The BRFPI input is only used when the ELST functional block is active (ELSTBYP=0 in Register 000H, 080H, 100H, 180H).

With the ELST enabled, BRFPO[x] is generated as a divide-by-256 of BRCLK. Provided that there is an active BRCLK input, BRFPO[x] will always be generated.

The counter generating BRFPO[x] from BRCLK is synchronously reset by the BRFPI input such that the BRFPI and BRFPO[x] signals are aligned.

BRFPO[x] can be configured as a multiframe pulse (controlled by the BRXCMFP bit in Register 001H, 081H, 101H, 181H). When BRFPO[x] is configured as a multiframe pulse, then another counter is activated which further divides the regular frame pulse by 16 to indicate the multiframe boundaries. In that case, the multiframe boundaries of the BRPCM[x] and BRSIG[x] data will be aligned to BRFPO[x]

The counter generating the multiframe pulse is *not* reset by the BRFPI input. This means that a multiframe pulse applied to BRFPI will not necessarily be aligned with a multiframe pulse output on BRFPO[x], although there will be an integral number of frames separating them.

When the EQUAD is in frame alignment, the first bit of Timeslot 0 in the BRPCM[x] and BRSIG[x] output signals will always be aligned to the BRFPO[x] pulse. It is recommended that BRFPO[x], rather than BRFPI, should be used to indicate the backplane frame alignment to external circuitry, although BRFPI is often allowable.

Q9) Can BRFPO[x] be connected to BRFPI on the EQUAD?

A9) Yes, there is no problem with feeding back BRFPO[x] as the BRFPI for the same ELST. The BRFPI resets the counter generating BRFPO[x] such that no clocking loop will occur.

With BRFPO[x] connected to BRFPI, the BRFPO[x] counter will chose some arbitrary point to assert the BRFPO[x] signal after a reset (software or hardware) of the EQUAD. From then on, the feedback to the BRFPI input will keep the BRFPO[x] at that same position with respect to BRCLK.

Q10) Does the EQUAD require a BRFPI signal to generate BRFPO[x]?

A10) No. It is valid to tie BRFPI low (to digital ground) and allow BRFPO[x] to free-run as a divide-down of the BRCLK input.

In this case, the BRFPO[x] counter will chose some arbitrary point to assert the BRFPO[x] signal after a reset (software or hardware) of the EQUAD. From then on, the BRFPO[x] will continue to be generated every time the counter "rolls over" thus maintaining that alignment with respect to BRCLK.

Q11) If the ELST is bypassed, how is the BRFPO[x] output signal generated?

A11) The ELST can be bypassed by setting the ELSTBYP Bit in Register 000H, 080H, 100H, 180H to a logic one.

When the ELST is bypassed, the BRFPO[x], BRPCM[x], and BRSIG[x] output signals will be updated with RCLKO[x], and the BRCLK and BRFPI inputs are ignored. Note that with the ELST bypassed, the system receive backplane must be timed to the recovered line rate (indicated on the RCLKO[x] output).

BRFPO[x] is a feed-through of the RFP[x] signal, but will not be aligned with the RFP[x] output due to differences in the path delays. The BRFPO[x] signal will indicate the frame alignment (the first bit of Timeslot 0) of the BRPCM[x] and BRSIG[x] signals.

Additionally, BRFPO[x] can be configured as a multiframe pulse (controlled by the BRXCMFP bit in Register 001H, 081H, 101H, 181H). When BRFPO[x] is configured as a multiframe pulse (BRXCMFP=1), then the multiframe boundaries of the BRPCM[x] and BRSIG[x] data will be aligned to BRFPO[x].

Note that the first bit of Timeslot 0 in the BRPCM[x] and BRSIG[x] output signals will always be aligned to the BRFPO[x] pulse.

Q12) Does the EQUAD meet ETSI CTR 12 output jitter requirements?

A12) Some 2048 kbit/s output jitter requirements, such as ETSI's CTR 12, will require more jitter attenuation than is provided by default by the DJAT functional block of the EQUAD.

However, this is easily remedied since the DJAT's jitter transfer function is programmable using the DJAT Divisor registers (019H, 099H, 119H, 199H and 01AH, 09AH, 11AH, 19AH). The use of these registers to change the jitter transfer function is explained in the Using the Digital Jitter Attenuator section of the EQUAD data book.

Simply, if more attenuation is required, the values of the DJAT Divisor registers should be increased. If a line rate (2048 kbit/s) clock is being used as the DJAT reference, then programming Registers 19H, 099H, 119H, 199H and 1AH, 09AH, 11AH, 19AH both to FFH will provide the maximum attenuation, thus meeting CTR 12 output jitter requirements.

Because the EQUAD uses a digital PLL in its jitter attenuator, its intrinsic jitter term can be significant. If an LIU having lower intrinsic jitter is used in conjunction with the EQUAD it is recommended that the LIU's jitter attenuator be used.

PMC-Sierra's PM4314 QDSX quadruple T1/E1 LIU device contains a digital jitter attenuator similar to the EQUAD's. In designs where the QDSX is being used with the EQUAD, it is recommended that both jitter attenuators be enabled in series (i.e. both in transmit path) and that the attenuation in both be increased to maximum (by setting the DJAT Divisor registers to FFH).

Q13) Can each quadrant of the EQUAD be configured for different framing modes?

A13) Yes, each quadrant in the EQUAD has separate control registers for the framing format (CRC Multiframe, Signalling Multiframe). Additionally, the receive and transmit framing configuration of each quadrant are also independent of one another. This flexibility allows the EQUAD to be used in inter-working (mixed-mode) applications.

Q14) Can each quadrant of the EQUAD have different timing options?

A14) Yes, each quadrant of the EQUAD can generally be operated with different timing options, but there are some exceptions.

When the EQUAD is interfacing to a synchronous backplane, all four quadrants will share receive backplane timing via the common BRCLK and BRFPI inputs.

When the EQUAD is in the backplane bit-interleaved multiplexed mode (MENB pin asserted low), all the quadrants share both receive backplane timing, via the MRCLK and MRFPI inputs, and transmit backplane timing, via the MTCLK and MTFP inputs.

Every quadrant can be independently configured for jitter attenuation enabled or disabled (controlled by the FIFOBYP bit in Register 004H, 084H, 104H, 184H) with the jitter attenuation placed in the receive or transmit path (controlled by the RCLKOSEL bit in Register 001H, 081H, 101H, 181H). When jitter attenuation is required in one or more quadrants, a 49.152 MHz clock must be applied to the XCLK input. Otherwise, a 16.384 MHz clock can be applied.

Q15) Can each quadrant of the EQUAD be looped back independently?

A15) Yes, each quadrant in the EQUAD has a separate Master Diagnostics Register (00AH, 08AH, 10AH, 18AH) which provides independent loopback capability.

There are three loopback modes available per quadrant as described in the Using the Loopback Modes section of the EQUAD data book.

Q16) What is the purpose of the EQUAD's Multiplexed Backplane format?

A16) In high density designs, it is often useful to reduce the number of signal traces which must be routed across printed circuit boards or through connectors. For this purpose, the EQUAD provides a bit-interleaved multiplexed backplane format.

In this multiplexed format, the EQUAD's four BRPCM[x] and BRSIG[x] outputs are multiplexed into a single 16.384 Mbit/s output (MRD) and the four BTPCM[x] and BTSIG[x] outputs are demultiplexed from a single 16.384 Mbit/s input (MTD). This provides a eight-to-one reduction in the number of traces which must be routed across the system backplane.

Note that the bit-interleaved multiplexed backplane mode can only be used when all four channels share the same system timing as indicated on MRFPI, MTFP, MRCLK and MTCLK.

CONTACTING PMC-SIERRA

PMC-Sierra, Inc.
105 - 8555 Baxter Place
Burnaby, B.C.
Canada V5A 4V7

Telephone: 604-415-6000
Facsimile: 604-415-6200

Product Information: info@pmc-sierra.bc.ca
Applications information: apps@pmc-sierra.bc.ca

World Wide Web Site: http://www.pmc-sierra.com

NOTES

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