PM7346

S/UNI™ QJET

S/UNI-QJET WITH FREEDM-8

REFERENCE DESIGN

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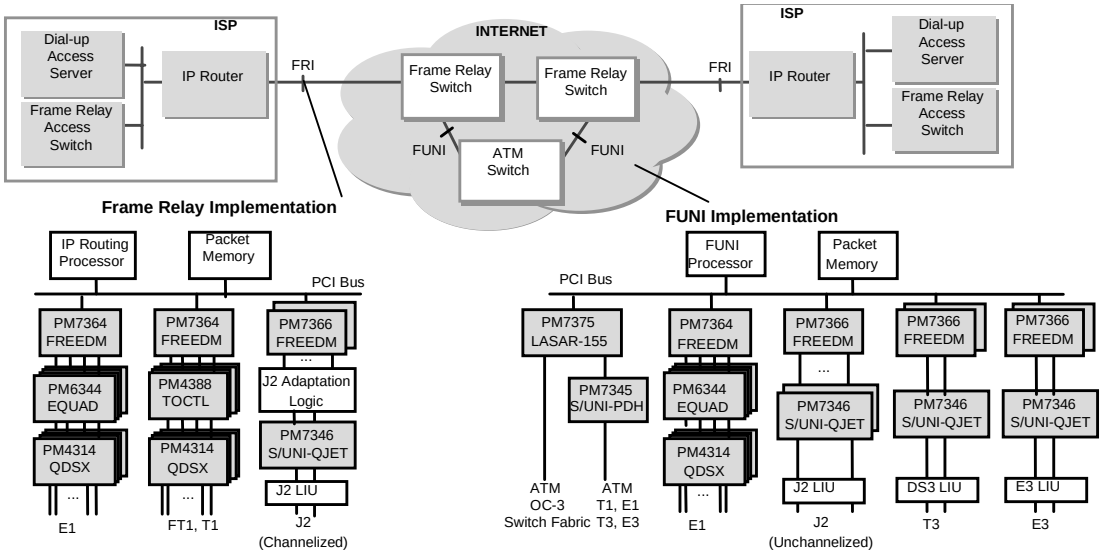
1.1 Application Perspective

The S/UNI-QJET standard product is a Quad ATM User Network Interface with on chip J2, E3, and T3 framers. By bypassing ATM User Network Interface functions, the S/UNI-QJET functions as a framer only which can be interfaced with the FREEDM-8 standard product to create J2, E3, and T3 interfaces for frame relay applications.

Frame relay is a multiplexed data networking technology supporting connectivity between user equipment (routers, nodal processors/fast packet switches) and between user equipment and the public frame relay network. The frame relay protocol supports data transmission over a connection-oriented path and enables the transmission of variable-length data units over an assigned virtual connection.

Frame relay technology can be used in LAN interconnection, Internet access and Internet backbones using link speeds ranging from 9600 baud to the DS3 rate. Figure 1 illustrates a typical implementation of a frame relay interface (FRI) and a frame relay user to network interface (FUNI) using fractional T1 (FT1), T1, E1, J2, E3 and DS3 rates. Other line options such as SONET virtual tributary (VT) mapping are not shown in the illustration.

Figure 1: - Frame Relay Inter-networking Overview



User equipment such as routers, T1 multiplexers, front end processors (FEPs), and packet assemblers/dissemblers (PADS) need to support the frame relay interface in order for them to be connected to a private or a public frame relay network.

1.2 Design Constraints

The purpose of the "S/UNI-QJET With FREEDM-8" reference design is to serve as an example to assist designers of routers and frame relay switches to design their products using PMC-Sierra's S/UNI-QJET and FREEDM-8 standard products, as shown in figure 6.

This design illustrates the frame relay application with interfaces to channelized J2, and unchannelized J2, E3, and T3 data streams. The hardware which implements these interfaces is built, tested and debugged thereby assisting designers to more quickly bring their designs to market.

The following hardware constraints have been included in this design:

- Support the PCI local bus revision 2.1, which allows up to four PCI devices per PCI bus segment to be connected to a host processor and packet memory. This constraint allows the reference design to be implemented as an add-in card to any readily available processor board with a revision 2.1 compliant PCI bus. Up to four reference design cards can be interfaced to the processor board. Note that using an add in card also limits the number of FREEDM-8 devices in the design to one.

- Mechanical and electrical constraints for interfacing an add-in card to the processor board, as specified in revision 2.1 of the PCI local bus specification.

The software interfaces to the FREEDM-8 via a host processor on the PCI bus and enables support of network protocol layers necessary to transmit and receive data packets of a PVC. Host software procedures are provided to illustrate the following:

- PCI device location and memory resource assignment
- Reset of the hardware via software
- Initialization of the hardware, software and the packet memory
- Activation/deactivation of the hardware

- Provisioning/unprovisioning of PVCs
- Transmit and receive packet processing
- Error handling
- Diagnostics

The following software constraints have been included in this design:

- The FREEDM-8 data interfaces are the only interfaces the software has access to. The content of the user data field of the HDLC frame is not processed. Other upper layer functions such as congestion management, LMI protocol and multi-cast capability are not implemented.
- Source code is written in the C language and developed using the VxWorks Tornado development environment. Executable code can run on i960 or Pentium based processor boards.

1.3 References

[1] PMC-960835, PMC-Sierra Inc., PM7346 S/UNI-QJET Data Sheet, Issue 4, December, 1997.

[2] PMC-970930, PMC-Sierra Inc., PM7366 FREEDM-8 Data Sheet, Issue 1, September, 1997

[3] PMC-970240, PMC-Sierra Inc., PM7364 FREEDM-32 with TOCTL Reference Design, Issue 1, September, 1997

[4] PCI SIG, PCI Local Bus Specification, June 1, 1995, Version 2.1

[5] PCI Compact Specification, PCI Industrial Computers Manufacturers Group, 1995, Version 1.0

[6] PMC-970280, PMC-Sierra, "FREEDM-32 Software Reference Design" Application Note, March, 1997, Issue 1

[7] PMC-961061, PMC-Sierra, "FREEDM-32 PCI Bus Utilization and Latency Analysis" Application Note, February, 1997, Issue 1

[8] PMC-970281, PMC-Sierra, "FREEDM-32 Programmer's Guide" Application Note, March, 1997, Issue 1

[9] PMC- 971136 PMC-Sierra, “Channelizing J2 Streams with the FREEDM-8 and the S/UNI-QJET” Application Note, November, 1997, Issue 1

[10] PMC-970959 PMC-Sierra, “MC68340 Software for the “FREEDM with TOCTL” Reference Design

2 FEATURE OVERVIEW

This reference design provides the following features:

- Frame relay processing of up to 128 logical channels associated with two channelized J2 data streams. Frame relay processing of eight logical channels associated with unchannelized J2 data streams. Frame relay processing of two logical channels associated with unchannelized E3 or T3 data streams. A logical channel can be composed of a single unchannelized data stream , or an aggregate number , from 1 to 98,of 64 kbit/sec time-slots within a channelized J2 data stream.
- Interfaces to a host processor and packet memory via the PCI local bus.
- Interface to one of two unchannelized E3 links, two unchannelized T3 links, eight unchannelized J2 links, or two channelized J2 links.
- E3, T3, and J2 framing performed by S/UNI-QJET.

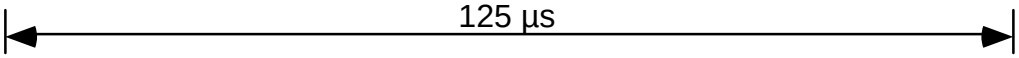
3 FUNCTIONAL DESCRIPTION

3.1 Overview

The S/UNI-QJET with FREEDM-8 reference design is an add-in card that connects the FREEDM-8 to a host processor and packet memory. The host processor may function as an IP routing processor, which serves to route packets among FREEDM-8 channels of the same reference design card, and/or FREEDM-8 channels of different reference design cards.

The line interface to this reference design is capable of interfacing to either one of the J2, E3, or T3 Plesiochronous Digital Hierarchy transport systems. The G.704 J2 standard specifies transmission at 6312 kbps with a 789 bit frame structure. The frame is divided into 98 byte time slots with 5 framing bits to end each frame. Four such structures are combined to create a J2 superframe. This structure is illustrated in figure 2 below.

Figure 2: - J2 Frame Format



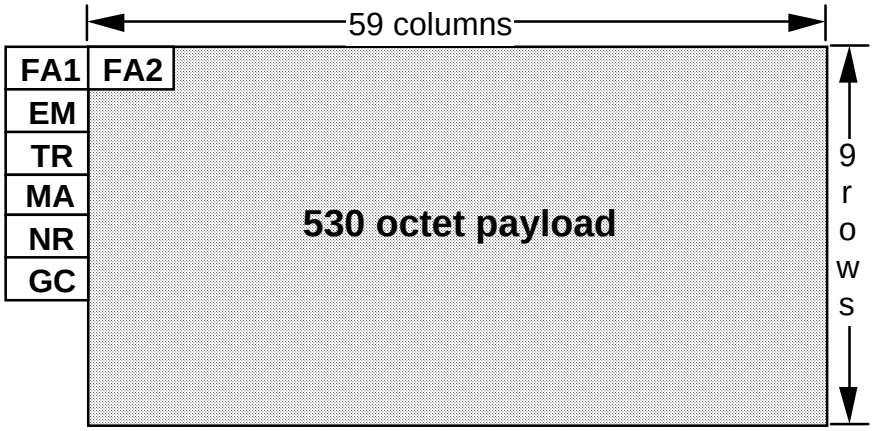
TS 1 - TS96 (96 Octets)	TS97	TS98	1	1	0	0	m
TS 1 - TS96 (96 Octets)	TS97	TS98	1	0	1	0	0
TS 1 - TS96 (96 Octets)	TS97	TS98	x1	x2	x3	a	m
TS 1 - TS96 (96 Octets)	TS97	TS98	e1	e2	e3	e4	e5

The E3 standard specifies a 34.368 Mbit/sec transmission rate. Both the G.751 and G.832 E3 specifications for frame formats are compatible with the S/UNI-QJET. These frame formats are shown in figures 3 and 4 respectively.

Figure 3: - G.751 E3 Frame Format

1	1	1	1	0	1	0	0	0	0	RAI	Na	372 Payload bits
C_{11}	C_{21}	C_{31}	C_{41}	380 Payload bits								
C_{12}	C_{22}	C_{32}	C_{42}	380 Payload bits								
C_{13}	C_{23}	C_{33}	C_{43}	J_1	J_2	J_3	J_4	376 Payload bits				

Figure 4: - G.832 E3 Frame Format



The S/UNI-QJET is also compatible with C-bit parity and M23 DS3 frame formats operating at 44.736 Mbit/sec. Both may be represented in figure 5 below.

Figure 5: - T3 Frame Format

	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits
M-subframe 1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

Differences in the two formats lie in the use of the C bits.

This card contains two S/UNI-QJET devices (labeled S/UNI-QJET-1 and S/UNI-QJET-2 in figure 6) and one FREEDM-8 device. The FREEDM-8 can support eight unchannelized links at 10 Mbit/sec per link, or two unchannelized links at up to 52 Mbit/sec per link. As a result, this reference design may interface to eight unchannelized J2 ports or two unchannelized E3 or T3 ports. Alternatively, the board may be configured for channelized J2 operation to support two J2 ports. Channelized J2 allows logical channels to be formed from an arbitrary selection of time slots in the J2 frame format allowing multiple

channels to exist on one channelized link. Unchannelized operation assumes no framing format or time slots and assigns each link to it's own single channel.

The S/UNI-QJET is a four port J2/E3/T3 SATURN user to network interface. As this reference design is not meant for ATM applications, ATM features such as ATM cell mapping and SCI-PHY and UTOPIA compliant interface, are not used. The S/UNI-QJET is operated in framer only mode, bypassing these functions.

FREEDM-8 is a HDLC processor with a PCI host interface capable of accepting data at an input rate of up to 52 Mbit/sec per port for two port operation, and up to 10 Mbit/sec per port for eight port operation with a maximum aggregate clock rate of 64 Mbit/sec. The reference board is capable of a maximum data rate of 89.47 Mbit/s using two unchannelized T3 ports and may be used as a DCE for J2, E3, and T3 data links.

The onboard microprocessor is used to monitor and control the onboard S/UNI-QJET devices as well as relay commands from an external terminal. This is done by connecting the microprocessor to the host via an RS-232 serial port. An onboard SRAM module is also present to buffer data being transferred.

Line interface units for E3 and T3 are used to interface the S/UNI-QJET units to physical E3 and T3 lines. Separate J2 Line interface units are used for J2 operation.

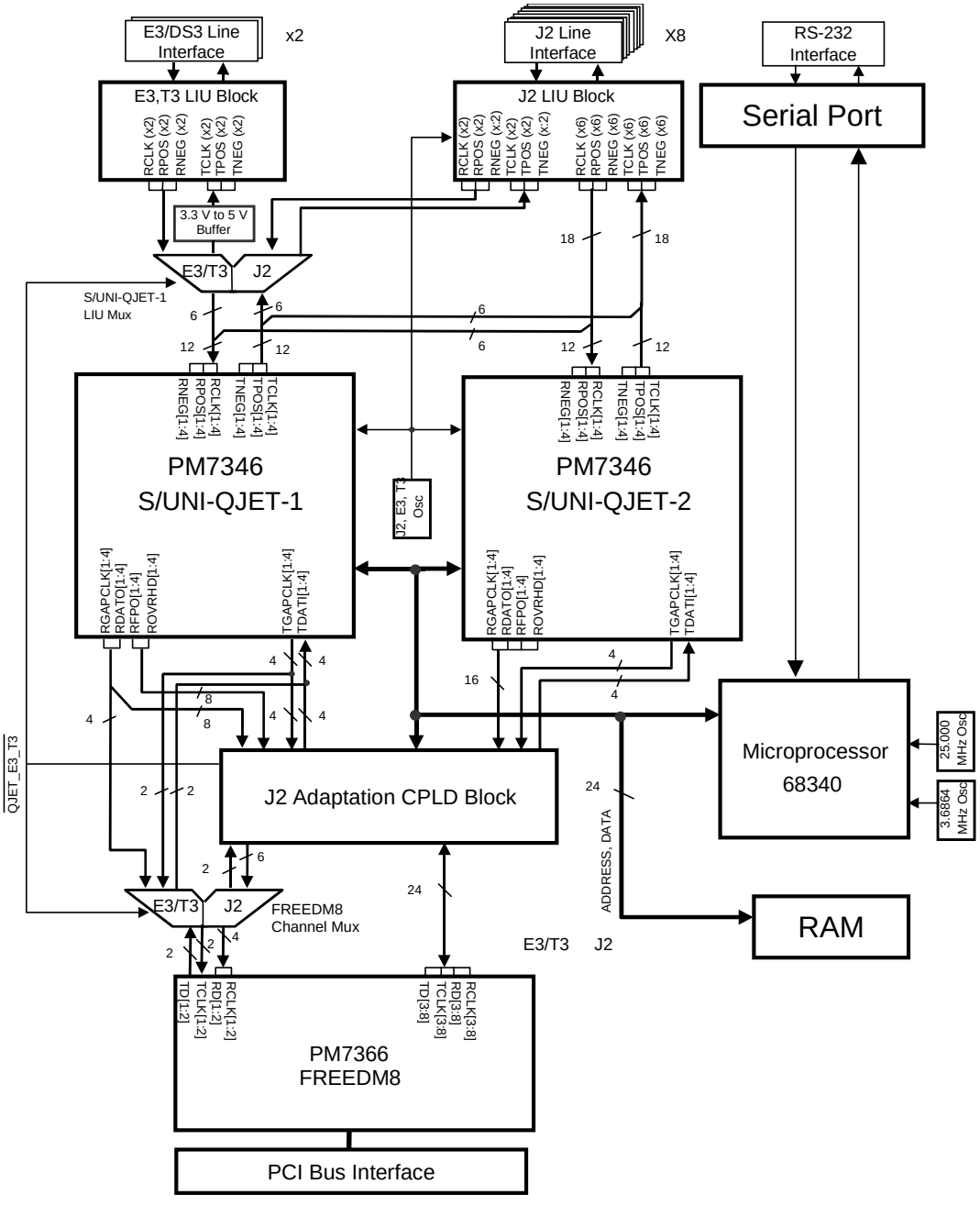
Some glue logic is required to interface the S/UNI-QJET and FREEDM-8 devices in J2 channelized mode. This is implemented in the J2 Adaptation CPLD. Multiplexers are used to maintain flexibility in the design and allow demonstration of various modes of operation possible when combining the S/UNI-QJET and the FREEDM-8 devices. One Multiplexer is used to select between J2 or E3/T3 LIU units to be used with ports 1 and 2 of S/UNI-QJET-1. Other multiplexers select between connecting the FREEDM-8 ports to either S/UNI-QJET devices or the J2 Adaptation CPLD Block.

Three onboard oscillators are required. One of them supplies the desired line rate at J2, E3, or T3. The second oscillator is used as a clock generator for the onboard microprocessor and the third is used to generate clock signals for the microprocessor's serial interface.

A block diagram of the reference design is shown in figure 6.

3.2 Block Diagram

Figure 6: - Reference Design Card Block Diagram



3.3 Data Flow

Data flowing to the host is received on one of the J2, E3, or T3 line interfaces. LIU units for each line decode the analog signals on the line to digital signals indicating negative and positive line pulses. Clock information is also recovered and converted to a digital signal. These signals are then passed to one of the line side link interfaces of the S/UNI-QJET devices. Each line side link interface consists of two data pins to receive the negative and positive pulse signals, and a clock signal; pins RNEG, RPOS, and RCLK respectively.

The exact path of the signals from the LIU's to the S/UNI-QJET-1 unit depends on the mode in which the board is operating. Signals for links one and two are selected by a bus switch and originate from either two of the J2 LIU's or the two E3/T3 LIU's. In unchannelized E3 or T3 mode, the E3/T3 LIU's are selected. In channelized or unchannelized J2 mode, the J2 LIU's are selected. The six other J2 LIU's are permanently connected to line side link interfaces of the S/UNI-QJET devices.

The data is framed by the S/UNI-QJET units which send the data, gapped clock, and framing information through the J2 Adaptation CPLD Block to the FREEDM-8. In unchannelized J2 mode, all eight links of the two S/UNI-QJET devices connect to a J2 link and pass data and gapped clocks to the FREEDM-8 without modification.

In channelized J2 mode, only links one and two of S/UNI-QJET-1 pass information to the eight FREEDM-8 links. The clock signals are demultiplexed to the FREEDM-8's ports by the J2 Adaptation CPLD Block to allow channelization of the two received J2 streams.

In unchannelized E3 or T3 mode, only links one and two of S/UNI-QJET-1 and the FREEDM-8 are active. The clock and data signals bypass the J2 Adaptation CPLD Block through a multiplexer to links one and two of the FREEDM-8.

Once the data has been processed by the FREEDM-8, it is passed to the host using DMA over the PCI bus interface.

In the transmit direction, data flowing from the host is passed to the FREEDM-8 using DMA over the PCI bus interface. This data is then passed through the J2 Adaptation CPLD Block to the two S/UNI-QJET devices. The links used to pass the data depend on the mode in which the board is being used.

In unchannelized J2 mode, all eight links of the FREEDM-8 pass data and gapped clocks to the two S/UNI-QJET devices without modification.

In channelized J2 mode, the eight FREEDM-8 links pass information to links one and two of S/UNI-QJET-1. The data signals are multiplexed to S/UNI-QJET-1's ports by the J2 Adaptation CPLD Block to allow channelization of the two received J2 streams.

In unchannelized E3 or T3 mode, only links one and two of S/UNI-QJET-1 and the FREEDM-8 are active. The clock and data signals bypass the J2 Adaptation CPLD Block through a multiplexer to links one and two of S/UNI-QJET-1.

The data is framed by the S/UNI-QJET units which send the positive and negative pulse, and clock information to the LIU's. The exact path of the signals from the S/UNI-QJET-1 unit to the LIU's depends on the mode in which the board is operating. Signal destinations for links one and two are selected by a bus switch to be either two of the J2 LIU's or the two E3/T3 LIU's. In unchannelized E3 or T3 mode, the E3/T3 LIU's are selected. In channelized or unchannelized J2 mode, the J2 LIU's are selected. The six other J2 LIU's are permanently connected to line side link interfaces of the S/UNI-QJET devices.

LIU units for each link encode the digital signals to J2, E3, or T3 analog signals. Clock information is also recovered and converted to a digital signal.

3.4 S/UNI-QJET

The PM7346 S/UNI-QJET is a quad ATM physical layer processor with integrated DS3 E3, and J2 framers. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation.

The S/UNI-QJET contains integral DS3 framers, which provide DS3 framing and error accumulation in accordance with ANSI T1.107, and T1.107a, integral E3 framers, which provide E3 framing in accordance with ITU-T Recommendations G.832 and G.751, and integral J2 framers, which provide J2 framing in accordance with ITU-T Recommendation G.704 and I.432.

When configured for DS3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

When configured for E3 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both HDB3-encoded bipolars or unipolar signals compatible with G.751 and G.832 applications.

When configured for J2 transmission system sublayer processing, the S/UNI-QJET accepts and outputs either or both B8ZS-encoded bipolar or unipolar signals compliant with G.704 and NTT 6.312 Mbit/s applications.

In the DS3 receive direction, the S/UNI-QJET frames to DS3 signals with a maximum average reframe time of 1.5 ms and detects line code violations, loss of signal, framing bit errors, parity errors, path parity errors, AIS, far end receive failure and idle code. The DS3 overhead bits are extracted and presented on serial outputs. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microcontroller port.

In the E3 receive direction, the S/UNI-QJET frames to G.751 and G.832 E3 signals with a maximum average reframe times of 135µs for G.751 frames and 250µs for G.832 frames. Line code violations, loss of signal, framing bit errors, AIS, and remote alarm indication are detected. Further, when processing G.832 formatted data, parity errors, far end receive failure, and far end block errors are also detected; and the Trail Trace message may be extracted and made available through the microcontroller port. HDLC receivers are provided for either the G.832 Network Requirement or the G.832 General Purpose Data Link support.

In the J2 receive direction, the S/UNI-QJET frames to G.704 6.312 Mbit/sec signals with a maximum average reframe time of 5.07ms. An alternate framing algorithm which uses the CRC-5 bits to rule out 99.9% of all static mimic framing patterns is available with a maximum average reframe time of 10.22ms when operating with a 10-4 bit error rate. Line code violations, loss of signal, loss of frame, framing bit errors, physical layer AIS, payload AIS, CRC-5 errors, Remote End Alarm, and Remote Alarm Indication are detected. HDLC receivers are provided for Data Link support.

Error event accumulation is also provided by the S/UNI-QJET. Framing bit errors, line code violations, parity errors, path parity errors and far end block errors are accumulated, when appropriate, in saturating counters for DS3, E3, and J2 frames. Loss of Frame detection for DS3, E3, and J2 is provided as recommended by ITU-T G.783 with integration times of 1ms, 2ms, and 3ms.

In the DS3 transmit direction, the S/UNI-QJET inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication Signals can be inserted by using internal register bits; other status signals such as the idle signal can be inserted when enabled by internal register bits. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at 1 C-bits for C-bit Parity application.

In the E3 transmit direction, the S/UNI-QJET inserts E3 framing in either G.832 or G.751 format. When enabled for G.832 operation, an HDLC transmitter is provided for insertion of either the Network Requirement or General Purpose Data Link into the appropriate overhead bits. The Alarm Indication Signal and other status signals can be inserted by internal register bits.

In the J2 transmit direction, the S/UNI-QJET inserts J2 6.312 Mbit/s G.704 framing. HDLC transmitters are provided for insertion of the Data Channels. CRC-5 check bits are calculated and inserted into the J2 multiframe. External pins are provided to enable overwriting of any of the overhead bits within the J2 frame.

The S/UNI-QJET also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms.

The S/UNI-QJET is configured, controlled and monitored via a generic 8-bit microcontroller bus through which all internal registers are accessed. All sources of interrupts can be identified, acknowledged, or masked via this interface.

3.5 FREEDM-8

The PM7366 FREEDM-8 Frame Engine and Datalink Manager device is a monolithic integrated circuit that implements HDLC processing, and PCI Bus memory management functions for a maximum of 128 bi-directional channels.

For channelized links, the FREEDM-8 allows up to 128 bi-directional HDLC channels to be assigned to individual time-slots within a maximum of 8 independently timed T1 or E1 links. The channel assignment supports the concatenation of time-slots (N x DS0) up to a maximum of 24 concatenated time-slots for a T1 link and 31 concatenated time-slots for an E1 link. Time-slots assigned to any particular channel need not be contiguous within the T1 or E1 link.

For unchannelized links, the FREEDM-8 processes up to 8 bi-directional HDLC channels within 8 independently timed links. The aggregate bandwidth of the unchannelized links must not exceed 65.536 Mbit/s in either direction. For example, the FREEDM could be used to process HDLC frames mapped into a single bi-directional DS-3 or OC-1 link or up to 8 bi-directional J2 links. The links can be of arbitrary frame format. When limited to two unchannelized links, each link can be rated at up to 45 Mbit/sec when host PCI clock is at 25 MHz and at up to 52 Mbit/sec when PCI clock is at 33 MHz. For lower rate unchannelized

links, the FREEDM-8 processes up to 8 links each rated at up to 10 Mbit/sec. In this case, the aggregate data rate of all the links is limited to 64 Mbit/sec.

3.6 J2 Adaptation CPLD Block

A Xilinx CPLD, the J2 Adaptation CPLD, is used to multiplex data signals and demultiplex clock signals between the S/UNI-QJET and the FREEDM-8, as well as generate transmit direction frame pulses, for channelized J2 operation. The J2 Adaptation CPLD also sets the correct data path for transmit direction signals via the S/UNI-QJET-1 LIU and FREEDM-8 channel multiplexers. The data path is dependent on the current operating mode. The J2 Adaptation CPLD Block also has additional bus switches to control the routing of signals between the S/UNI-QJET devices, the J2 Adaptation CPLD, and the FREEDM-8. During E3/T3 operation, the J2 Adaptation CPLD blocks data to/from ports 3 to 8 of the FREEDM-8. The J2 Adaptation CPLD is configured for a particular operating mode via microcontroller access to an internal register. Headers connected to the CPLD's JTAG port allows programming of the CPLD's internal logic using the appropriate Xilinx programming hardware.

3.7 Onboard Microprocessor

The Motorola 68340 is used to monitor and control the S/UNI-QJET and J2 Adaptation CPLD devices as well as perform FDL extraction. It provides the following features:

- 16-bit data bus
- Interrupt controller
- Address decoder
- Timer
- Serial interface

The 68340, is commonly used in many host applications, and its main advantage is that it requires a very small number of external components to be operational. The components include clock circuitry, RAM, ROM, and a serial interface (RS232). It also has an abundance of third-party software support, such as real-time operating systems and C-compilers. In addition, the 68340, has a built-in background debug function, which greatly simplifies the code debugging operation.

3.8 S/UNI-QJET-1 LIU Multiplexer

The S/UNI-QJET-1 LIU multiplexer performs signal selection to change between E3/T3 operation, and J2 (channelized or unchannelized) operation. The S/UNI-QJET-1 LIU multiplexer connects the RCLK, RPOS, RNEG, TCLK, TPOS, and TNEG signals of links one and two of S/UNI-QJET-1 to the appropriate two LIU's (either two E3/T3 LIU's or two J2 LIU's). As both transmit and receive signals pass through the S/UNI-QJET-1 LIU multiplexer, the multiplexer is implemented using a bi-directional bus switch which can also tie inputs not used in the current operating mode to ground.

3.9 FREEDM-8 Channel Multiplexer

The FREEDM-8 channel multiplexer performs signal selection to change between E3/T3 operation, and J2 (channelized or unchannelized) operation. The FREEDM-8 channel multiplexer connects RCLK, RD, TCLK, and TD signals of links one and two of the FREEDM-8 to either the J2 Adaptation CPLD (for channelized or unchannelized J2 operation) or the first two links of S/UNI-QJET-1. When connecting to S/UNI-QJET-1, the RDATO, RGAPCLK, TDATO, and TGAPCLK signals of the S/UNI-QJET are connected to the RD, RCLK, TD, and TCLK signals of the S/UNI-QJET, respectively. Bypassing the J2 Adaptation CPLD is required as the J2 Adaptation CPLD's propagation delay of 20 ns is too long to pass signals at T3 or E3 rates. As both transmit and receive signals pass through the FREEDM-8 channel multiplexer, the multiplexer is implemented using a bi-directional bus switch which can also tie inputs not used in the current operating mode to ground.

3.10 Buffer Ram

A single 64 KB module of static ram is used to buffer FDL data between the S/UNI-QJET and the host. FDL data in J2, E3, T3 data streams is extracted or inserted by the S/UNI-QJET units and accessed by microprocessor reads and writes to the appropriate S/UNI-QJET registers. Four FDL links are present for each QJET unit corresponding to the four J2, E3, or T3 links available on each.

3.11 3.3 Volt to 5 Volt Converter

The S/UNI-QJET uses a 5 volt reference pin to allow inputs to tolerate 5 volt input signals. However, the S/UNI-QJET can only produce a guaranteed output high voltage of 2.4 volts. Because most LIU's available require 5 volt signals, outputs from the S/UNI-QJET to the LIU's may require buffering. In this design, 74ACT541, advanced TTL compatible CMOS buffers, are used to convert the 2.4

volt output high voltage to the required 3.5 volt level required by the E3/T3 LIU units. Note that the J2 LIU used in this design is voltage compatible with the S/UNI-QJET and thus does not require a buffer.

3.12 E3/T3 Line Interface

Two TDK TSC 78P7200 LIUs are used to provide E3 and T3 interface to ports 1 and 2 of S/UNI-QJET-1. In T3 mode, the LIU converts transmit digital B8ZS encoded data to its analog equivalent and converts receive analog B8ZS to its digital equivalent. In E3 mode, the LIU converts transmit digital HDB3 encoded data to its analog equivalent and converts receive analog HDB3 to its digital equivalent.

In the receive direction, the LIU provides a CMOS level receive clock, and positive and negative receive data. In the transmit direction the LIU receives a CMOS level transmit clock, and positive and negative transmit data. CMOS level signals are compatible with the S/UNI-QJET's inputs. However, as the S/UNI-QJET is a 3.3 V device, a voltage buffer is required to boost the output signals of the S/UNI-QJET to match the levels required by the 78P7200.

3.13 J2 Line Interface

Eight Transwitch MRT TXC02050 J2 LIUs are used to provide the J2 line interface to the S/UNI-QJET devices. The LIU converts the digital B8ZS encoded data to its analog equivalent and converts analog B8ZS to it's digital equivalent.

In the receive direction, the LIU provides TTL level receive clock, and positive and negative receive data. In the transmit direction the LIU receives TTL level transmit clock, and positive and negative transmit data. The TTL input and output levels are directly compatible with the S/UNI-QJET. Buffers are required on the line side to drive the line transformers.

3.14 Serial Interface

An RS-232 serial connector is used to interface the onboard microprocessor to the host. Commands to configure the S/UNI-QJET and J2 Adaptation CPLD devices as well as data to indicate the status of the S/UNI-QJET devices are sent over this interface.

3.15 PCI Interface

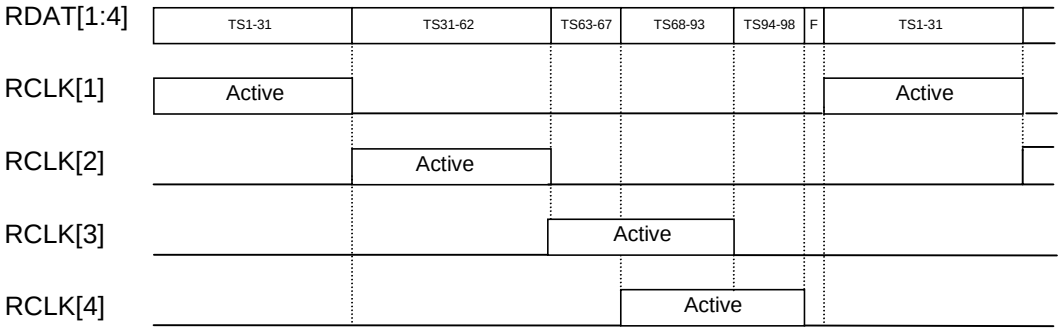
The PCI interface allows communication between the host and the FREEDM-8 device. Configuration of the FREEDM-8 occurs via this interface. Transfer of HDLC data is performed by DMA to host memory.

3.16 Channelized J2 Multiplexing Scheme

In channelized J2 transmission, all eight of the FREEDM-8's ports are utilized to accommodate two J2 ports of S/UNI-QJET-1. S/UNI-QJET-2 is not used in channelized J2 operation. To allow the FREEM8 device to perform time slot channel assignment of a J2 stream, data must be presented to the FREEDM-8 such that it is in an E1 format at each input. On the receive side, this is done by delivering J2 data from one of the S/UNI-QJET ports, in common, to four of the eight ports of the FREEDM-8. The corresponding clock signals are also distributed to the four FREEDM-8 ports but at different intervals for each port. On the transmit side, this is done by multiplexing four E1 data streams of the corresponding FREEDM-8 ports to the one corresponding S/UNI-QJET port. Clock signals are delivered in exactly the same fashion as in the receive side. The multiplexing scheme is implemented by the J2 Adaptation CPLD which acts as an interface between the S/UNI-QJET and FREEDM-8 devices during this mode of operation.

Four ports are required as each port can only handle 31 eight bit time slots of data for each frame, while J2 delivers 98 time slots per frame. The FREEDM-8 requires that 31 timeslots of information be sampled by each port during a frame. Frame boundaries are detected by the FREEDM-8 after the receive clock for a port has been inactive for a duration specified through the FREEDM-8's RCAS Framing Bit Threshold register. As the combined capacity of the four E1 ports exceeds the required 6.312 Mbit/s throughput of J2, a portion of the sampled data will be common between ports 3 and 4. This redundant data may be ignored by assigning all redundant time slots to an arbitrary channel that the FREEDM-8 subsequently ignores. The receive timing for channelized J2 is shown in figure 7.

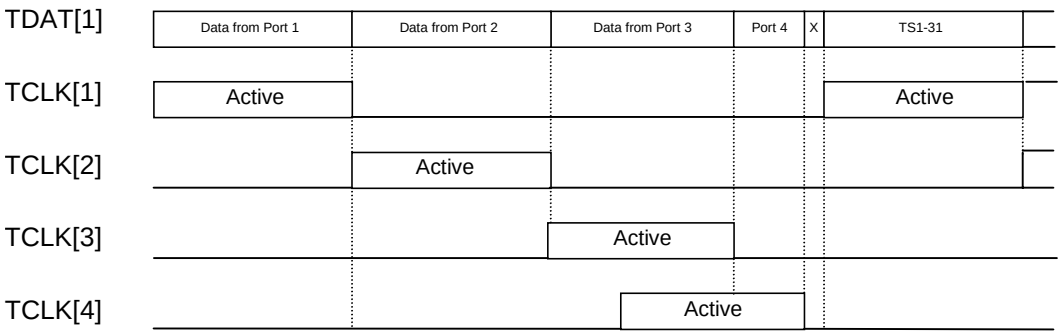
Figure 7: - J2 Receive Timing Diagram



RCLK[1:4] are the receive clocking signals passed from the S/UNI-QJET through the J2 Adaptation CPLD to the FREEDM-8, and RDAT[1:4] is the J2 data delivered in common to four of the FREEDM-8's data inputs through the J2 Adaptation CPLD. "F" represents the 5 bit framing pattern of the J2 format. Each of ports 1 to 3 receives continuous clock signals for a 31 timeslot duration. Note that port 4 has redundant time slots from time slot 68 to time slot 93. RCLK[1:4] signals are kept low when not active.

In the transmit direction, data from the four E1 ports must be multiplexed in reverse fashion to form a single J2 port that is presented to the S/UNI-QJET. Each FREEDM-8 port takes a turn sending data to the S/UNI-QJET port with the fourth port only sending data during the last five time slots. The corresponding timing is shown in figure 8.

Figure 8: - J2 Transmit Timing Diagram



TCLK[1:4] are the receive clocking signals passed from the S/UNI-QJET through the J2 Adaptation CPLD to the FREEDM-8. TDAT[x] is the data from the FREEDM-8 delivered to one of the S/UNI-QJET's J2 ports. The signal source is

indicated in each box. The "X" corresponds to the position of the framing pattern which is ignored by the S/UNI-QJET. TCLK[x] signals are kept low when not active. For further information, refer to "Channelizing J2 Streams with the FREEDM-8 and S/UNI-QJET"[10].

3.17 Unchannelized J2, E3, T3 Operation

During unchannelized operation of the board, each active port is assigned a separate channel by the FREEDM-8. In unchannelized E3/T3 mode, only ports 1 and 2 of the FREEDM-8 are active. These ports are connected, through the FREEDM-8 Channel multiplexer, to ports 1 and 2 of S/UNI-QJET-1. S/UNI-QJET-2 is not active during unchannelized E3/T3 operation.

In unchannelized J2 operation, all eight ports of the FREEDM-8 and both S/UNI-QJET units are active. Data transferred between the two S/UNI-QJET units and the FREEDM-8 are passed transparently through the J2 Adaptation CPLD Block. S/UNI-QJET-1's ports are connected to ports 1 to 4 of the FREEDM-8 while S/UNI-QJET-2 is connected to ports 5 to 8.

3.18 E3/T3 LIU Jumpers

The E3/T3 LIU transceivers utilize the same receive and transmit line transformers for both E3 and T3 operation. Other components which are used to determine the operating frequency and termination impedance are not common between the two modes and require jumpers to select the correct circuit for a particular operating mode.

4 EXTERNAL INTERFACE SIGNAL DESCRIPTION

This board has an RS-232 interface and a PCI interface. The RS-232 interface provides a user interface for configuration and monitoring of the board. The PCI interface connects the board to a host processor with packet memory.

4.1 RS-232 Serial Interface

Table 1 - RS-232 Interface Signals Description

Signal	Type	PIN NO.	Description
DCD	I	1	Data Carrier Detect
RXD	I	2	Serial Receive Data
TXD	O	3	Serial Transmit Data
DTR	Not Used	4	Data Terminal Ready
GND	Ground	5	Signal Ground
DSR	I	6	Data Signal Ready
RTS	I	7	Request to Send
CTS	I	8	Clear to Send
RI	I	9	Ring Indicator

4.2 PCI Interface

PCI interface signal descriptions may be found in “PCI Local Bus Specification” [4].

Timing for the signals may be found in the FREEDM-8 data sheet[2].

5 IMPLEMENTATION DESCRIPTION

5.1 Sheet 1: Top Level Drawing

This sheet provides an overview of the design. Major functional blocks are shown with signals that connect the blocks. A description of each block can be found in section 3.

5.2 Sheet 2: FREEDM-8 Block

- The FREEDM-8 (U4) is connected to the host through a 32 bit PCI card connector (P1). The host configures the FREEDM-8 device, as well as transmits and receives data through this interface.

- TD[2:1] is used during high speed E3 and T3 operation. Source terminating resistors are placed in series with TD [2:1] to minimize reflection when operating at these high bit rates.

5.3 Sheet 3: Power and Decoupling

- Connectors (J14) supply the +5 V (VCC) and GND from the motherboard power supply. This supply is routed directly to all parts requiring +5 V power.

- +3.3 V power to the FREEDM-8 device is supplied via voltage regulator U27 from the 5 V PCI power.

- +3.3 V power to the S/UNI-QJET devices is supplied from either voltage regulator U22 or voltage regulator U27. Voltage regulator U22 supplies power from the motherboard power, while voltage regulator U27 supplies power from the 5 V PCI bus power.

5.4 Sheet 4: Signal Multiplexing Logic

- The CPLD (U9) generates the signal T3 which is used to select the appropriate LIU pulse transmission characteristics for T3 or E3 (when the signal T3 is low). The CPLD also generates TFPI signals for S/UNI-QJET-1during channelized J2 operation.

- Bits 5, 6 and 7 of the CPLD's internal configuration register are used to set or clear T3, NOT_UNCHAN_J2, and NOT_E3_T3 bits respectively.

- The data paths to and from the FREEDM-8 are selected to be either passing through the CPLD, or coming directly from the S/UNI-QJET units. The FREEDM-8 Channel Multiplexer (U11) selects the proper data path for ports 1 and 2 of the FREEDM-8 while bus switches U12 and U13 perform the same function for ports 3 to 8. Use of these additional bus switches greatly reduces the resources that would be required of the J2 Adaptation CPLD to perform this additional routing internally.

- Data paths are selected using two signals (NOT_QJET_E3_T3 and UNCHAN_J2) which indicate the operating mode of the board (NOT_QJET_E3_T3 and NOT_UNCHAN_J2 are [1, 1] for channelized J2, [1, 0] for unchannelized J2, and [0, 1] for E3/T3).

- Headers (J2) are connected to the JTAG access pins of the CPLD to allow in system reprogramming of the device.

5.5 Sheet 5,6: S/UNI-QJET Block

- TICLK is delivered in common to all eight TICLK inputs of the two S/UNI-QJET devices.

- 75 ohm resistor source terminations are placed in series with connections associated with ports one and two of S/UNI-QJET-1 (U14). These terminations are to reduce reflections on these lines during high speed E3 and T3 operation.

- A single bus switch (U16) acts as the S/UNI-QJET-1 LIU multiplexer and selects the appropriate set of LIU signals to route to ports one and two of S/UNI-QJET-1. Ports one and two are connected to signals from the two E3/T3 LIU's in unchannelized E3 or T3 mode. Ports one and two are connected to signals from two of the J2 LIU's in channelized and unchannelized J2 operation. The NOT_QJET_E3_T3 signal is used to control the bus switch.

- A +5 V voltage reference is connected to the BIAS pins of the two S/UNI-QJET devices to enable the S/UNI-QJET to tolerate +5V inputs.

- Care is required when routing RDATO[3:0] and RGAPCLK[3:0]. Because the hold time of the FREEDM-8 and the propagation delay of the S/UNI-QJET are both 2 ns, layout should be done to ensure that RDATO[3:0] arrives at the FREEDM-8 at the same time or later than RGAPCLK[3:0].

5.6 Sheet 7,8: J2 Line Interface

- Buffers U31 and U44 are used to drive line transformers in the transmit direction to ensure current capabilities of the LIU are not exceeded.

- Ferrite beads and capacitors are used to filter noise in the power supply.

5.7 Sheet 9: E3/T3 Line Interface

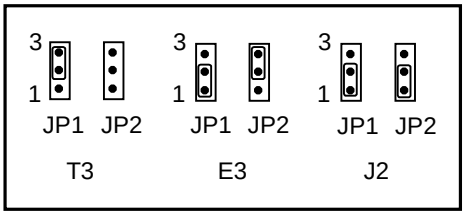
- High slew rate buffers (U3) are used to drive terminal side signals from the LIU units U49 and U50. This is done to avoid possible distortion due to slow rise and fall times of the LIU, coupled with the TTL input thresholds of the S/UNI-QJET device.

- Jumpers JP5, JP6, JP7, JP8, JP9, JP10, JP11, and JP12 are used to select the appropriate analog circuitry used in E3 operation or T3 operation. By setting all jumpers to connect the second and third pins, circuitry for T3 operation is selected. By setting all jumpers to connect the first and second pins, circuitry for E3 operation is selected.

5.8 Sheet 10: Timing

- Jumpers JP1 and JP2 are used to select the appropriate operating frequency for the desired line rate (E3, T3, or J2). For T3 operation, pins three and two of JP2 should be connected. For E3 operation, pins one and two of JP2 should be connected as well as pins two and three of JP1. For J2 operation, pins one and two of JP2 should be connected as well as pins one and two of JP1. These settings are shown in figure 9 below

Figure 9 - Jumper Settings for Timing Block



- Signals are buffered and series terminated to avoid distortion of the clock due to heavy load or reflection.

5.9 Sheet 11: Microprocessor Interface

- MAX203 (U8) (+5V supply only, and no external capacitors needed) is used for the RS232 interface. A 3.6864MHz oscillator shown as Y5 is used for the RS232 interface.

- The reset circuit, controlled by switch SW1, resets the MC68340 and provides RSTB to reset all other devices.

- Background Debug Monitor (BDM) connector, J4, is used for software development. Note that pin BKPTB must be pulled-up to VCC (through 10K). It is recommended that pin BERRB be pulled up also in a similar fashion. CLKOUT from the MC68340 needs to be connected to a test point to be used by the BDM connector. XFC pin of the MC68340 needs to be de-coupled with 0.1uF to ground.

- Other details on the MC68340:

  - XTAL must be left open if external oscillator used for SYSCLK, which is the case in this reference design

  - VCCSYN needs to be pulled up to VCC

  - All unused inputs are pulled up through 10K

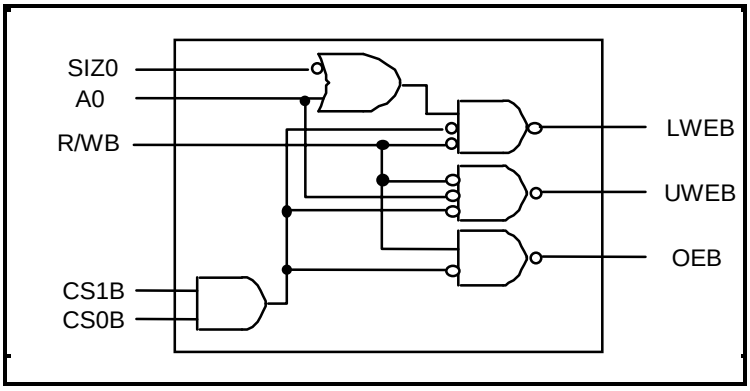
- De-coupling Capacitors of 0.01uF are used for each power pin of the MC68340.

5.10 Sheet 12: Microprocessor Decode Logic

- The data pins D8 through D15 of the MC68340 are extended to the two S/UNI-QJET, and the J2 Adaptation CPLD via an 8-bit transceiver (U24). These same data pins combined with the D0 through to D7 data pins from another transceiver(U25) are extended to the SRAM (U5 and U6) and EPROM (U15).

- The 32 Kword of SRAM is driven for read or write access by decode logic within a 22V10 PAL (U10). Figure 10 shows the decode logic based on the MC68340 signals provided to the PAL.

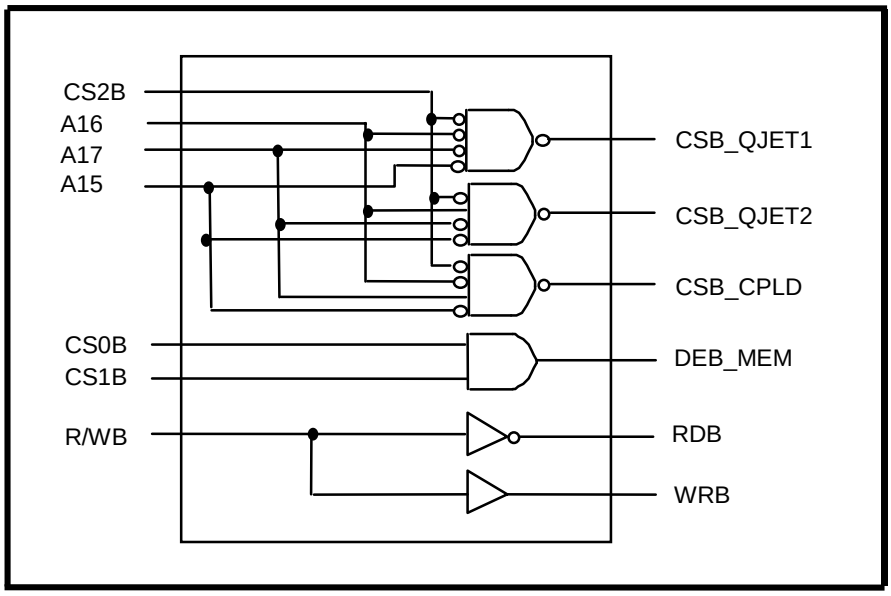
Figure 10: - Logic of signals provided to SRAM



Note: CS1B and CS0B are AND'ed together (i.e. either CS0B or CS1B asserted) since the MC68340 always asserts CS0B during code download into SRAM using the background debug monitor, while it asserts CS1B during normal SRAM accesses. This applies to the case where only the SRAM is being used (typically during code development). If the EPROM is used (which is selected by CS0B), then this AND gate should be removed, and only CS1B should be used here.

- CS0B of the MC68340 provides an active low chip select to the EPROM.
- CS2B of the MC68340 provide an active low chip select to the two S/UNI-QJET, and the J2 Adaptation CPLD using the decode logic shown in figure 11. The decode logic is implemented by the 22V10 PAL. The RDB and WRB signals are also derived from the R/WB signal.
- The decode logic of the PAL in figure 11 also provides an output enable to the data transceiver connected to the SRAM and EPROM. CS2B is used as the output enable to the data transceiver connected to the S/UNI-QJET devices, and the J2 Adaptation CPLD.

Figure 11:- J2 Adaptation CPLD, S/UNI-QJET, Transceiver Decode Logic



- Wait states are required during read accesses to the two S/UNI-QJET devices. The S/UNI-QJET datasheet specifies a maximum propagation delay of 70ns, which implies that 1 wait state is necessary to interface the MC68340 with the S/UNI-QJET devices. The wait state is programmed via a register within the MC68340 such that whenever the CS2B is active there is one wait state inserted.

6 SOFTWARE RESOURCE AND CONFIGURATION REGISTER MAP

6.1 PCI to Host Software Interface

The FREEDM-8 is configured, controlled and monitored across the PCI bus interface by a host processor and packet memory (RAM). In some configurations there may be multiple reference design cards on the PCI bus, and during a bus transaction one of the FREEDM-8 devices may act as the bus master in accessing the packet memory, or the host processor may act as the bus master in accessing one of the FREEDM-8 registers of a reference design card.

Figure 12 shows an address map for a PCI bus, which shows one FREEDM-8 device. The data structures shown are required to interface one FREEDM-8 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses, which can be observed at the address pins of the PCI bus interface.

When multiple FREEDM-8's are attached to the bus each FREEDM-8 must have a unique set of the following data structures.

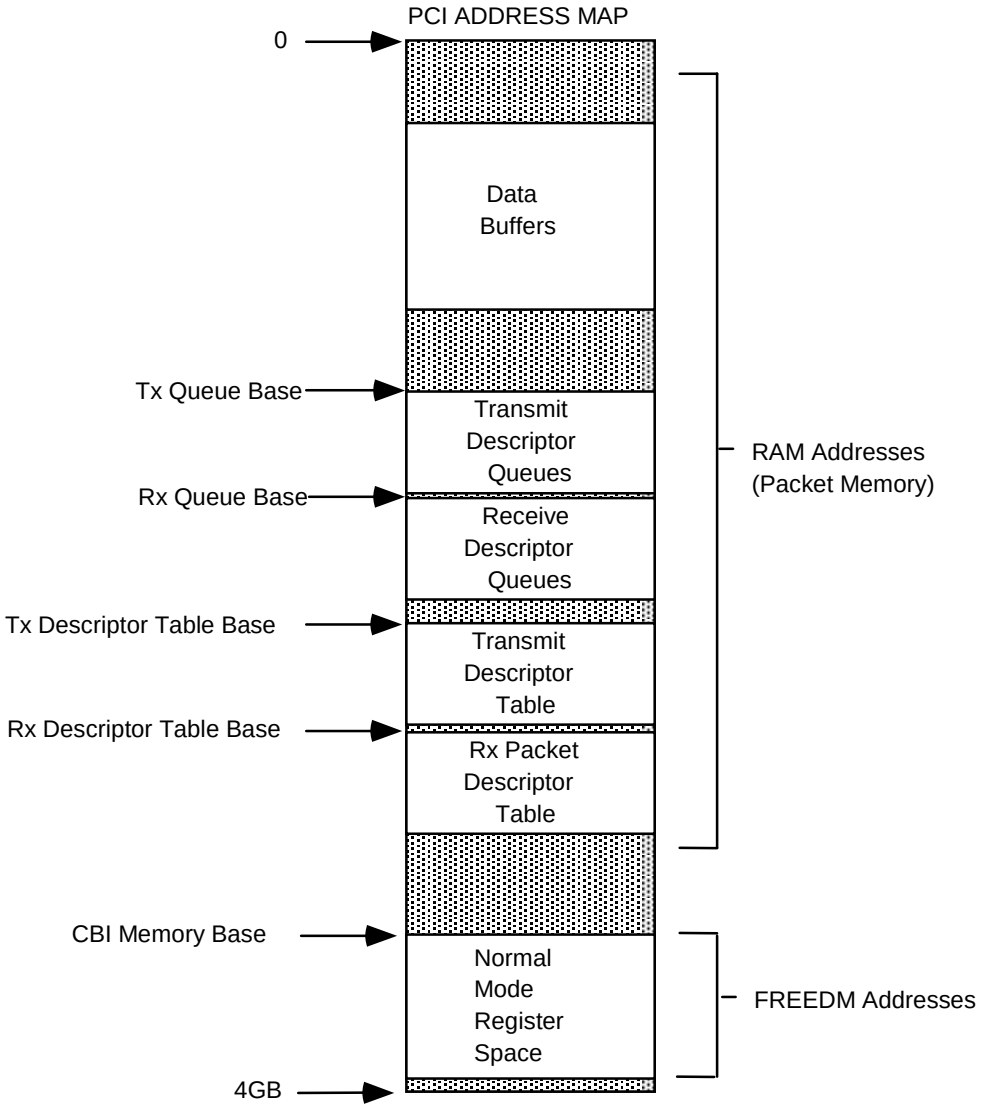
- Transmit Descriptor Table
- Receive Descriptor Table
- Transmit Queue Space
- Receive Queue Space
- Normal Mode Register Space

The data structures within packet memory are accessed by software running on the host processor, or by the FREEDM-8. The software specifies the location of these data structures by writing base addresses into the appropriate FREEDM-8 registers, before activating the FREEDM-8.

The data Buffers are filled with the data received by the FREEDM-8, or contain transmit data which is read by the FREEDM-8. The descriptor tables and the queues are required to manage these buffers.

The Normal Mode Register space is accessed by the software running on the host processor to manage and control operation of a FREEDM-8 device. This register space is located in the FREEDM-8 and is mapped into the PCI address space by the software running on the host processor during the boot-up sequence.

Figure 12: -PCI Address Map



The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device (the FREEDM-8 in this case), and is accessed by the host processor in a PCI bus Configuration Read (or Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough discussion of it can be found in the PCI specification[4].

The software running on the host processor should be similar to that of the FREEDM with TOCTL Reference design. Details of this software can be found in the "MC68340 Software for the FREEDM with TOCTL Reference Design" Document[10].

6.2 On Board Software Interfaces

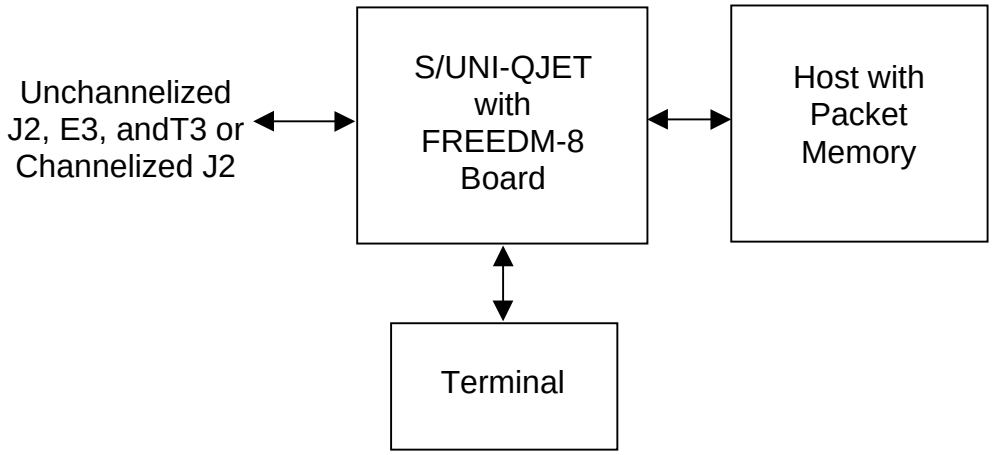
The firmware in the ROM enables reading and writing to registers. This enables the QJET and J2 Adaptation CPLD devices to be reset, initialized, and monitored for errors etc. Please refer to "MC68340 Software for the FREEDM with TOCTL Reference Design" [9] document for more information as software for the FREEDM with TOCTL Reference Design will be similar.

7 OPERATIONS

7.1 System Setup

The S/UNI-QJET with FREEDM-8 reference design is to be connected to a terminal and a host with packet memory as shown in figure 13 below.

Figure 13: Operating Environment of the S/UNI-QJET with FREEDM-8 Reference Board



The terminal is connected to the card by the RS 232 serial port and provides a user interface to configure and monitor the two S/UNI-QJET devices. The host with packet memory is connected directly to the FREEDM-8 by the PCI bus interface. The PCI bus interface allows multiple S/UNI-QJET with FREEDM-8 boards to connect to the same host via the PCI bus. On the line side, the board supports unchannelized J2, E3, and T3 traffic, and channelized J2 traffic.

7.2 Operating Modes

The S/UNI-QJET device supports framing for four J2, E3, and T3 frame formats. The FREEDM-8 device supports up to eight unchannelized links at 10 Mbit/sec per link, up to two high speed unchannelized links at 52 Mbit/sec per link, and up to eight channelized links in E1 or T1 frame formats. The reference board uses these features of the S/UNI-QJET and FREEDM-8 devices to allow four different modes of operation – unchannelized J2, E3, T3, and channelized J2.

7.2.1 Unchannelized J2

Unchannelized J2 uses two S/UNI-QJET devices to frame eight J2 data streams (four J2 streams per S/UNI-QJET device). The FREEDM-8 is configured for eight unchannelized links which receive and transmit data in eight J2 streams framed by the two S/UNI-QJET devices. One logical HDLC channel is assigned by the FREEDM-8 to each link.

7.2.2 Unchannelized E3 and T3

Unchannelized E3 and T3 use two ports of S/UNI-QJET-1 to frame two E3 or T3 data streams; other ports of S/UNI-QJET-1 and 2 are left unused. The FREEDM-8 is configured for two high speed unchannelized links which receive and transmit data in the two E3 or T3 streams. One logical HDLC channel is assigned by the FREEDM-8 to each link. Care should be made to ensure that delay on lines for clock and data signals of the two ports are equal to ensure proper operation.

7.2.3 Channelized J2

Channelized J2 requires the mapping of the 98 byte time slots of J2 into four separate 31 byte time slot E1 frames. Two ports of S/UNI-QJET-1 are used to frame two J2 data streams; other ports of S/UNI-QJET-1 and 2 are left unused. These streams are mapped to eight E1 streams by the J2 Adaptation CPLD. The FREEDM-8 device sends and receives channelized data on these E1 streams. Logical channels may be formed out of 1-98 time slots within each J2 stream. This is done by assigning the desired number of timeslots, from the four associated E2 streams, to a logical channel. If timeslots 97 and 98 are to be used for data, rather than signalling, the J2SIGTHRU bit in the S/UNI-QJET FRMR LOF Status register of S/UNI-QJET should be set to ‘1’. Otherwise, data transmitted during timeslots 97 and 98 will be overwritten by S/UNI-QJET-1. The byte patterns set in the J2-TRAN TS97 Signaling and J2-TRAN TS98 Signaling registers of S/UNI-QJET-1 would then be inserted into timeslots 97 and 98 respectively.

8 BILL OF MATERIALS

NO.	Part Name - Value	Jedec Type	Ref Des	Qty
1	1N4148-1N4148W	SOD-123	D4-D11	8
2	74AC11004	DIP20_3	U3	1
3	74FCT541_SOIC-BASE	SOIC20W	U1	1
4	74FCT541_SOIC1-BASE	SOIC20W	U7, U31, U44	3
5	74HCT00_SOIC-123_XXXXXX	SOIC14	U2	1
6	74XXX245_SOIC-HCMOS	SOIC20W	U24, U25	2
7	78P7200_PLCC-BASE	PLCC28	U49, U50	2
8	BNC_AMPHENOL-BASE	AMPHENOL_BNC	J3, J6-J13, J15-J25	20
9	CAPACITOR-0.001UF	SMDCAP805	C5, C60, C79, C136, C164	5
10	CAPACITOR-0.01UF, 50V, X7R_805	SMDCAP805	C11-C16, C23-C26, C30-C42, C62, C64, C108, C109, C129-C133, C138, C139, C141, C142, C145-C152, C156-C163, C166-C168, C176-C185, C187, C196, C198, C230, C232, C266, C267	72
11	CAPACITOR-0.022UF, 50V, X7R_805	SMDCAP805	C254, C255	2
12	CAPACITOR-0.047UF, 50V, X7R_1206	SMDCAP1206	C27-C29	3
13	CAPACITOR-0.1UF, 25V, Y5V_805	SMDCAP805	C45-C48, C53-C58, C61, C63, C65-C74, C83, C86, C92-C95, C98-C105, C110-C119, C122, C125, C127, C155, C173, C174, C189-C195, C197, C199-C208, C213, C214, C217-C220, C223-C229, C231, C233-C242, C246, C248-C251, C256, C257, C264, C265	103

14	CAPACITOR-0.1UF, 50V, X7R_1206	SMDCAP1206	C2-C4, C6, C19, C49, C50, C59, C77, C78, C80-C82, C87, C88, C106, C107, C134, C135, C137, C140, C143, C144, C153, C154, C165, C169-C172, C186	31
15	CAPACITOR-0.22UF, 16V, Y5V_805	SMDCAP805	C7-C10, C252, C253	6
16	CAPACITOR-1000PF, 50V, X7R_805	SMDCAP805	C270, C271	2
17	CAPACITOR-10PF, 50V, NPO_805	SMDCAP805	C258-C260, C262	4
18	CAPACITOR-10UF, 6.3V, TANT TE	SMDTANCAP_A	C1, C43, C44, C51, C52, C75, C76, C84, C85, C89, C90, C96, C97, C120, C121, C123, C124, C126, C175, C188, C209-C212, C215, C216, C221, C222, C243-C245, C247	32
19	CAPACITOR-3PF, 50V, NPO_805	SMDCAP805	C261, C263	2
20	CAPACITOR-68UF, 6.3V, TANT TEH	NEC_D	C17, C18, C20-C22, C91, C128	7
21	CAPACITOR-82PF, 50V, NPO_805	SMDCAP805	C268, C269	2
22	CHIP_RES_NETWORK_8_S MD-10K	RN-EXBA	RN1-RN3	3
23	CY7C276__PLCC_SOCKET -BASE	PLCC44_SOCKET	U15	1
24	DB9_FEMALE-BASE	AMP_745781-4	J5	1
25	DIODEZENER_SMD-4.7V, 1W	DL_41	D2, D3	2
26	DIODEZENER_SMD-6.2V, 1W	DL_41	D1	1
27	FREEDM_8-BASE	SBGA_256	U4	1
28	FUSE__SMD-3A, NANO	NANO_SMF	F1, F2	2
29	HEADER5X2-BASE	HEADER_5X2	J4	1
30	HEADER6-BASE	SIP6	J2	1
31	HEADER_3_JUMPER-BASE	JUMPER3	JP1-JP12	12

32	IDT71256_SOJ-BASE	NONE	U5, U6	2
33	INDUCTOR-4.7UH, , DIGI-KEY DN10472CT-ND	L9-L14	4.7UH	?
34	INDUCTOR-470NH, , PANASONIC	IND-1008	L15, L16	2
35	INDUCTOR-6.8UH, , PANASONIC	IND-1008	L17, L18	2
36	INDUCTOR-FB, 133_100MHZ, FAIR RIA	RES500	L1-L8	8
37	LED-RED, PCB RIGHT ANGLE	LED	D12	1
38	LT1528_SMD-BASE	TO-263	U22, U27	2
39	MAX203_DIP-BASE	DIP20_3	U8	1
40	MC68340-BASE	PQFP144	U29	1
41	MOLEX_8981_4R-BASE	MOLEX_8981_4 R	J14	1
42	MRT_PLCC-BASE	PLCC44	U20, U21, U28, U30, U38, U39, U42, U43	8
43	OSC-TTL, 34.368MHZ, 25PPM, OUT1, OA	OSC14	Y2	1
44	OSC-TTL, 44.736MHZ, 20PPM, OUT1, OA	OSC14	Y1	1
45	OSC-TTL, 6.312MHZ, 25PPM, OUT1, OUA	OSC14	Y3	1
46	OSC_TTL_DIP-25.0000MHZ, 100 PPMA	CRYS14	Y4	1
47	OSC_TTL_DIP-3.6864MHZ, 100 PPM, A	CRYS14	Y5	1
48	PAL22V10_PLCC_SKT-BA SE	PLCC28_SOCKET	U10	1
49	PBNO-BASE	CK_TP11	SW1	1
50	PCI_UNIV_32_CARD_CON N-BASE	PCI_UNIV_32_ EDGE	P1	1
51	PE65968-BASE	RF-TRANS6	T1-T4	4
52	PI5C16212_TSSOP-BASE	TSSOP56	U11-U13, U16	4
53	PWRBLOCK-BASE	CONN04END	J1	1
54	QJET1-BASE	SBGA256_SOCKET	U14, U17	2
55	RESISTOR-1.0K, 5%, 805	SMDRES805	R1, R54, R55, R59, R62, R75-R79, R83, R84, R100-R103, R128-R131	20
56	RESISTOR-100K, 1%,	SMDRES805	R110, R112	2

	805			
57	RESISTOR-10K, 5%, 805	SMDRES805	R9-R11, R23-R27, R46, R47, R60, R61, R88, R89, R133-R149, R158-R161, R182, R183	37
58	RESISTOR-270, 5%, 805	SMDRES805	R6, R87	2
59	RESISTOR-301, 1%, 805	SMDRES805	R122, R123	2
60	RESISTOR-330, 5%, 805	SMDRES805	R13, R14	2
61	RESISTOR-36, 5%, 805	SMDRES805	R67-R74, R92-R99	16
62	RESISTOR-4.7K, 5%, 805	SMDRES805	R3-R5	3
63	RESISTOR-422, 1%, 805	SMDRES805	R118, R119	2
64	RESISTOR-475, 1%, 1206	SMDRES1206	R57, R58, R65, R66, R81, R82, R90, R91	8
65	RESISTOR-5.23K, 1%, 805	SMDRES805	R116, R117	2
66	RESISTOR-6.04K, 1%, 805	SMDRES805	R111, R113	2
67	RESISTOR-604, 1%, 805	SMDRES805	R120, R121	2
68	RESISTOR-6K81, 1%, 805	SMDRES805	R114, R115	2
69	RESISTOR-75, 5%, 805	SMDRES805	R2, R7, R8, R12, R15-R22, R28-R45, R48-R53, R56, R63, R64, R80, R85, R86, R104-R109, R132, R150-R157, R162-R181	77
70	RESISTOR-75.0, 1%, 805	SMDRES805	R124-R127	4
71	RES_ARRAY_15_SMD-10K	SOIC16	RN27, RN28	2
72	RES_ARRAY_8_SMD-10K	SOIC16	RN29	1
73	TST_PT-BASE	TST_PT_1	TP2-TP5, TP13, TP28, TP48, TP52, TP53, TP57	10
74	WB1010-BASE	DIP6_3	U18, U19, U23, U26, U32-U37, U40, U41, U45-U48	16
75	XC95108_PQ100	PQFP100	U9	1

9 SCHEMATICS

REVISIONS				
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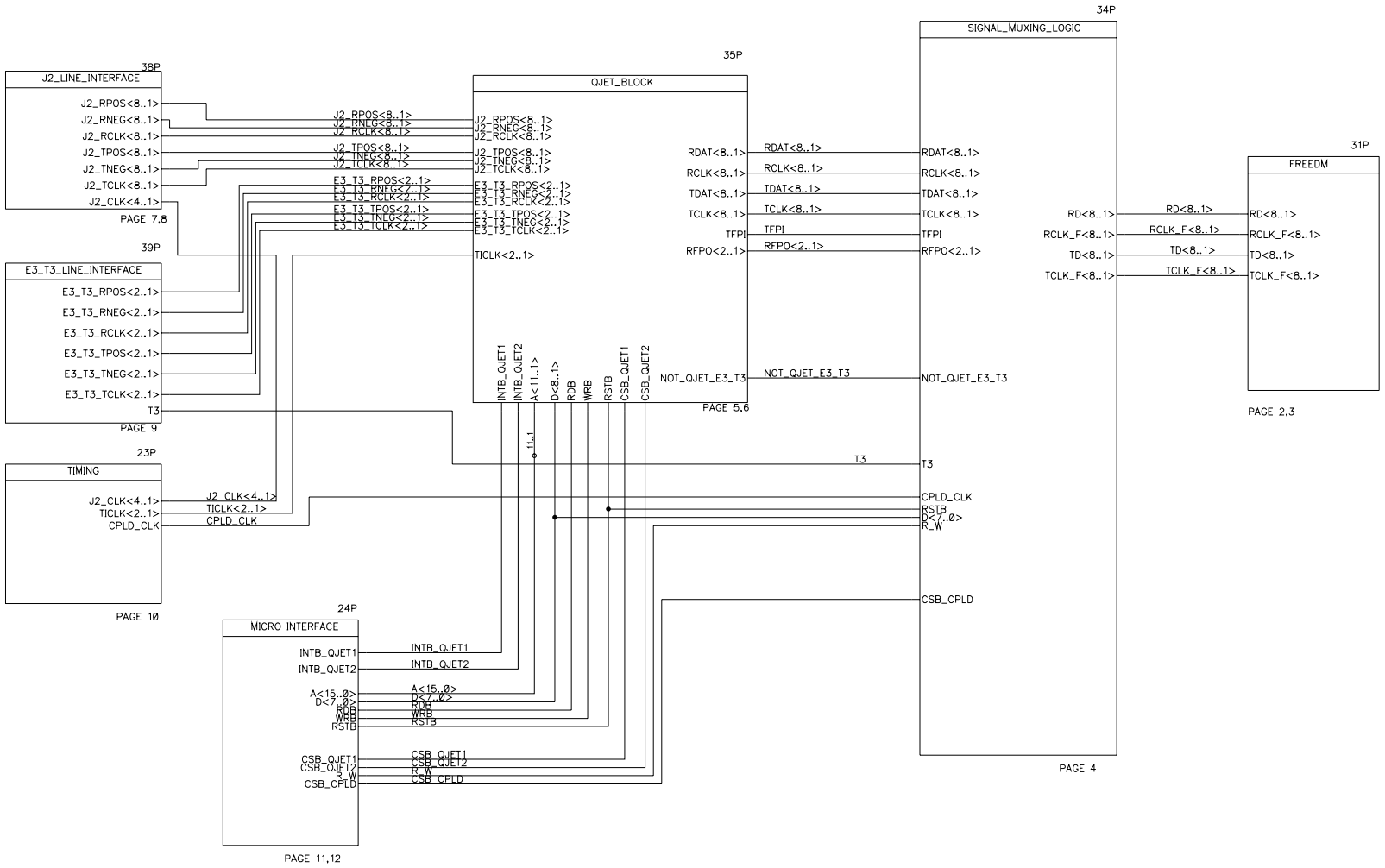

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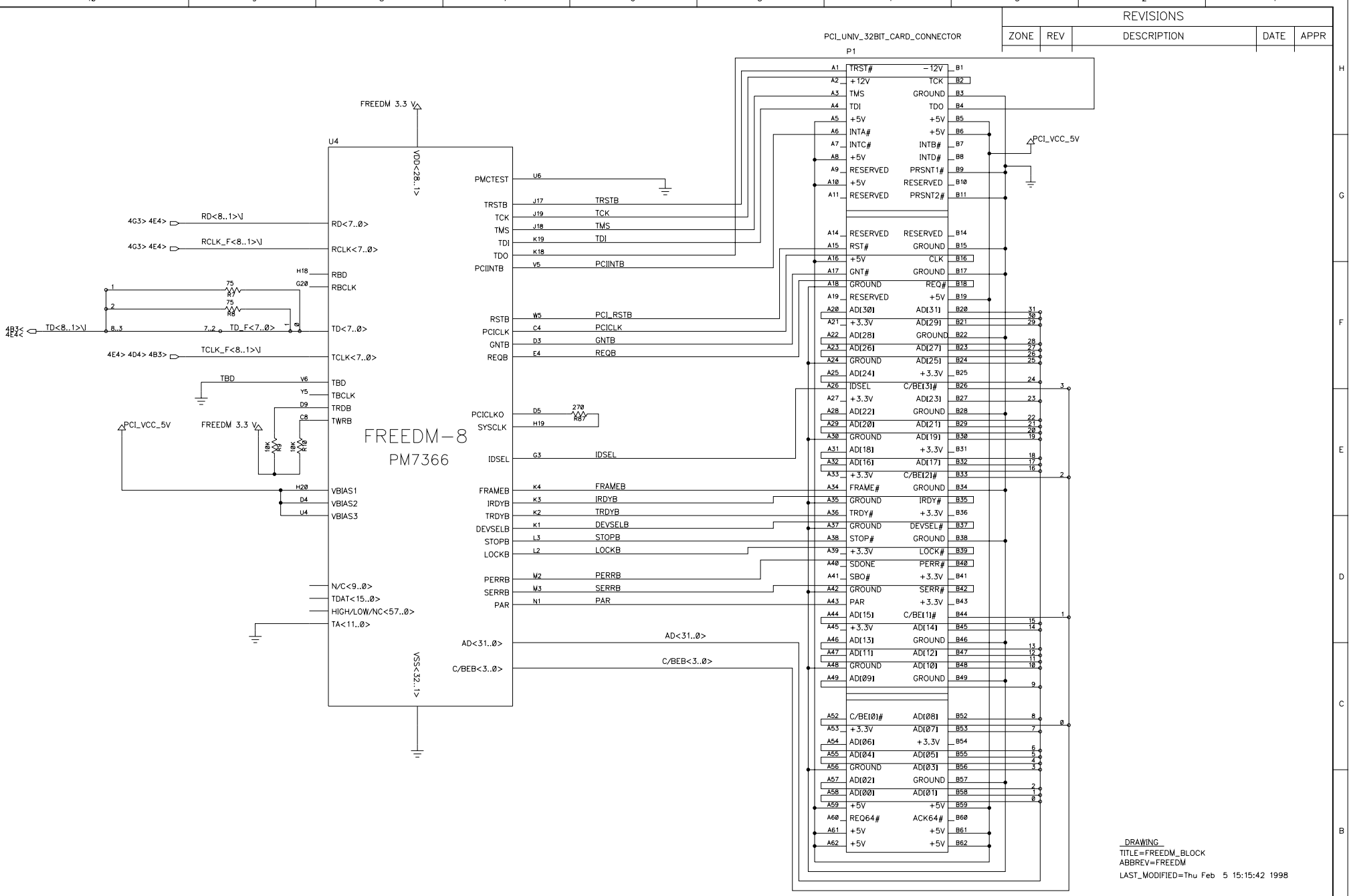
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-971060 *PRELIMINARY*	ISSUE: 1.1
TITLE: QJET WITH FREEDM REFERENCE DESIGN ROOT DRAWING	DATE: FEB. 3, 97
ENGINEER: ERIC SOO	PAGE: 1 OF 12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P1
U4
FREEDM-8
PM7366
FREEDM 3.3 V
PCI_VCC_5V
VDD<28..1>
VSS<32..1>
PMCTEST
TRSTB
TCK
TMS
TDI
TDO
PCIINTB
RSTB
PCICLK
GNTB
REQB
PCICLKO
SYSCLK
IDSEL
FRAMEB
IRDYB
TRDYB
DEVSELB
STOPB
LOCKB
PERRB
SERRB
PAR
AD<31..0>
C/BEB<3..0>
RD<8..1>\I
RD<7..0>
RCLK_F<8..1>\I
RCLK<7..0>
RBD
RBCLK
TD<8..1>\I
TD_F<7..0>
TD<7..0>
TCLK_F<8..1>\I
TCLK<7..0>
TBD
TBCLK
TRDB
TWRB
VBIAS1
VBIAS2
VBIAS3
N/C<9..0>
TDAT<15..0>
HIGH/LOW/NC<57..0>
TA<11..0>
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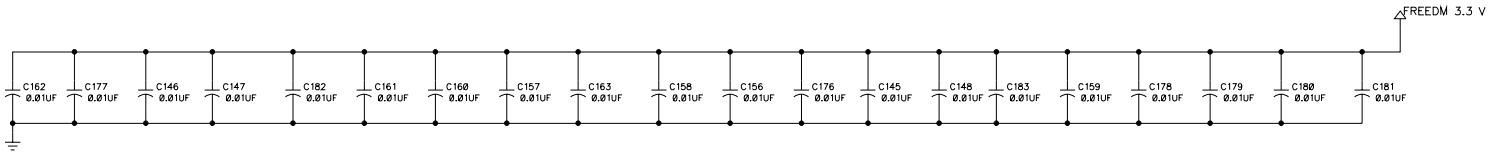
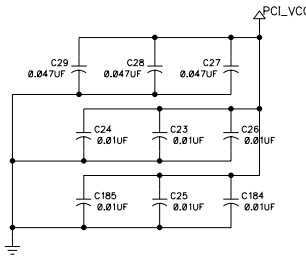
ABBREV=FREEDM
LAST_MODIFIED=Thu Feb 5 15:15:42 1998
NOTE
CHECK THE LATEST PCI SPEC FOR
COMPONENT AND LAYOUT RESTRICTIONS
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-971060 *PRELIMINARY*
ISSUE: 1.1
TITLE: QJET WITH FREEDM REFERENCE DESIGN FREEDM & PCI CONNECTOR
DATE: 97/11/18
ENGINEER: ERIC SOO
PAGE: 2 OF 12

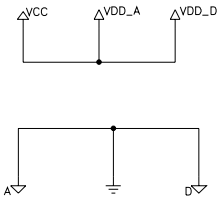
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DECOUPLING CAPS FOR FREEDM VDD

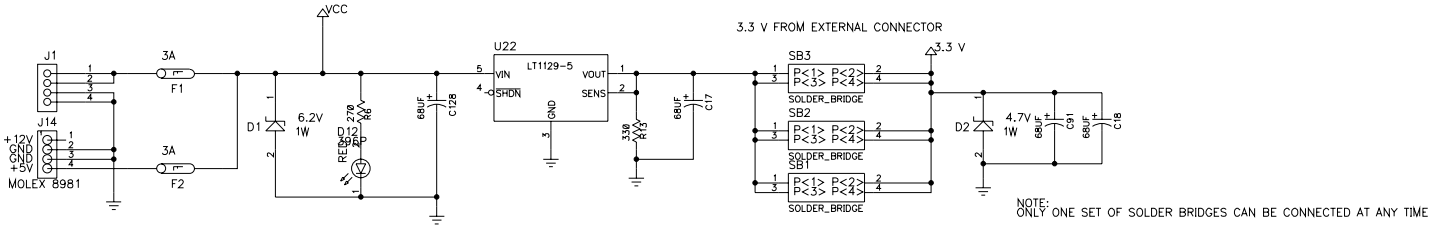




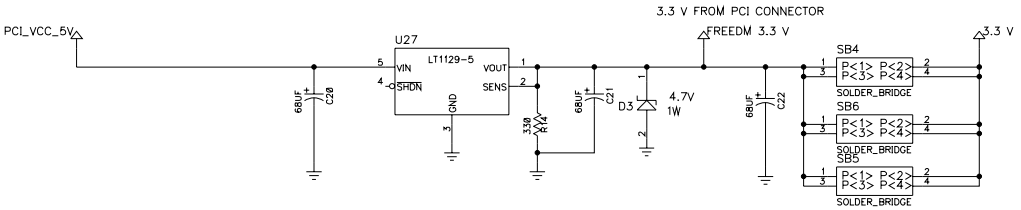
NOTE:
THE FOLLOWING DECOUPLING CAPS ARE USED FOR PCI BUS POWER RAIL. THEY SHOULD BE PLACED IN SUCH A WAY THAT AT LEAST AN AVERAGE OF Ø.Ø1UF PER VCC PIN IS ACHIEVED.

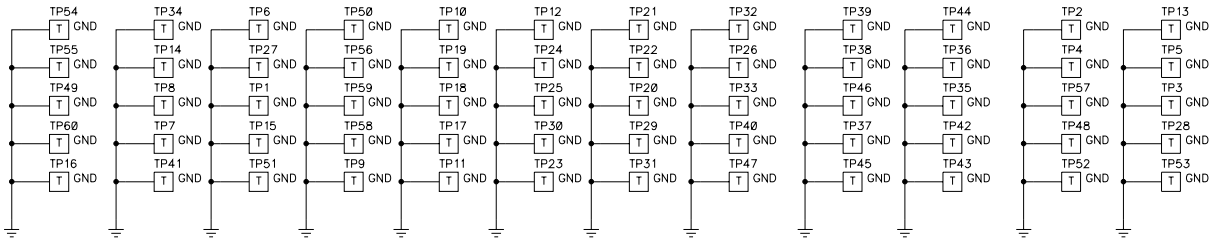


SINGLE GROUND PLANE USED



NOTE:
ONLY ONE SET OF SOLDER BRIDGES CAN BE CONNECTED AT ANY TIME





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PMC-Sierra, Inc.

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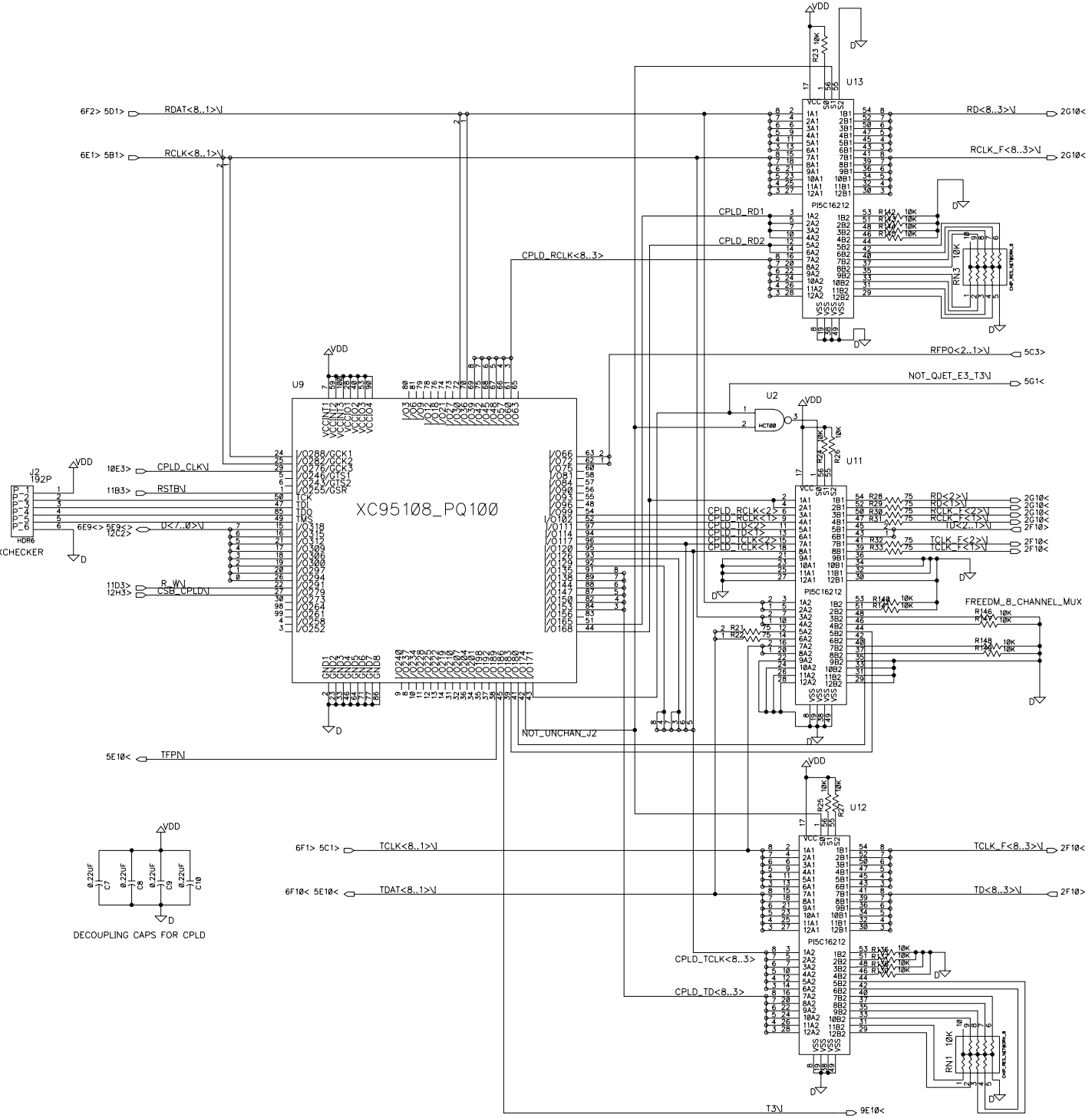
TITLE: QUET WITH FREEDM REFERENCE DESIGN POWER AND DECOUPLING CAPS	DATE: 97/11/18
ENGINEER: ERIC SOO	PAGE: 3 OF 12

SIGNAL_MUXING_LOGIC

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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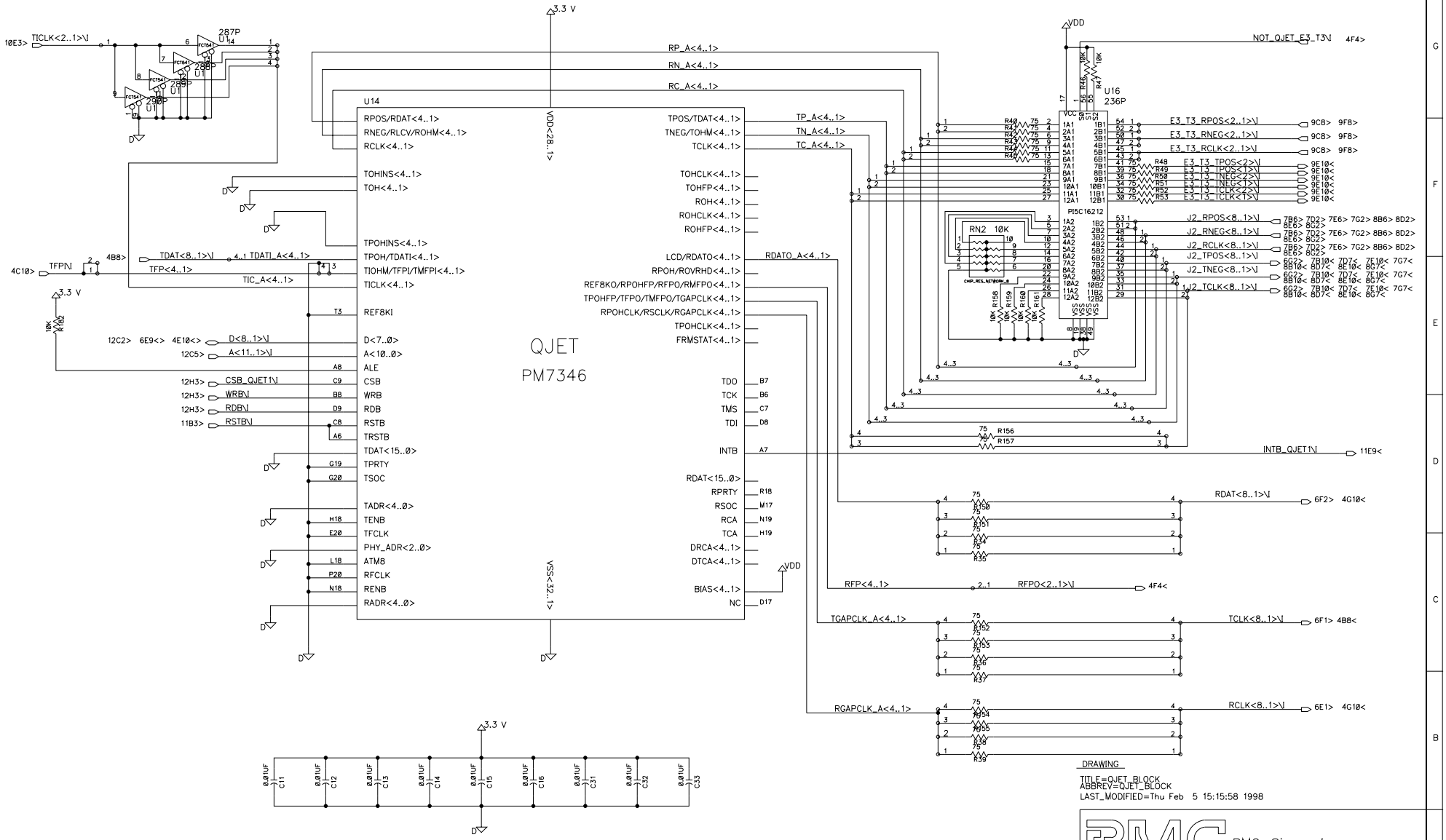
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-971060	ISSUE: 1.1
TITLE: QJET WITH FREEDM REFERENCE DESIGN SIGNAL_MUXING_LOGIC	DATE: 97/11/18
ENGINEER: ERIC SOO	PAGE: 4 OF 12


REVISIONS
ZONE REV DESCRIPTION DATE APPR
QJET
PM7346
U14
RPOS/RDAT<4..1>
RNEG/RLCV/ROHM<4..1>
RCLK<4..1>
TOHINS<4..1>
TOH<4..1>
TPOHINS<4..1>
TPOH/TDATI<4..1>
TIOHM/TFPI/TMFPI<4..1>
TICLK<4..1>
REF8KI
D<7..0>
A<10..0>
ALE
CSB
WRB
RDB
RSTB
TRSTB
TDAT<15..0>
TPRTY
TSOC
TADR<4..0>
TENB
TFCLK
PHY_ADR<2..0>
ATMB
RFCLK
RENB
RADR<4..0>
TPOS/TDAT<4..1>
TNEG/TOHM<4..1>
TCLK<4..1>
TOHCLK<4..1>
TOHFP<4..1>
ROH<4..1>
ROHCLK<4..1>
ROHFP<4..1>
LCD/RDATO<4..1>
RPOH/ROVRHD<4..1>
REF8KO/RPOHFP/RFPO/RMFPO<4..1>
TPOHFP/TFPO/TMFPO/TGAPCLK<4..1>
RPOHCLK/RSCLK/RGAPCLK<4..1>
TPOHCLK<4..1>
FRMSTAT<4..1>
RDAT<15..0>
RPRTY
RSOC
RCA
TCA
DRCA<4..1>
DTCA<4..1>
BIAS<4..1>
NC
TDO
TCK
TMS
TDI
INTB
VDD<28..1>
VSS<32..1>
3.3 V
VDD
RP_A<4..1>
RN_A<4..1>
RC_A<4..1>
TP_A<4..1>
TN_A<4..1>
TC_A<4..1>
RDATO_A<4..1>
TICLK<2..1>\I
TFPI\I
TDAT<8..1>\I
TIC_A<4..1>
CSB_QJET1\I
WRB\I
RDB\I
RSTB\I
D<8..1>\I
A<11..1>\I
INTB_QJET1\I
NOT_QJET_E3_T3\I
E3_T3_RPOS<2..1>\I
E3_T3_RNEG<2..1>\I
E3_T3_RCLK<2..1>\I
E3_T3_TPOS<2>\I
E3_T3_TNEG<2>\I
E3_T3_TCLK<2>\I
E3_T3_TPOS<1>\I
E3_T3_TNEG<1>\I
E3_T3_TCLK<1>\I
J2_RPOS<8..1>\I
J2_RNEG<8..1>\I
J2_RCLK<8..1>\I
J2_TPOS<8..1>\I
J2_TNEG<8..1>\I
J2_TCLK<8..1>\I
RDAT<8..1>\I
RFP<4..1>
RFPO<2..1>\I
TGAPCLK_A<4..1>
TCLK<8..1>\I
RGAPCLK_A<4..1>
RCLK<8..1>\I
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236P
PI5C16212
RN2 10K
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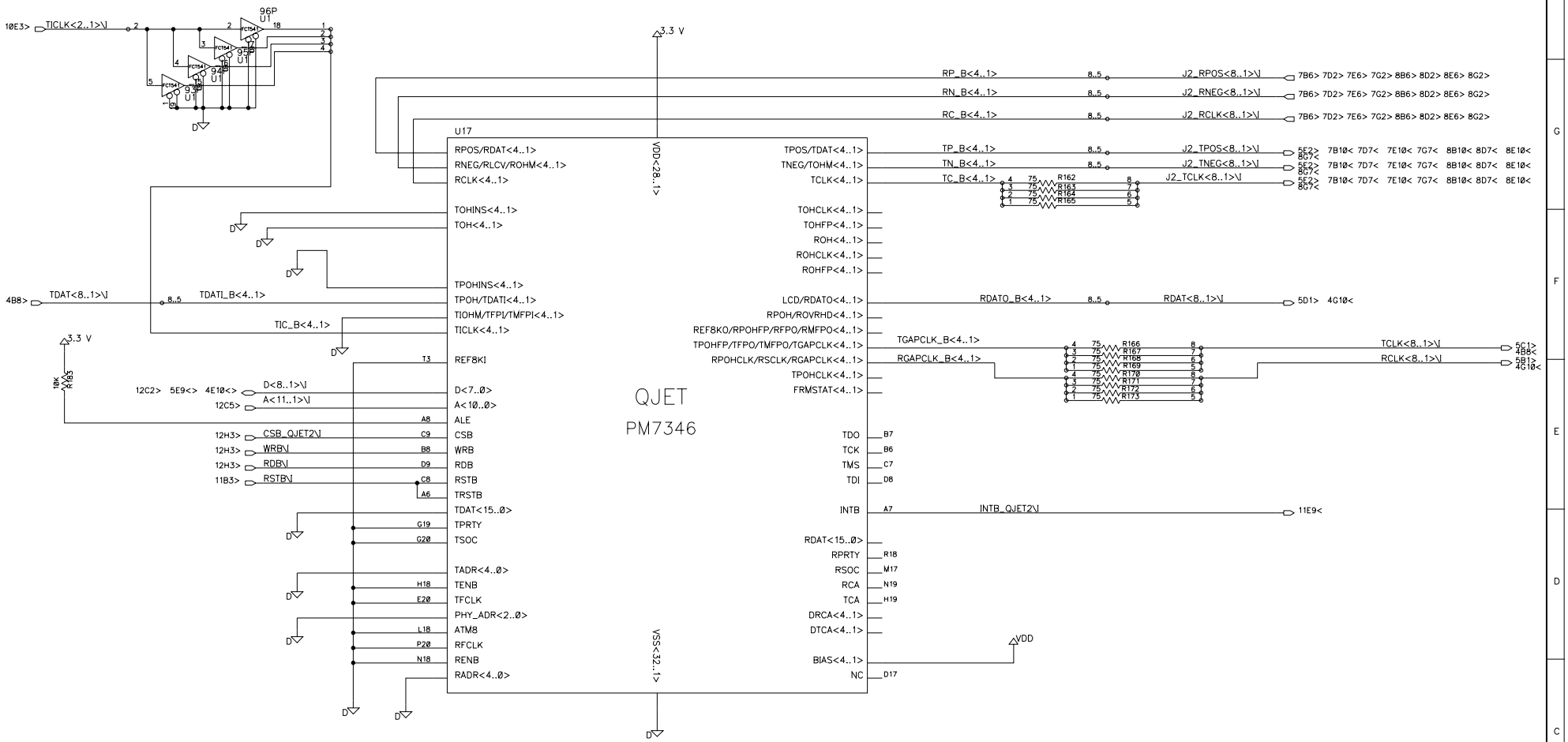
LAST_MODIFIED=Thu Feb 5 15:15:58 1998
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-970240
ISSUE: 1.1
TITLE: QJET WITH FREEDM REFERENCE DESIGN QJET BLOCK
DATE: 97/11/18
ENGINEER: ERIC SOO
PAGE: 5 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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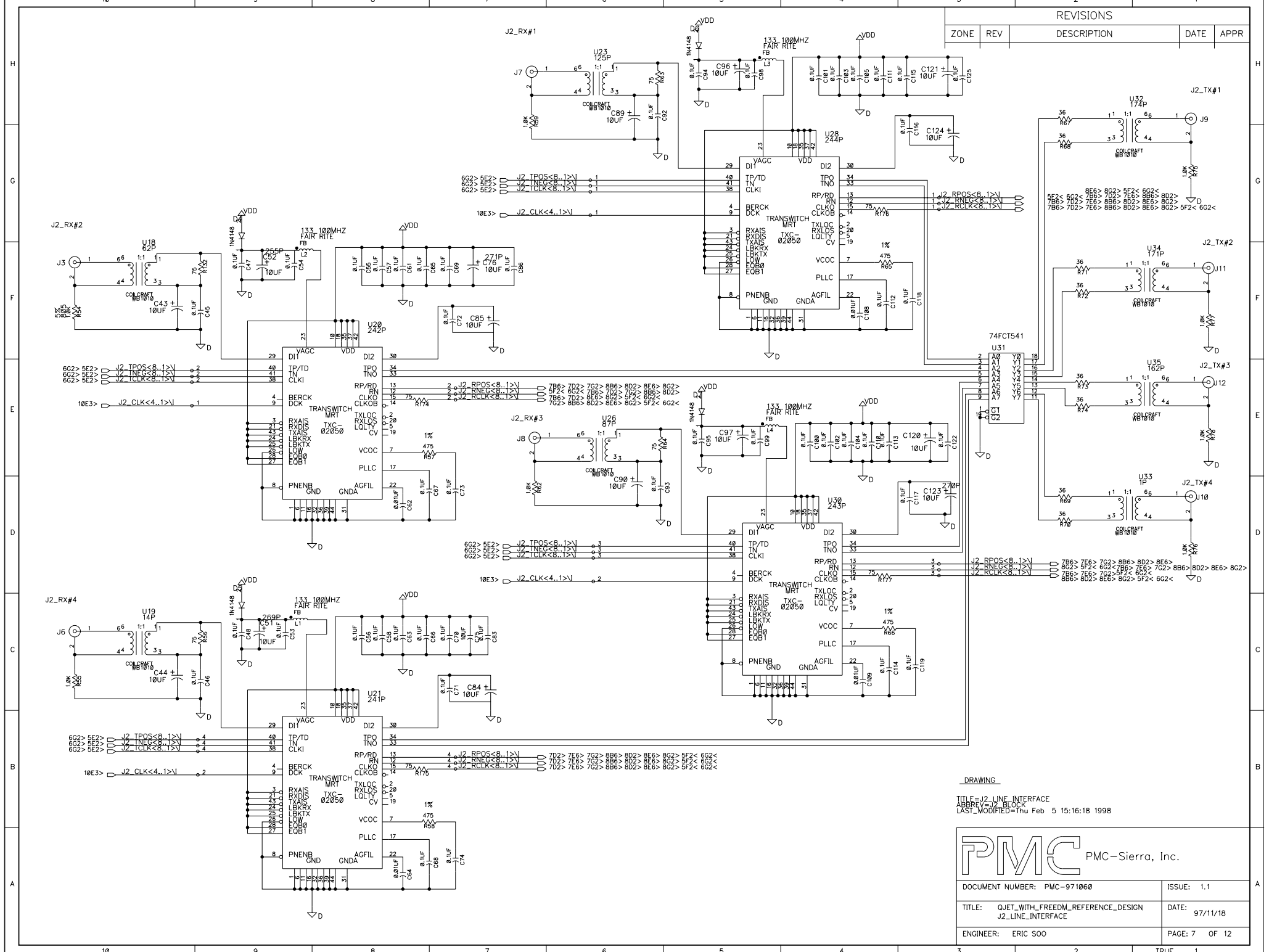
LAST_MODIFIED=Thu Feb 5 15:16:11 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-970240	ISSUE: 1.1
TITLE: QJET WITH FREEDOM REFERENCE DESIGN QJET BLOCK	DATE: 97/11/18
ENGINEER: ERIC SOO	PAGE: 6 OF 12


REVISIONS
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J2_RX#1
J2_RX#2
J2_RX#3
J2_RX#4
J2_TX#1
J2_TX#2
J2_TX#3
J2_TX#4
U20 242P
U21 241P
U30 243P
U28 244P
74FCT541
U31
TRANSWITCH MRT TXC-02050
133.100MHZ FAIR RITE FB
J2_TPOS<8..1>\|
J2_TNEG<8..1>\|
J2_TCLK<8..1>\|
J2_CLK<4..1>\|
J2_RPOS<8..1>\|
J2_RNEG<8..1>\|
J2_RCLK<8..1>\|
DRAWING
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PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-971060
ISSUE: 1.1
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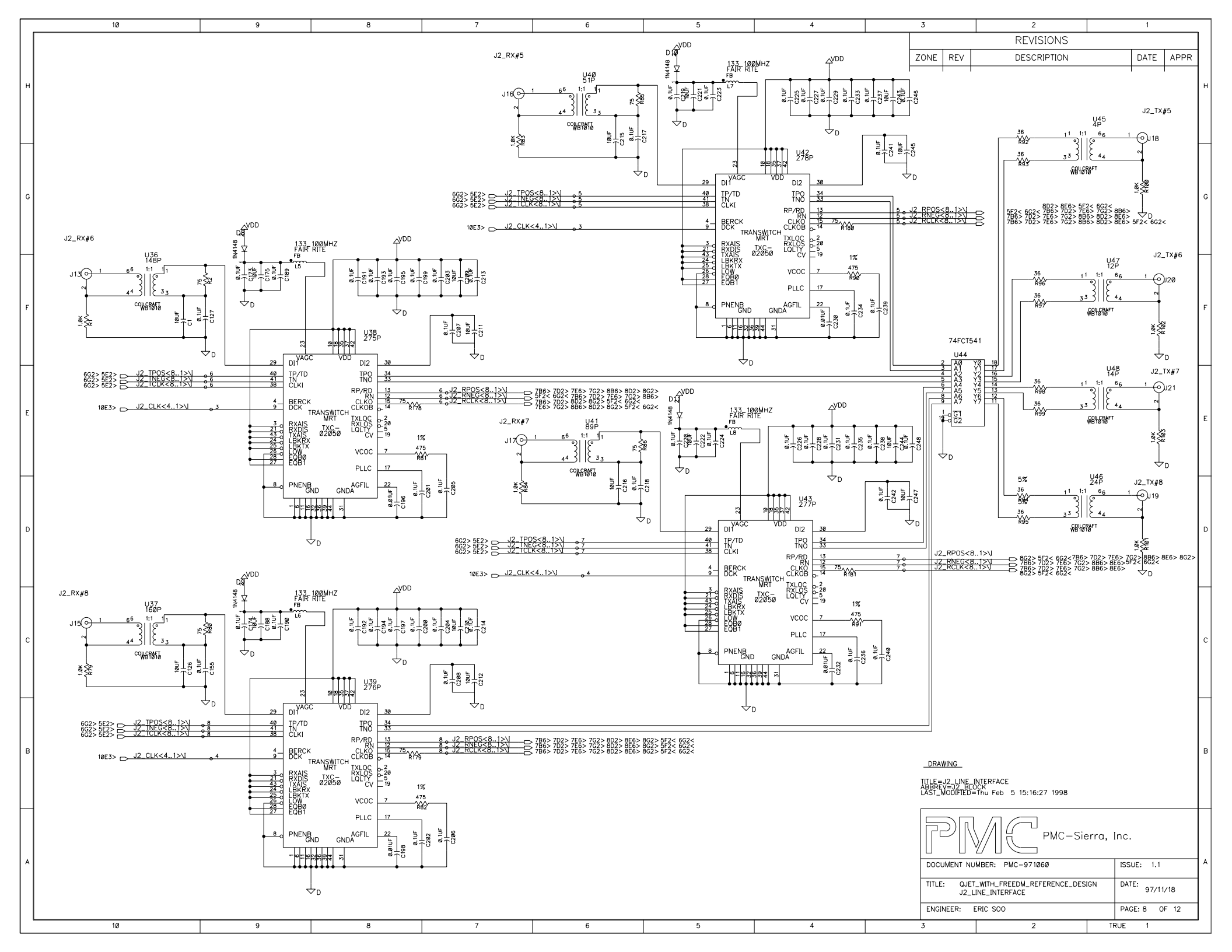
DATE: 97/11/18
ENGINEER: ERIC SOO
PAGE: 7 OF 12


REVISIONS
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J2_RX#5
J2_RX#6
J2_RX#7
J2_RX#8
J2_TX#5
J2_TX#6
J2_TX#7
J2_TX#8
74FCT541
TRANSWITCH TXC-02050
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PMC-Sierra, Inc.
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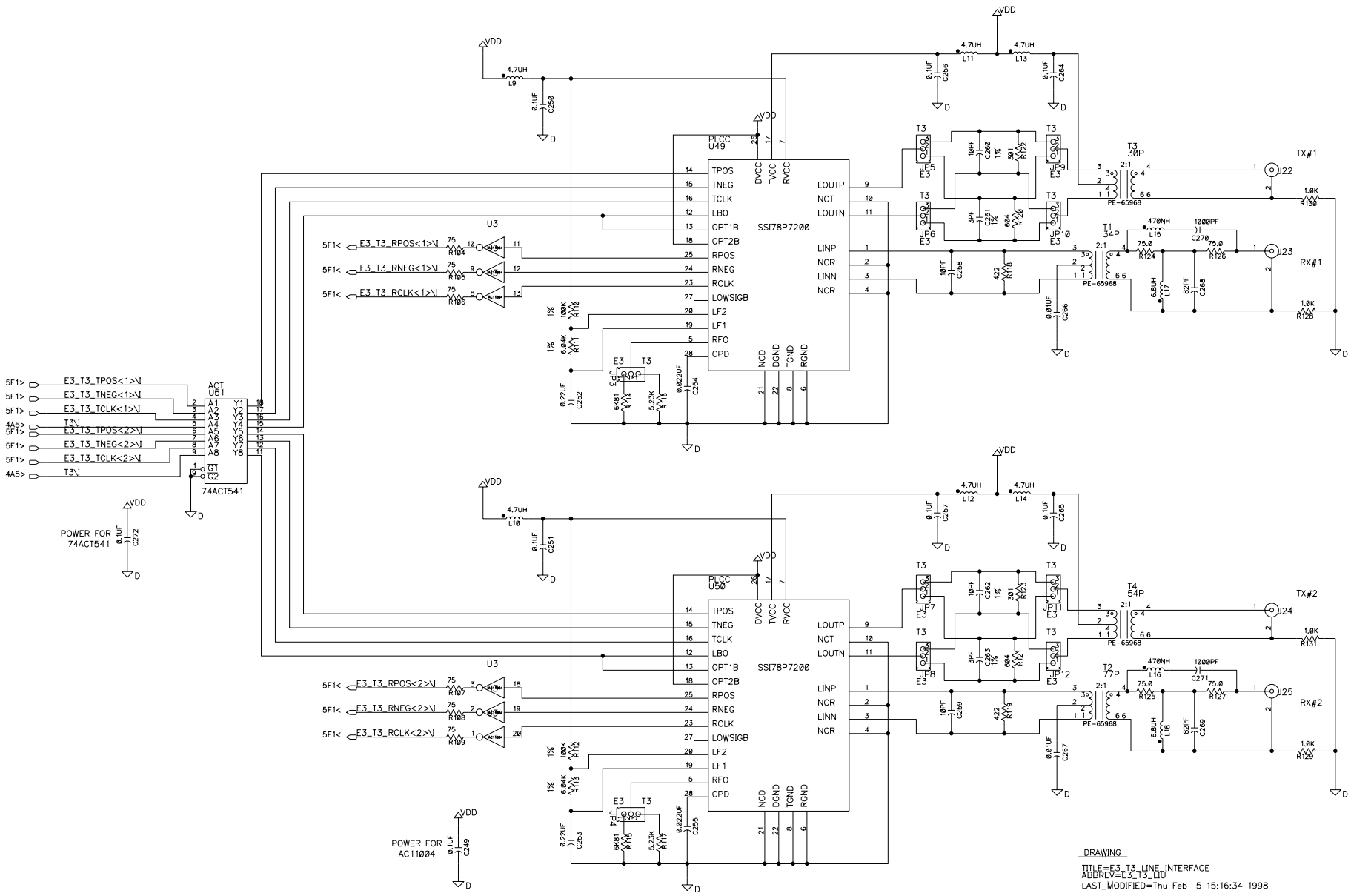
ISSUE: 1.1
TITLE: QJET_WITH_FREEDM_REFERENCE_DESIGN J2_LINE_INTERFACE
DATE: 97/11/18
ENGINEER: ERIC SOO
PAGE: 8 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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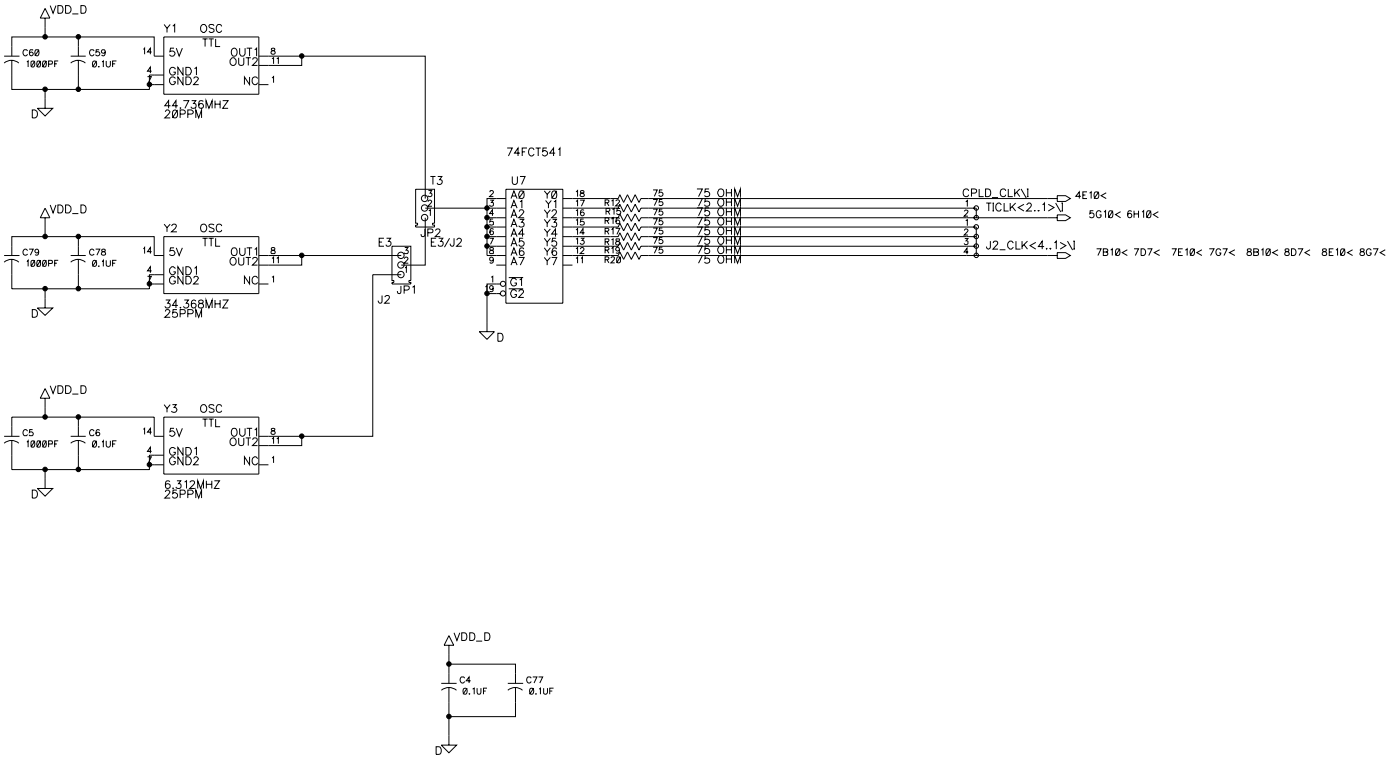
LAST_MODIFIED=Thu Feb 5 15:16:34 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-971060	ISSUE: 1.1
TITLE: QJET WITH FREEDM REFERENCE DESIGN E3_T3_LINE_INTERFACE	DATE: 97/11/18
ENGINEER: ERIC SOO	PAGE: 9 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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PMC-Sierra, Inc.

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TITLE: QJET WITH FREEDM REFERENCE DESIGN TIMING	DATE: 97/11/18
ENGINEER: ERIC SOO	PAGE: 10 OF 12

MICROPROCESSOR CIRCUIT

REVISIONS				
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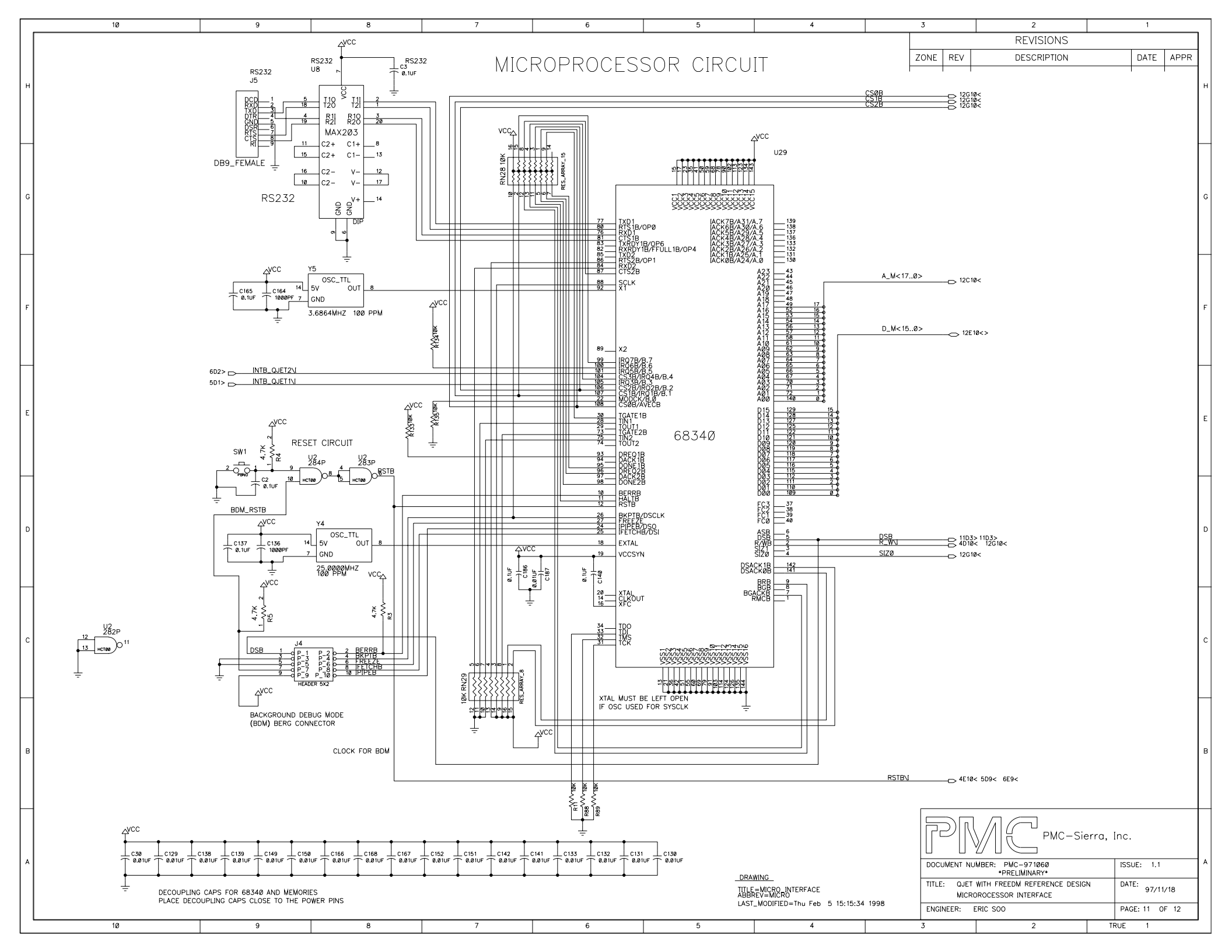

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-971060 *PRELIMINARY*	ISSUE: 1.1
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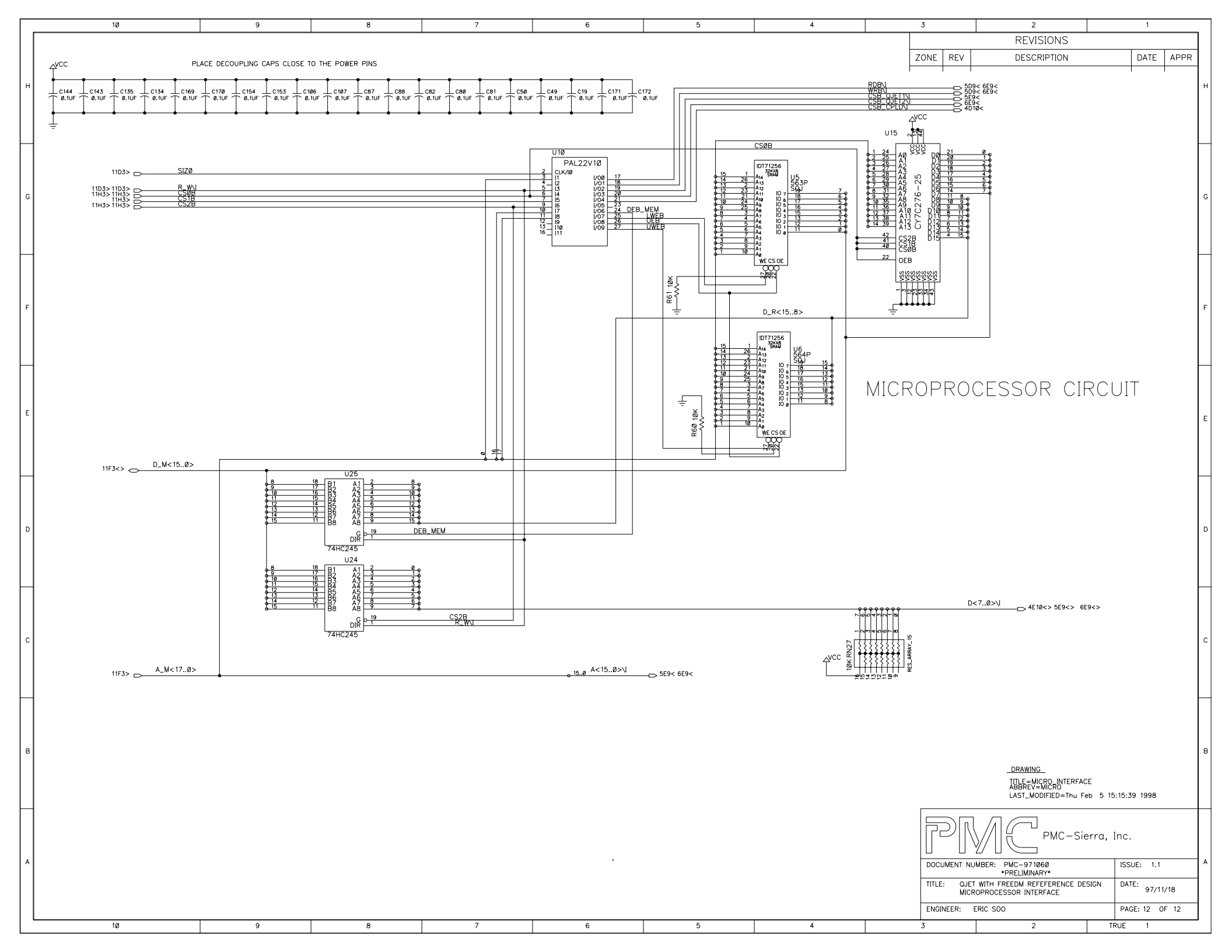
ENGINEER: ERIC SOO	PAGE: 11 OF 12


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
PLACE DECOUPLING CAPS CLOSE TO THE POWER PINS
VCC
C144 Ø.1UF
C143 Ø.1UF
C135 Ø.1UF
C134 Ø.1UF
C169 Ø.1UF
C170 Ø.1UF
C154 Ø.1UF
C153 Ø.1UF
C106 Ø.1UF
C107 Ø.1UF
C87 Ø.1UF
C88 Ø.1UF
C82 Ø.1UF
C80 Ø.1UF
C81 Ø.1UF
C50 Ø.1UF
C49 Ø.1UF
C19 Ø.1UF
C171 Ø.1UF
C172 Ø.1UF
RDB\
WRB\
CSB_QJET1\
CSB_QJET2\
CSB_CPLD\
5D9< 6E9<
5D9< 6E9<
5E9<
6E9<
4D10<
U15
CY7C276-25
CS2B
CS1B
CS0B
OEB
U10
PAL22V10
CLK/I0
SIZØ
R_W\
CS0B
CS1B
CS2B
11D3>
11H3>
DEB_MEM
LWEB
OEB
UWEB
U5
563P
IDT71256
32KX8
SRAM
WE CS OE
R61 10K
D_R<15..8>
U6
564P
R60 10K
MICROPROCESSOR CIRCUIT
11F3<>
D_M<15..Ø>
U25
74HC245
DIR
DEB_MEM
U24
CS2B
R_W\
D<7..Ø>\
4E10<> 5E9<> 6E9<>
VCC
10K RN27
RES_ARRAY_15
11F3>
A_M<17..Ø>
15..Ø A<15..Ø>\
5E9< 6E9<
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LAST_MODIFIED=Thu Feb 5 15:15:39 1998
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-971060 *PRELIMINARY*
ISSUE: 1.1
TITLE: QJET WITH FREEDM REFEFERENCE DESIGN MICROPROCESSOR INTERFACE
DATE: 97/11/18
ENGINEER: ERIC SOO
PAGE: 12 OF 12

10 DISCLAIMER

The reference design presented in this document is correct to the best of our knowledge. The CPLD logic has been simulated on a workstation and a separate reference design, documented in PMC-980182, 'S/UNI-QJET Reference Design', will be built and will verify most of the circuitry associated with the S/UNI-QJET presented in this design. However, this design has not been built.

APPENDIX A: CPLD DESIGN AND TESTING

The CPLD design was entered using Xilinx's Foundation Series software via schematic capture. To ensure compatibility with the intended board layout, output pads of the design were designated to be fitted to particular pins according to the intended board design (see 9. SCHEMATICS). Timing constraints were then used to ensure an acceptable level of performance is achieved after the fitting process. Post fit timing simulation was then run to obtain the best possible estimate of the CPLD's performance.

All tests were performed using the Foundation interactive simulator. The following table lists features of the CPLD tested and the corresponding results.

Table 2 CPLD Feature Test

Test Description	Result
Verify Read and Write access to internal register	Correct
Verify NOT_E3_T3, NOT_UNCHAN_J2, and T3 signals set according to internal register (see 5.4 Sheet 4: Signal Multiplexing Logic for more details)	Correct
Verify that TCLK[x], and RCLK[x] are kept idle when channelized J2 is not the current operating mode	Correct
Verify TFPI repetition period to be 789 clock cycles	Correct
Verify TCLK[x] start and stop times relative to TFPI output	Correct
Verify TD[x] to TDATI[x] multiplexing operation	Correct
Verify RCLK[x] start and stop times relative to RFPO input	Correct
Verify RSTB reset functionality	Correct
Check propagation delay from RSCLK[x] to RCLK[x]	25 ns
Check propagation delay from RDATO[x] to RD[x]	20 ns
Check propagation delay from TICLK to TCLK[x]	25 ns
Check propagation delay from TICLK to TDATI[x]	10 ns

NOTES

CONTACTING PMC-SIERRA, INC.

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