Eight Link Circuit Emulation Service on a Chip

FEATURES

- Performs AAL1 Segmentation And Reassembly (SAR) function on either eight T1/E1 links or a single DS3/E3 link.
- Supports 256 Virtual Channels (VCs).
- Adheres to the ATM Forum's Circuit Emulation Service (CES) 2.0 (af-vtoa-0078.000) specification and ITU-T Recommendation I363.1 for AAL1.
- Supports both structured and unstructured data formats selectable on a per-link basis.
- Supports both T1 and E1 lines selectable on a per-link basis.
- Supports $n \times 64$ structured data format with Common Channel Signaling (CCS) and Channel Associated Signaling (CAS) configuration options.
- Supports arbitrary timeslot-to-VC mappings, including alternating timeslots.
- Provides per-VC data and signalling conditioning in both the transmit and the receive directions.
- Arbitrates a 16-bit microprocessor interface to two 128K $\times$ 8 (12 ns) SRAMs.
- Supports multicast connections, ATM Monitoring (AMON), Remote Monitoring (RMON), and ATM Circuit Steering (ACS).
- Supports a glueless interface to the PM4344 TQUAD, PM6344 EQUAD, and PM4351 COMET T1/E1 interface devices.
- Supports counters as required by ATM Forum CES 2.0 MIB.
- Pin-compatible with the WAC-021-X.
- Built-in T1/E1 transmit line clock generation based on received Synchronous Residual Time Stamp (SRTS) values, the received line clock, or a nominal frequency.

TRANSMIT CELL INTERFACE FEATURES

- Provides an ATM-layer or PHY-layer 33 MHz UTOPIA Level 2 interface. Both Single PHY (SPHY) and Multi-PHY (MPHY) modes are supported.
- Provides per-VC transmit queueing with individual partially filled cell length settings.
- Supports a calendar queue service algorithm that produces minimal Cell Delay Variation (CDV).
- Generates and transmits SRTS values for unstructured modes.
- Provides a supervisory transmit buffer for Operations, Administration, and Maintenance (OAM) cells, and for ATM signalling.

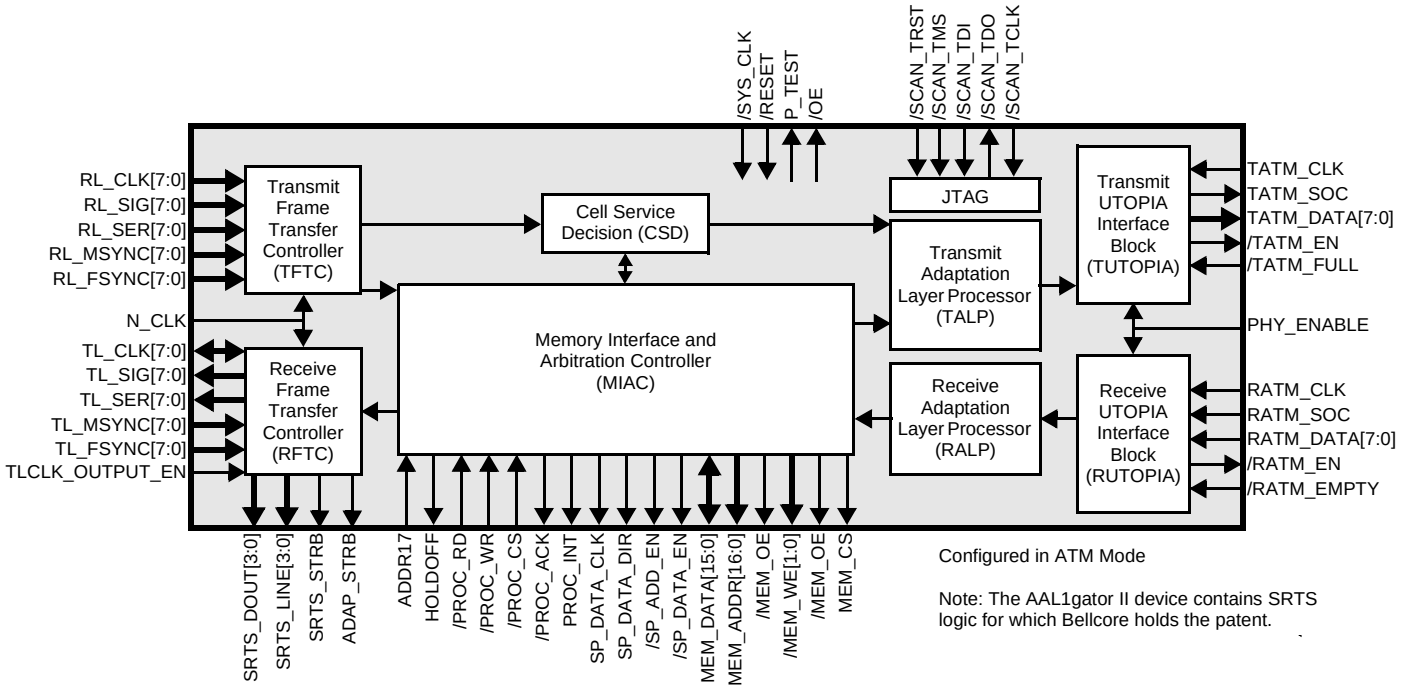
RECEIVE CELL INTERFACE

- Provides an ATM-layer or PHY-layer 33 MHz UTOPIA Level 2 interface. Both SPHY and MPHY modes are supported.
- Provides per-VC queues with individual CDV tolerance settings and partially filled cell length settings.
- Provides per-VC partially filled cell length settings.
- Provides a multiplexed interface to external receive Phase-Locked Loops (PLLs) for SRTS clock recovery for unstructured modes or adaptive clock recovery.
- Provides a supervisory receive queue and processor interrupts for OAM cell receptions.
- Provides sequence number processing in accordance with the "Fast SN Algorithm" as specified in the ITU-T Recommendation I.363.1.

APPLICATIONS

- ATM Multiservice Switches
- ATM Access Concentrators or Multiplexers
- Digital Access Cross-Connects
- Multiservice Access Devices

BLOCK DIAGRAM



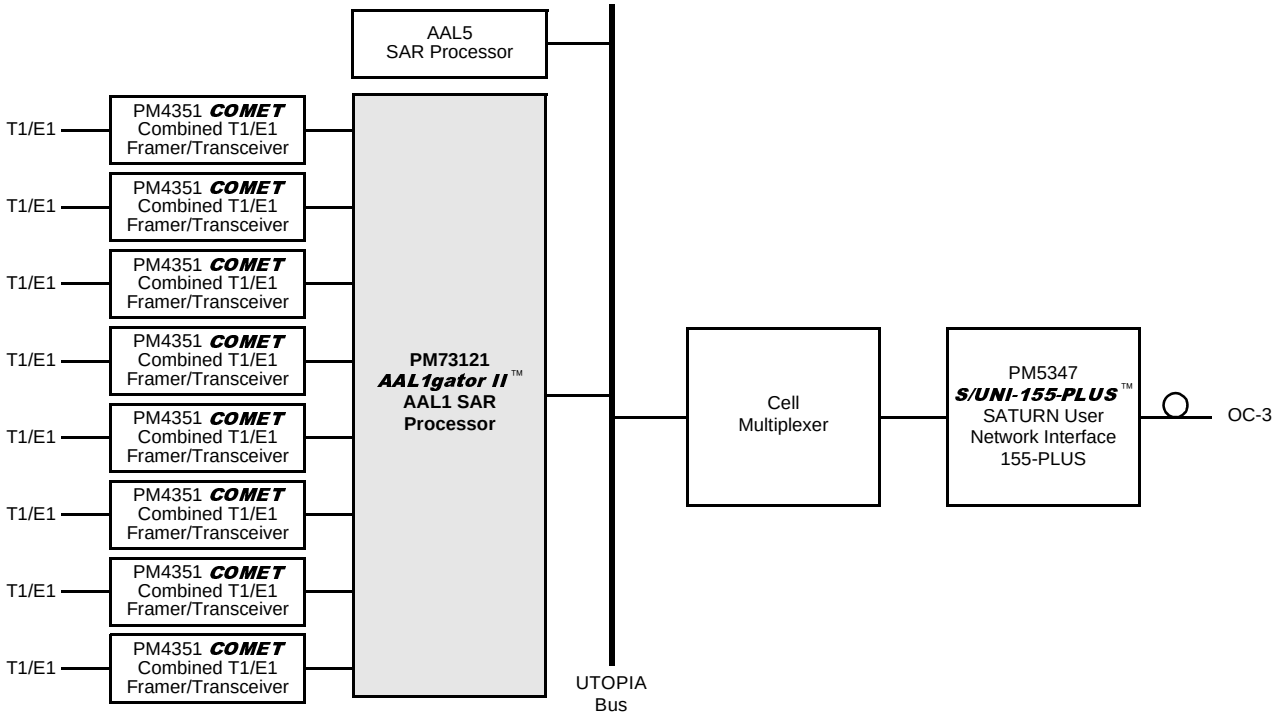
Configured in ATM Mode

Note: The AAL1gator II device contains SRTS logic for which Bellcore holds the patent.

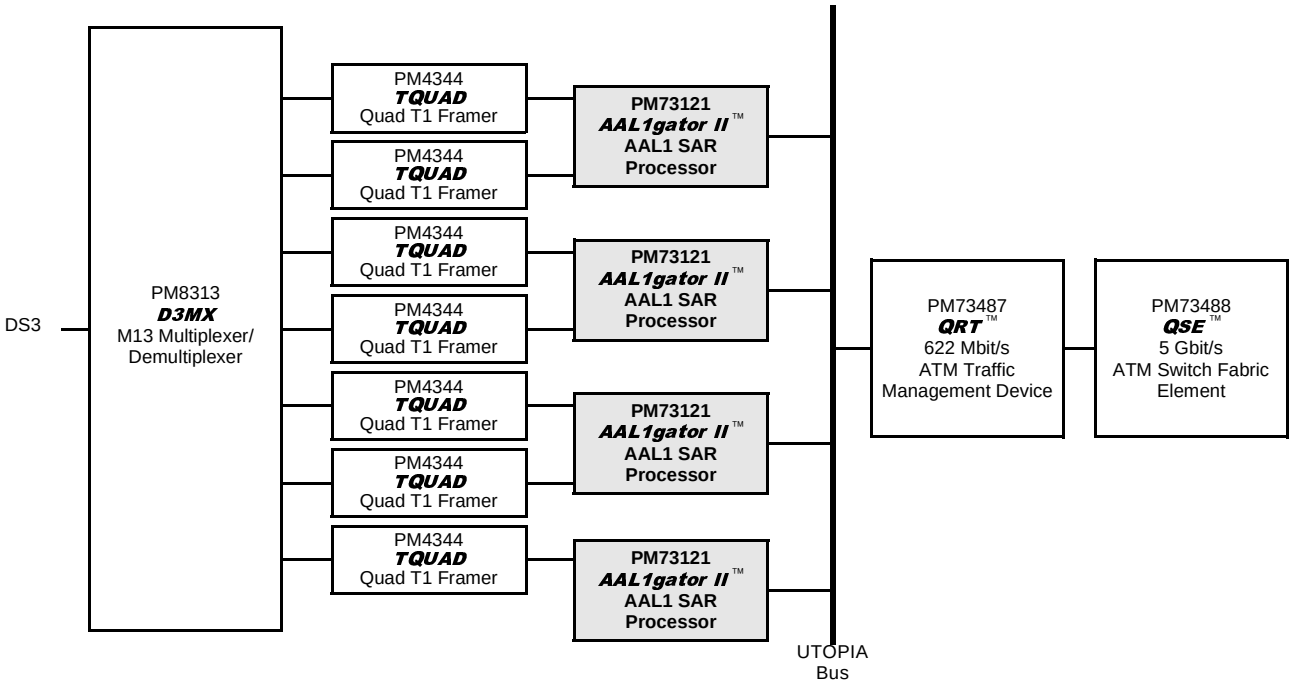
Eight Link Circuit Emulation Service on a Chip

TYPICAL APPLICATIONS

EIGHT LINK T1/E1 CIRCUIT EMULATION APPLICATION



CHANNELIZED DS3 PORT CARD FOR MULTISERVICE ATM SWITCH



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation,
send email to:
document@pmc-sierra.com
or contact the head office,
Attn: Document Coordinator

All product documentation is available
on our web site at:
http://www.pmc-sierra.com
For corporate information,
send email to:
info@pmc-sierra.com

PMC-980621 (P2)

September, 1998