PM5349

S/UNI-® 155-QUAD

S/UNI-QUAD

SATURN USER NETWORK INTERFACE (155-QUAD)

ERRATA

PRELIMINARY

ISSUE 3: JUNE 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
3	June 1999	This document contains errata information corresponding to the issue 5 data sheet and device revision E.
2	Jan 1999	This document contains errata information corresponding to the issue 5 data sheet and device revision C.
1	Nov 1998	This document contains errata information corresponding to the issue 4 data sheet and device revision C.

CONTENTS

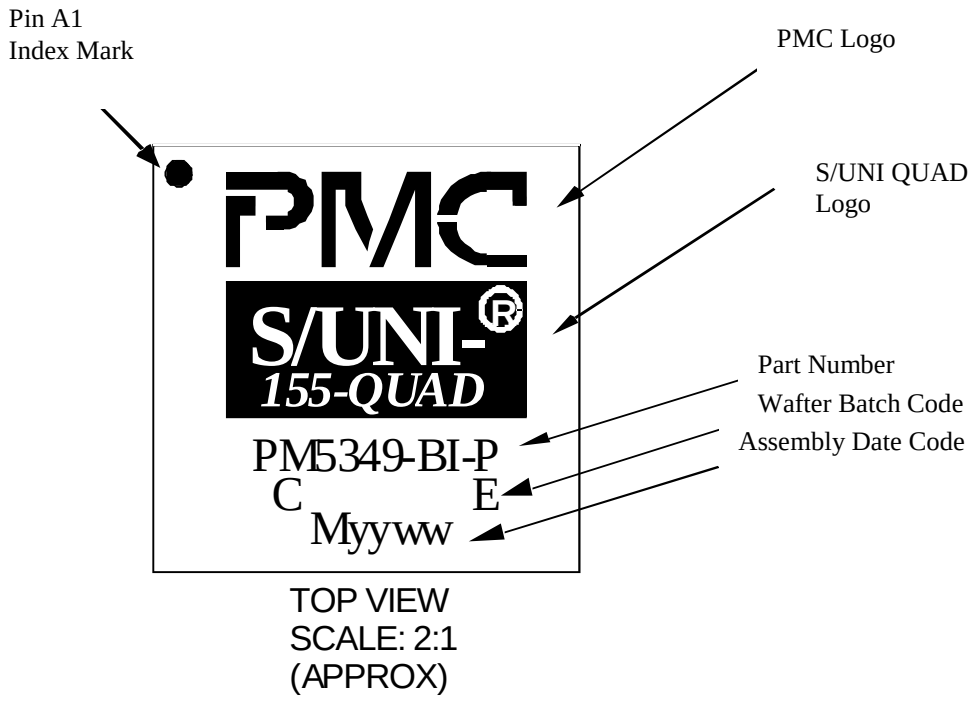
1 ISSUE 3 ERRATA

This issue 3 contains errata applied to the PMC-971239 S/UNI-QUAD Issue 5 datasheet. The issue 5 datasheet and issue 3 errata supersede all prior editions and versions

1.1 Device Identification

The information contains in this document applies to the PM5349 S/UNI-QUAD revision E device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5349 S/UNI-QUAD revision E is packaged in a 304 pin Super BGA package.

Figure 1: PM5349 S/UNI-QUAD Branding Format



2 S/UNI-QUAD FUNCTIONAL DESCREPANCIES

There are no known functional deficiencies for Revision E of S/UNI-QUAD (as of the publication date of this document).

Please report any functional deficiencies to PMC-Sierra.

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3 S/UNI-QUAD DATASHEET DISCREPANCIES

This section lists known documentation errata with regards to issue 5 of the S/UNI QUAD datasheet.

Legend

1. unaltered text is unchanged to add context to changes

2. new material is bold and Italicized

~~3. obsolete material is struck out~~

4. comments specific to this document are in italics

5. A vertical bar in left margin indicates that this is a new item which was not present in the previous issue of this document.

3.1 Page 49 Incorrect Line AIS Insert Description

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled ~~by the TLAIS input or~~ through an internal register ***(Reg 0x14 TSOP)*** accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

3.2 Page 137 Incorrect EPRDISRC and EPRDIEN Description

EPRDISRC

The enhanced path receive defect indication alarm source bit (EPRDISRC) controls the source of RDI input to be inserted onto the G1 byte. ~~When EPRDIEN is logic zero, this bit is ignored~~. ***When EPRDIEN is logic zero, the extended RDI bits of the G1 byte are always inserted according to value in register 0x49 bits G1[1:0]. When EPRDIEN is logic one and EPRDISCR is logic zero, the extended RDI bits of the G1 byte, bits 6 and 7, are inserted according to the value in the G1[1:0] register bits (register 0x49). When EPRDIEN is logic one and EPRDISCR is logic one, the value in register 0x49 G1[1:0] is ignored and the EPRDI bits in the G1 byte are set according to the setting of the Channel Auto Enhanced Path RDI Control registers (0x92 and 0x93).***

EPRDIEN

The enhanced path receive defect indication alarm enable bit (EPRDIEN) controls the use of 3-bit RDI mode. ***When EPRDIEN is set to logic 0, the basic path RDI scheme is used and only G1[5] is used to indicate PRDI and the value of the G1 byte, bits 6 and 7 are***

controlled by the G1[1:0] register bits (register 0x49). When EPRDIEN is set to logic 1, the enhanced path RDI scheme is used and the three G1[7:5] bits are used to indicate PRDI. The actual three bit code will be controlled according to the EPRDISRC.

3.3 Page 147 Incorrect G[1:0] Description

G[1:0]:

The G1[1:0] bits are inserted in bits 1 and 2 of the path status byte G1. ~~These bits are ignored when EPRDIEN is logic zero or when EPRDIEN and EPRDISRC are both logic one~~. ***These bits are ignored when EPRDIEN and EPRDISRC are both logic one. See the description of EPRDIEN and EPRDISRC for more details on how G1 can be controlled.***

3.4 Page 147 Incorrect PRDI Description

PRDI:

The PRDI bit controls the insertion of the path remote defect indication. When a logic one is written to this bit position, the PRDI bit position in the path status byte is set high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low. This bit is ignored ~~when EPRDIEN is logic zero or~~ when EPRDIEN and EPRDISRC are both logic one ***and the PRDI bit in the G1 byte (bit 6) is set according to the setting of the Channel Auto Enhanced Path RDI Control registers (0x92 and 0x93).***

3.5 Page 161 Incorrect Bit 4 (PSLMPRDI) in 0x91 (Channel Auto Path RDI Control) Description

Register 0x91: S/UNI-QUAD Channel Auto Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDPRDI	0
Bit 6	R/W	ALRMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	~~R/W~~	~~PSLMPRDI~~ ***Reserved***	~~1~~
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

3.6 Page 163 Incorrect Bit 4 in 0x92 (Channel Auto Enhanced Path RDI Control) Description

Register 0x92: S/UNI-QUAD Channel Auto Enhanced Path RDI Control

BIT	TYPE	FUNCTION	DEFAULT
Bit 7	R/W	LCDEPRDI	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	~~R/W~~	~~PSLMEPRDI~~ ***Reserved***	~~1~~
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	NOLOPCONEPRDI	0
Bit 1	R/W	Reserved	0
BIT 0	R/W	Reserved	1

3.7 Page 165 Incorrect Bit 1,0 and EPRDI_EN only write only in 0x93 (Channel Receive RDI and Enhanced RDI Control Extensions)

Register 0x93: S/UNI-QUAD Channel Receive RDI and Enhanced RDI Control Extensions

BIT	TYPE	FUNCTION	DEFAULT
Bit 7	R/W	PAISCONPRDI	0
Bit 6	R/W	NOPAISCONEPRDI	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	***W***	EPRDI_EN	0
Bit 1	~~R/W~~	~~UNEQPRDI~~ ***Reserved***	~~1~~
Bit 0	~~R/W~~	~~UNEQEPRDI~~ ***Reserved***	~~1~~

EPRDI_EN was indicated as a Read/Write bit. It is Write only bit.

3.8 Page 167 Incorrect Bit 4 and 5 in 0x95 (Channel Receive Path AIS Control) Description

Register 0x95: S/UNI-QUAD Channel Receive Path AIS Control

BIT	TYPE	FUNCTION	DEFAULT
Bit 7	R/W	PAISCONPAIS	1
Bit 6	R/W	LOPCONPAIS	1
Bit 5	~~R/W~~	~~PSLUPAIS~~	~~1~~
		Reserved	
Bit 4	~~R/W~~	~~PSLMPAIS~~	~~1~~
		Reserved	
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	PAISPAIS	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	Reserved	1

3.9 Page 171 Incorrect Bit 5 in 0x96 (Channel Receive Alarm Control #1)

Register 0x96: S/UNI-QUAD Channel Receive Alarm Control #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	~~R/W~~	~~PSLMEN~~	~~0~~
		Reserved	
Bit 4	R/W	PERDIEN	0
Bit 3	R/W	PRDIEN	0
Bit 2	R/W	PAISEN	0
Bit 1	R/W	LCDEN	0
Bit 0	R/W	LOPEN	0

3.10 Page 188 Incorrect LOPCONPRDI Description

The Loss of Pointer Concatenation Indication PRDI (LOPCONPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPCONPRDI is set to logic ~~zero~~ ***one***, the transmit line RDI will be inserted. When LOPCONPRDI is set to logic zero, no action is taken. This register bit has effect only if the AUTOPRDI register bit is also set to logic one.

3.11 Page 204 Incorrect Bit 7 Z1/S1_CAP description in 0x95 (RASE Configuration/Control)

Z1/S1_CAP:

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for ~~three~~ ***eight*** consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

3.12 Page 229 Incorrect Path overhead byte H4 description

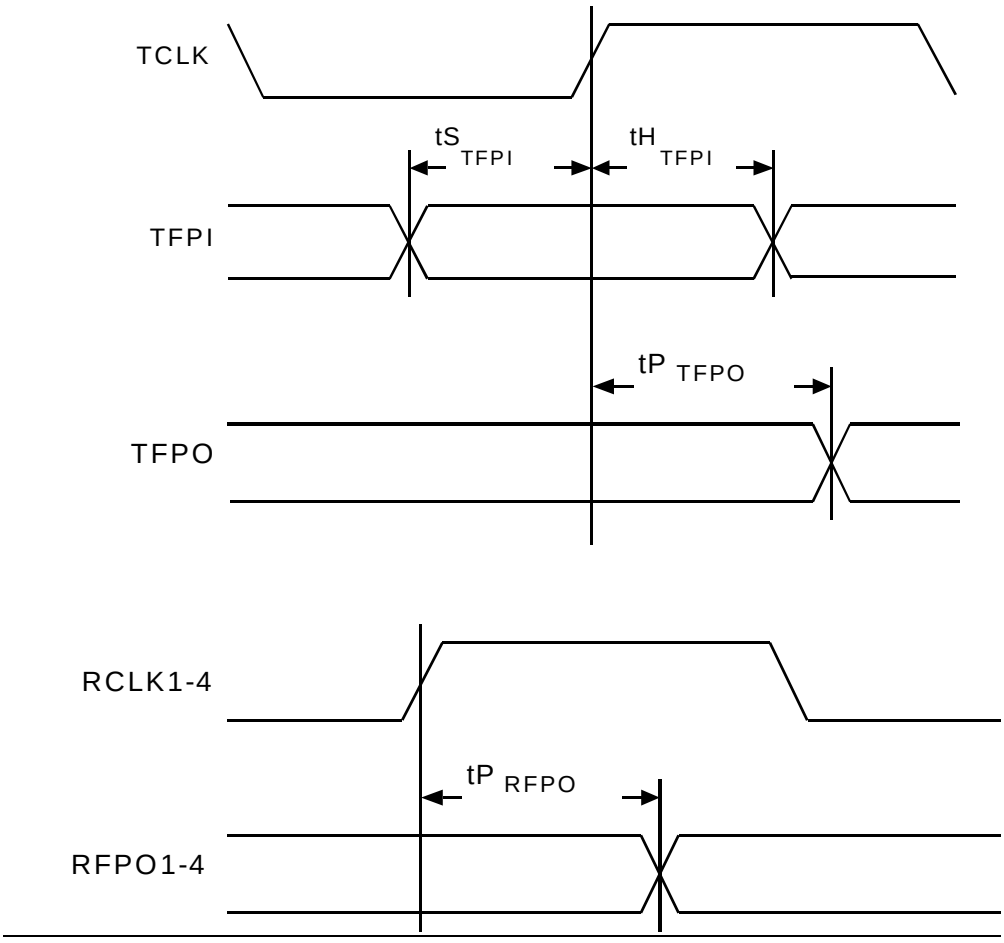
H4: The multiframe indicator byte is a payload specific byte, and is not used for ATM payloads. ~~This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.~~

3.13 Pg. 263 Revised TFPI Setup and Hold times

Table 1: Transmit and Receive Frame Pulse Timing (Figure 1)

Symbol	Description	Min	Max	Units
tS_{TFPI}	TFPI Set-up Time to TCLK High	~~10~~ ***15***		ns
tH_{TFPI}	TFPI Hold Time to TCLK High	~~10~~ ***0***		ns
tP_{TFPO}	TCLK High to TFPO Valid	0	10	ns
tP_{RFPO}	RCLK1-4 High to RFPO1-4 Valid	0	10	ns

Figure 1: Transmit and Receive Frame Pulses



3.14 Pg. 30 Revised Pin description notes

2. The RDAT[7:0], RPRTY, RSOC, RCA, TCA, TCLK and RCLK1-4 outputs have a ~~16~~ ***4*** mA drive capability. All other output pins have a 2 mA drive capability. The TXD+ and TXD- outputs ***should*** be terminated in a passive network and interface at PECL levels.

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