PM73488

QSE

10 GBIT/S ATM SWITCH FABRIC BUILDING BLOCK

REFERENCE DESIGN

RELEASED

ISSUE 3: NOVEMBER 1999

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Dec 1998	Document created.
2	Jan 1999	Added Schematics Added BOM Added Implementation Description
3	Oct 1999	Added PLD Section Updated BOM Added AC Coupling caps to serial receivers Added cPCI interface

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 FEATURES

- Two PM73488 QSE 5Gbit/s ATM Switching Fabric Element devices to perform cell switching.
- Interfaces to multiple PM73488 QSE reference designs or PM73487 QRT reference designs to create larger switch fabrics.
- Each QSE reference design may be connected to up to 8 other QSE or QRT reference designs at the input ports and 8 QSE or QRT reference designs at the output ports.
- High speed serializer/deserializer I/O's decrease inter-board pin count and increases switch design flexibility.

2 APPLICATIONS

- Core Switches
- LAN Switches
- Edge Switches
- Enterprise Switches

3 REFERENCES

1. PMC-Sierra, Inc., PMC-980616, “PM73488 QSE 5 Gbit/s ATM Switch Fabric Element Datasheet”, Issue 2, October 1998.

2. PMC-Sierra, Inc., PMC-980618, “PM73487 QRT 622 Mbps ATM Traffic Management Device Datasheet”, Issue 2, October 1998.

3. PMC-Sierra, Inc., PMC-990330, “ATM Switch using S/UNI-ATLAS, QRT, and QSE”, Issue 2, July 1999.

4 APPLICATION EXAMPLES

The PM73488 QSE device is a 32x32 ATM switch device capable of peak bandwidth of 8 Gbits/s and a sustainable bandwidth of 5 Gbit/s. The device is intended for use with other QSE devices to form a larger switch fabric. The QSE supports unicast cells with multiple priorities. To ensure switch fabric performance, the QSE ATM switch element utilizes randomization and “Evil Twin” switching to prevent build up of internal hot spots.

The PM73488 QSE reference design features two QSE devices which may be used alone to create a 64x64 10 Gbit/s switch or with other QSE reference designs to make larger switch fabrics. Note, in the case of a 64x64 fabric, the port cards would utilize two PM73487 QRT devices and a compatible serialization strategy. Multiple configurations are possible allowing a variety of bandwidth capacities and port numbers. Two such implementations are shown below in figure 1 and figure 2.

Figure 1 - Single Stage 10 Gbit/s ATM Switch Application

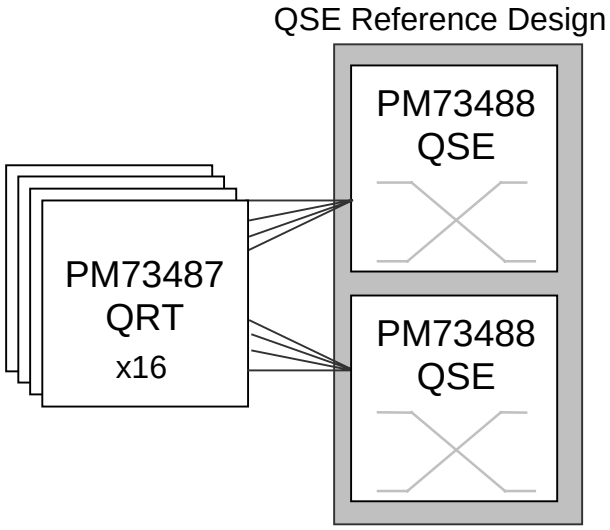


Figure 2 - Three Stage 40 Gbit/s ATM Switch Application

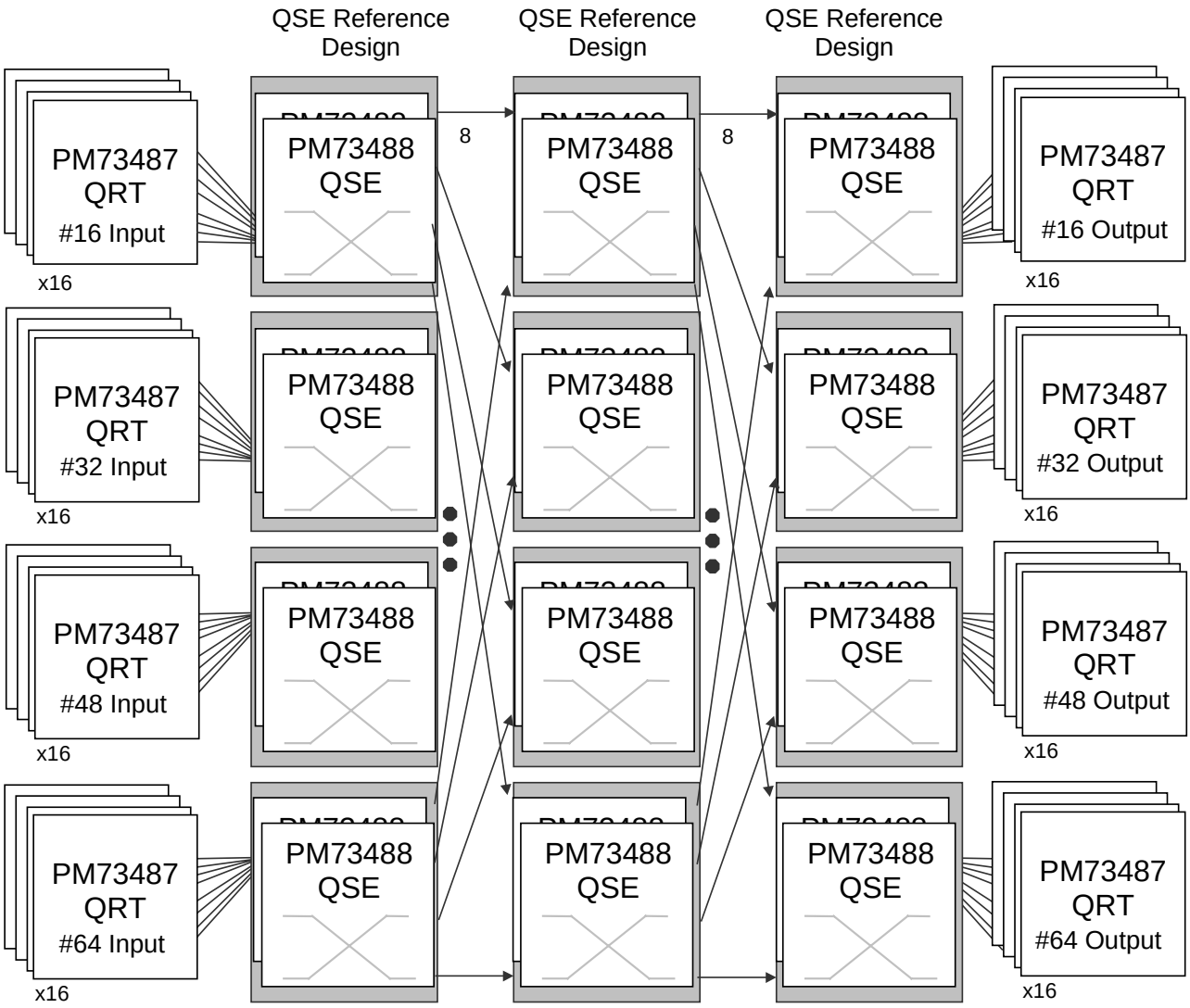
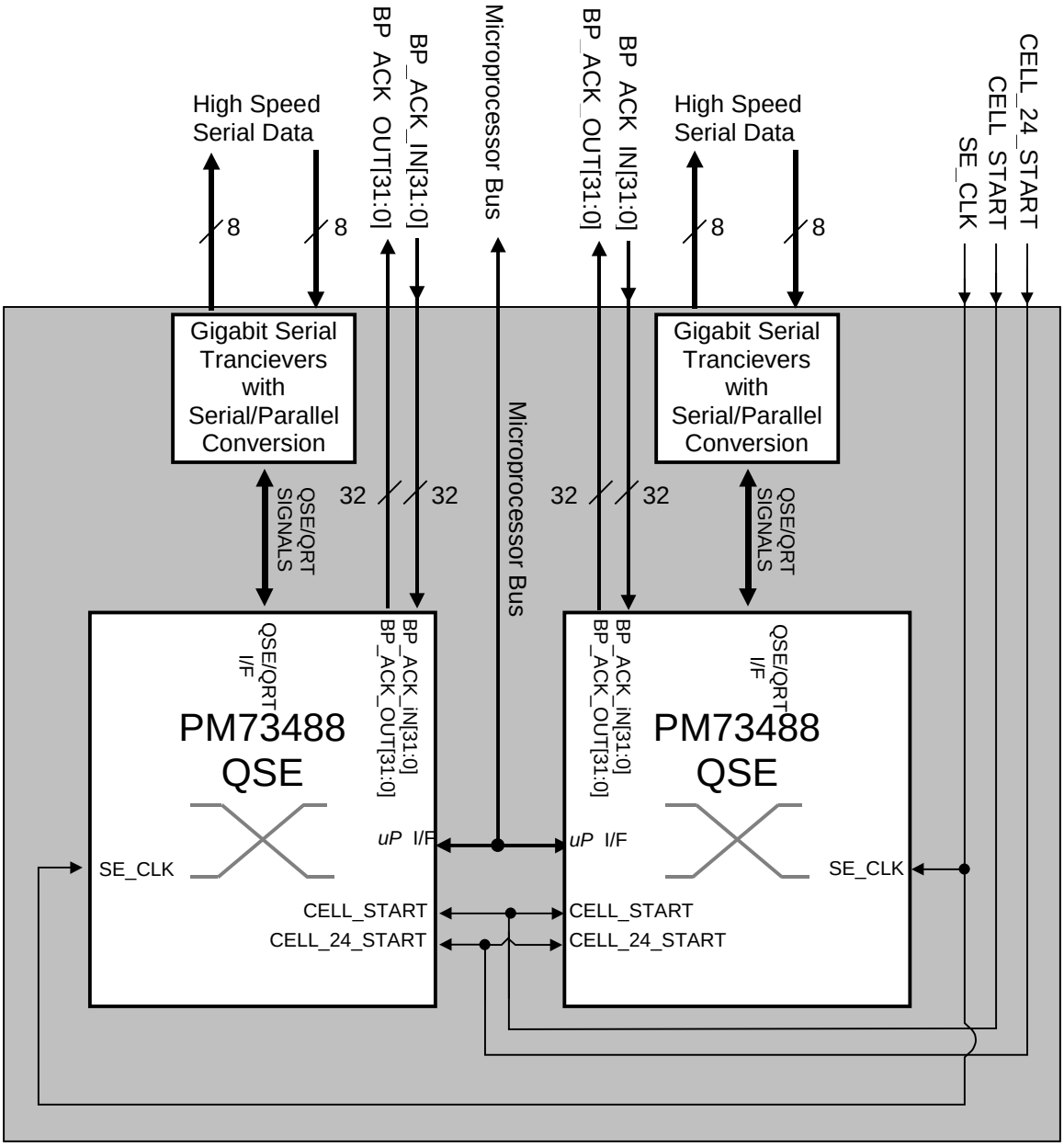


Figure 1 shows a single stage switch implemented using only one QSE reference design. Figure 2 shows a 40 Gbit/s three stage fabric using 12 QSE reference designs. Inherently, the three stage design allows for a greater number of paths from input to output.

At the switch fabric inputs and outputs, the QSE reference design interfaces to QRT reference designs.

5 BLOCK DIAGRAM



6 DESCRIPTION

The PM73488 QSE Reference Design is a basic switch element designed to allow flexible and simple design of larger ATM switch fabrics. The reference design features two PM73488 QSE 5 Gbit/s ATM Switching Element devices allowing a 10 Gbit/s switch to be implemented on a single reference design. Each QSE device features 32 input and output ports.

In an effort to minimize the off-card interconnect requirements the data and SOC signals for 4 ports are serialized into high speed serial streams. Therefore each QSE is supported by 8 sets of serializer and deserializers devices. The serial streams may be connected to other QSE and QRT devices which also utilize serializers.

The BP_ACK signals are not serialized and are handled in a more conventional manner.

Timing references SE_CLK, CELL_START, and CELL_24_START are derived from off board sources and are global within the switching fabric.

7 FUNCTIONAL DESCRIPTION

As shown in the block diagram the QSE switch card consists primarily of 2 identical independent QSE circuits. Each QSE has 32 input ports and 32 output ports each consisting of a 6 pin interface. In order to minimize interconnect requirements Gigabit serializer and deserializer devices are utilized.

The transmit serializers used are 3.3 volt devices which can generate high–speed data links between switch elements. These devices are capable of accepting 17 bits of parallel data at a **SE_CLK** (66 MHz) data rate and serialize it into a differential data stream at 20 times the SE_CLK rate utilizing a PLL multiplying technique. The extra bits are used to convey clocking, control, and synchronization information.

The receive serializers are also 3.3 volt devices, and are capable of receiving Gigabit rate data streams via a differential pair inputs and resolving them into 17 bits of parallel data. They utilize PLL technology in order to synchronize to the incoming data stream and to extract the data information. The incoming rate is actually 20 times the parallel word rate. The other bits are used for clocking, control, and synchronization information. These devices are operated with their **PASSENB** mode off in this particular application. The receivers extract the data from the stream, and emit the data to the QSE devices at the rate determined by the recovered clock. Since the QSE devices operate with their phase aligners on, there is no requirement that the data be phase aligned to the **SE_CLK** signal. However, the recovered clock will be frequency locked to the SE_CLK, since the entire system is driven from the same clock source.

The back pressure acknowledge signals are not serialized in this design. There is one BP_ACK_IN and one BP_ACK_OUT associated with each port of the QSE. These signals are sent in the opposite direction from the data, and therefore do not lend themselves to efficient serialization. The BP_ACK_OUT signals are registered before leaving the card in order to increase the bus drive capability. The QSE devices receive these signals with phase aligners so timing constraints are minimal.

8 IMPLEMENTATION DESCRIPTION

8.1 CPU Interface (sheets 3-5)

The 2 QSE devices are controlled via a CPCI interface. CPCI signals arrive via the P1 connector, and are routed to a PLX 9050 PCI slave interface device. This device simplifies connection of peripherals to a CPCI master. The 9050 supplies a local bus of its own to the QSE devices. Appropriate control signals, along with dedicated interrupt and acknowledge signals, and chip select signals are used to control all QSE transactions with the CPU.

8.2 Multicast Circuit (sheets 10 &17)

Each QSE has an external multicast RAM circuit. This RAM is completely accessed and operated via dedicated QSE pins. This RAM can be either a 2 MB or 4 MB device depending upon number of multicast groups to be supported. If less than 128 multicast groups are required then this RAM need not be installed. The RAM interface operates at 100 MHz and must be considered a high speed circuit for PCB design rules.

8.3 Switch Connectors (sheets 5 &6)

Switch data information is conveyed in and out of the card by AMP HS3 family high-speed, high-density connectors. These devices are strip-line devices with a characteristic impedance of 50 ohms and are characterized for high-speed digital data, as well as Gigabit differential serial streams.

8.4 Receive Serializers (sheets 11,12,18 &19)

Each QSE has 8 receive serializers, one for each QSE group. They accept differential data from off the card via the HS3 connectors and convert it to a parallel 17 bit data bus. This contains 4 ports of data information and one SOC status. The SOC status signal is sent to all 4 ports of the switch group. This is acceptable since all 4 ports of the data passes through the serializers originated with identical SOC timing. This data is then presented to the QSE input ports.

The deserializers satisfy the skew requirements of the QSE devices when operated with phase aligners on.

8.5 QSE Switch Elements (sheets 13,14,20, 21 & 24)

Each QSE accepts data from the receive serializers. This data flows through the QSE devices and emerges on one of the 32 output ports. The QSE devices supply only one output SOC for each 4 ports of data.

There are 32 BP_ACK_OUT signals per QSE, which are registered before they leave the switch card. These are to be supplied to upstream switch elements to inform the sending entity of the disposition of incoming cells.

There are 32 BP_ACK_IN signals per QSE. These are used to inform the QSE devices of how exiting cells were accepted by downstream switch elements. These inputs are supplied directly to the QSE devices without additional buffering.

8.6 Transmitter Serializers (sheets 15, 16, 22 & 23)

Each group of data emerging from the QSE devices, which consists of 4 nibbles of port data and one SOC, are immediately serialized into Gigabit differential data streams. This requires 8 serializers per QSE. These devices require a phase aligned SE_CLK in order to clock the data into the serializers. These high speed serial streams then exit the card via the appropriate data connector.

8.7 LED Display (sheet 25)

A LED display is provided in order to display the status of the serializer devices. Each transmit serializers supplied a **LOCKED** output which indicates the transmit PLL is sucessfully locked to the parallel clock rate. Each receiver supplies a **RXREADY** signal which indicates word alignment has established an error free history. Each receiver also provides a **RXERROR** signal that indicates there is something wrong with the current word received. These 48 status signals are displayed 8 at a time on the status LEDS. Another 3 LEDs are utilized to indicate which group of 8 status signals are currently being displayed. A front panel momentary switch is used to select which group of LEDS is currently displayed. Another LED is utilized to indicate if any of the 48 status signals is indicating a failure condition. Specifics regarding this display information is supplied in the section that describes the PLD source code.

8.8 Miscellaneous Circuitry (sheet 26)

The SE_CLK signal is the main clock for the switch card. This signal is brought in and buffered to create the numerous SE_CLK required for card operation. These are utilized throughout the card. Care must be taken to control the clock skew between the QSE devices, the transmit serializers, and the ack registers. This is accomplished by matching the lengths of the clock lines.

The switch card requires cell start information for the QSE devices. These are generated off card as CELL_START and CELL_24_START. They are registered on card and then supplied to the QSE devices,

J6 is a 20 pin right angle connector which is located on the front card edge. This connector is compatible with HP logic analyzer probes. Several important signals can be verified via this connector.

8.9 Power Supply Issues

Most of the devices on the switch card are high-speed and consequently operate with high edge rates. In addition the QSE devices can switch many outputs simultaneously. The HP devices are by nature extremely sensitive to extraneous noise due to the analog nature of their PLL circuitry.

Because of these issues, proper bypass methodology must be employed. Each power supply pin for all devices must be properly bypassed.

The HP devices have a separate power supply for analog portion of the parts. These pins are supplied via separate power and ground planes. The reference between the ground planes is established off the card. The analog pins require their own bypass capacitors.

Status LEDs are provided for both power supplies to indicate if the voltages are present. These do not reflect the accuracy of the voltages, but merely their presence.

9 SCHEMATICS

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Title: CONTENTS

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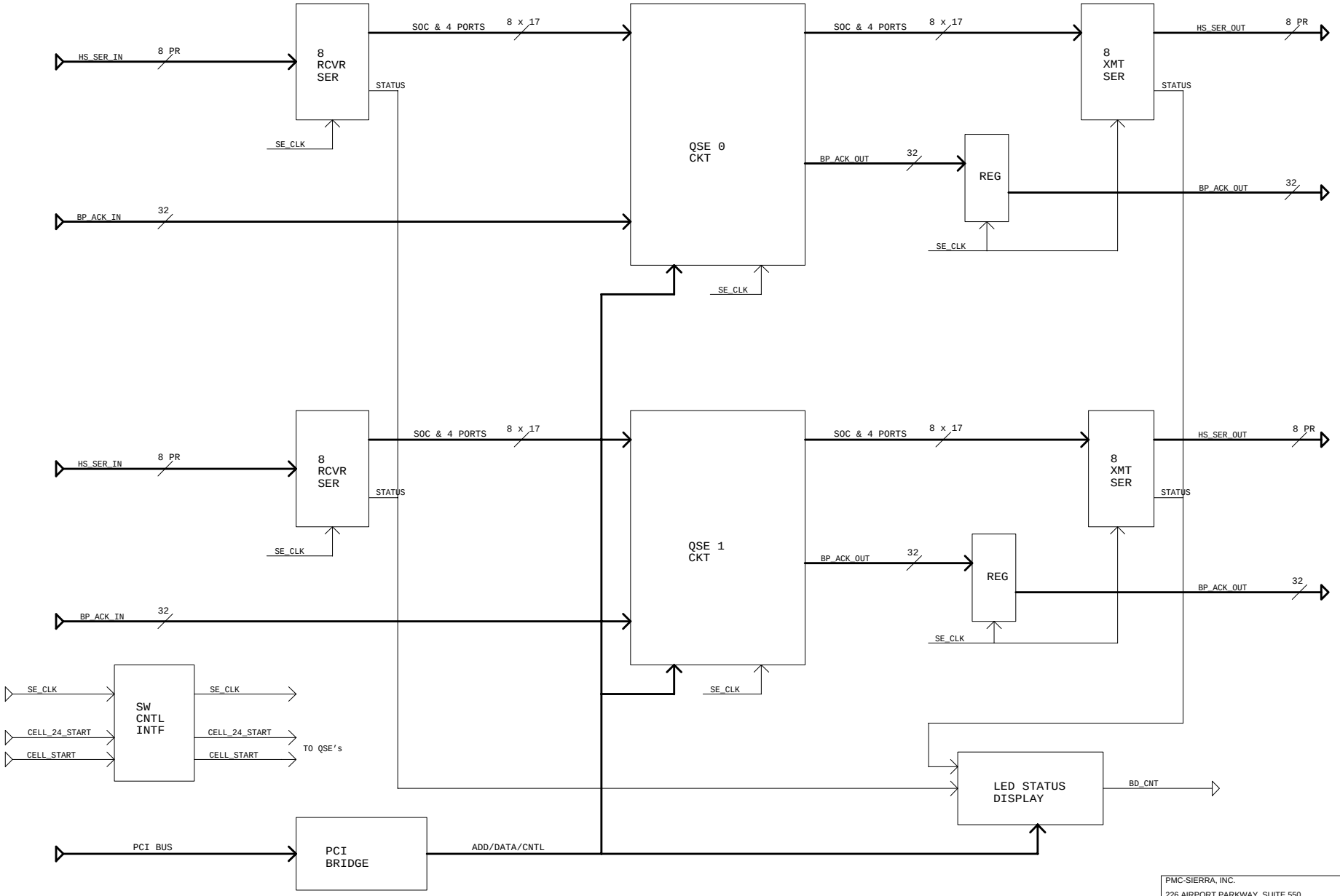

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Title: BLOCK DIAGRAM

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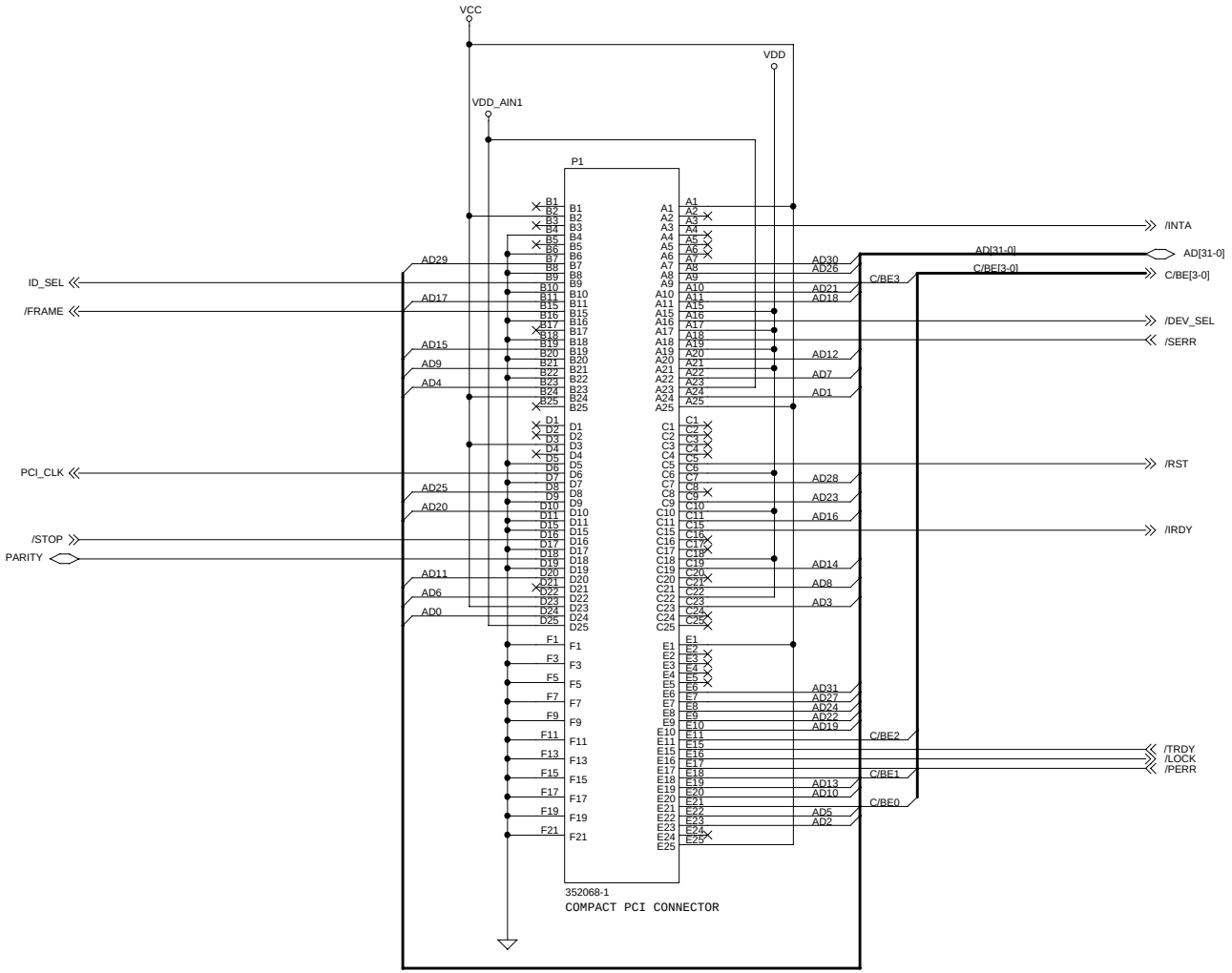

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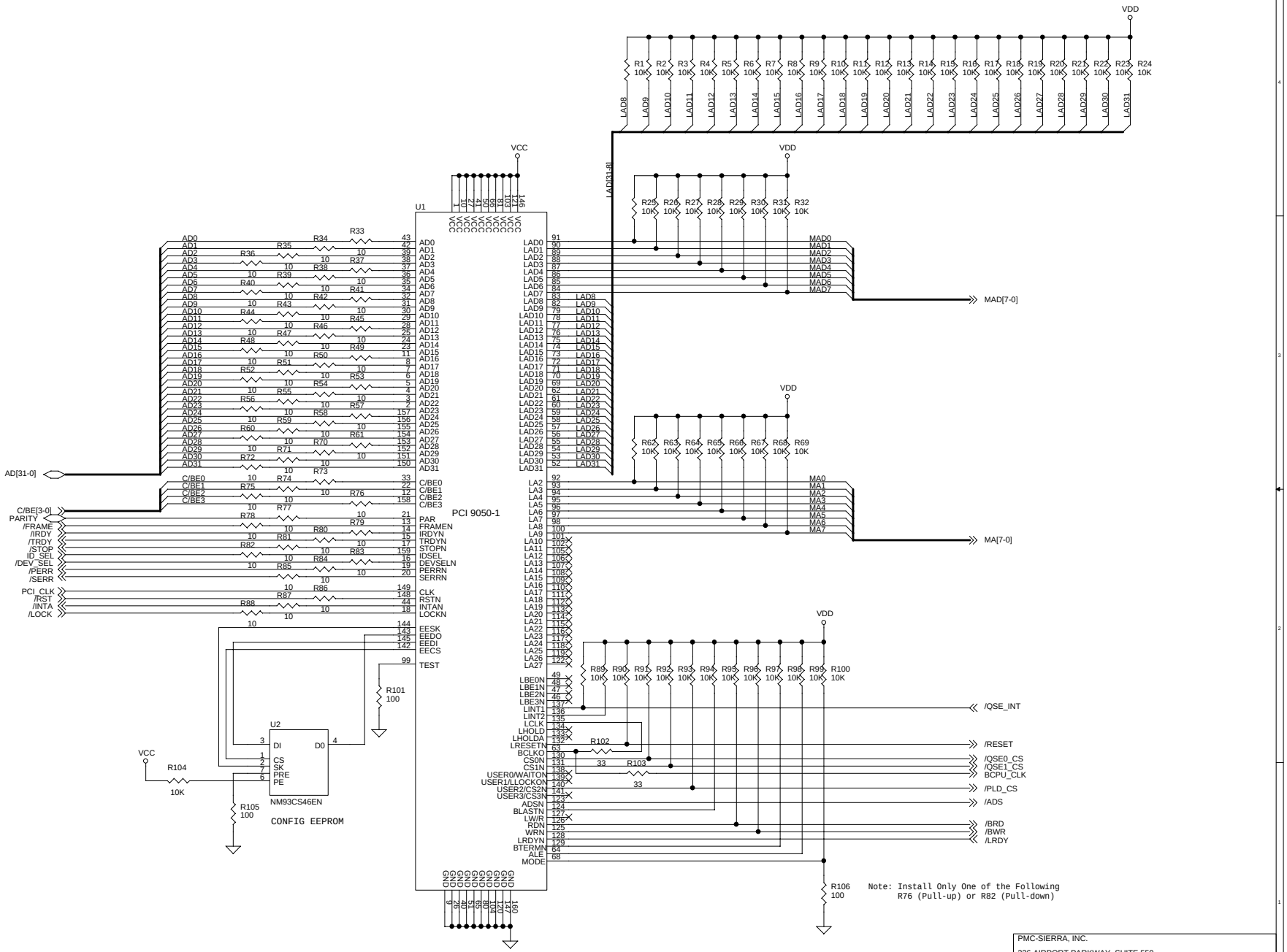

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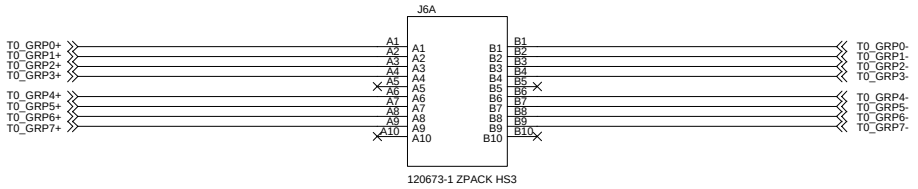
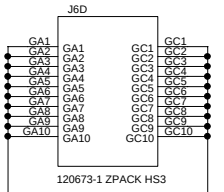
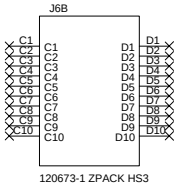
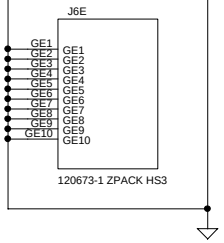
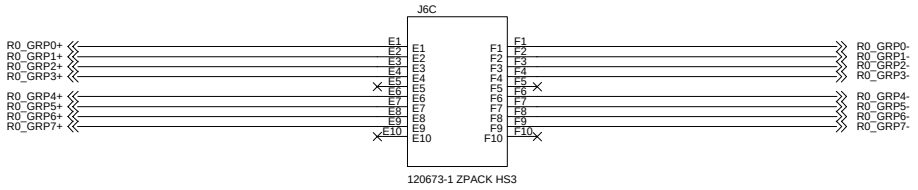
BP_ACK REGISTERED OUTPUT FROM QSE











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Title	HS SERIAL CONNECTOR 1	
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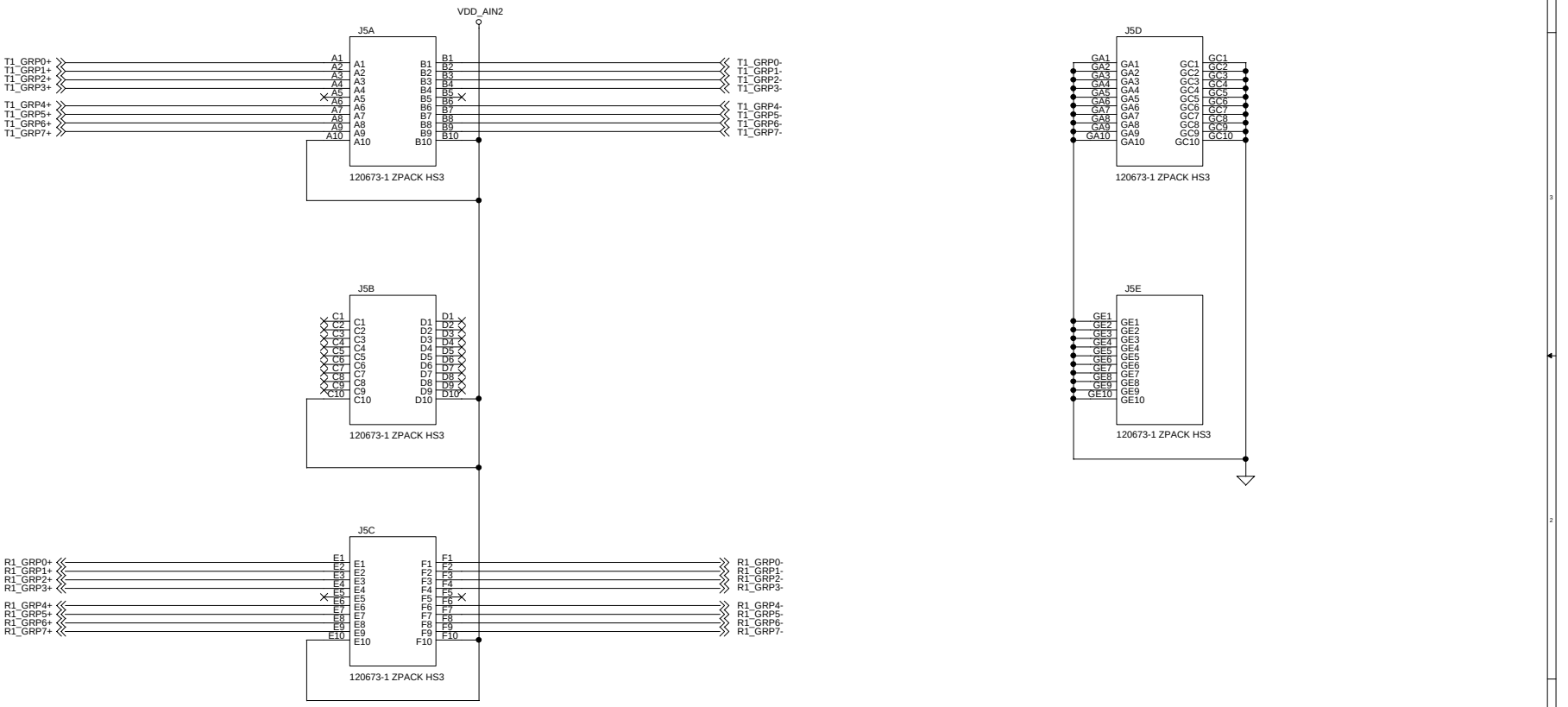

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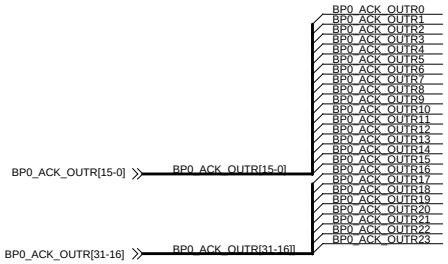

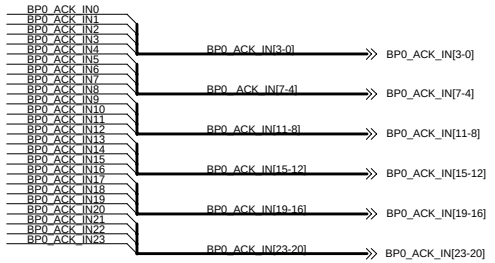

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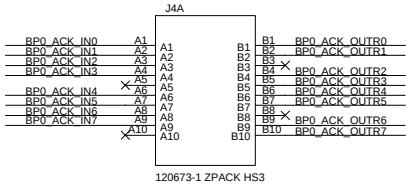

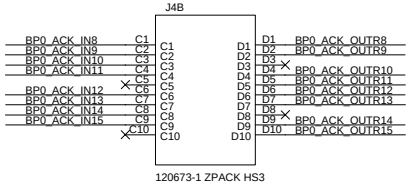

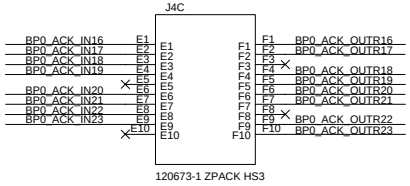

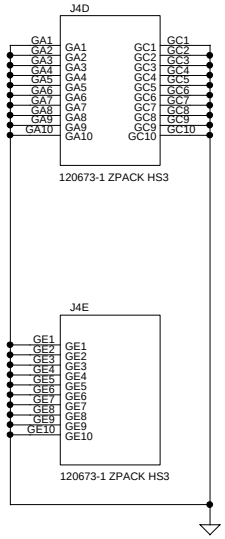

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Title	ACK CONNECTOR 1	
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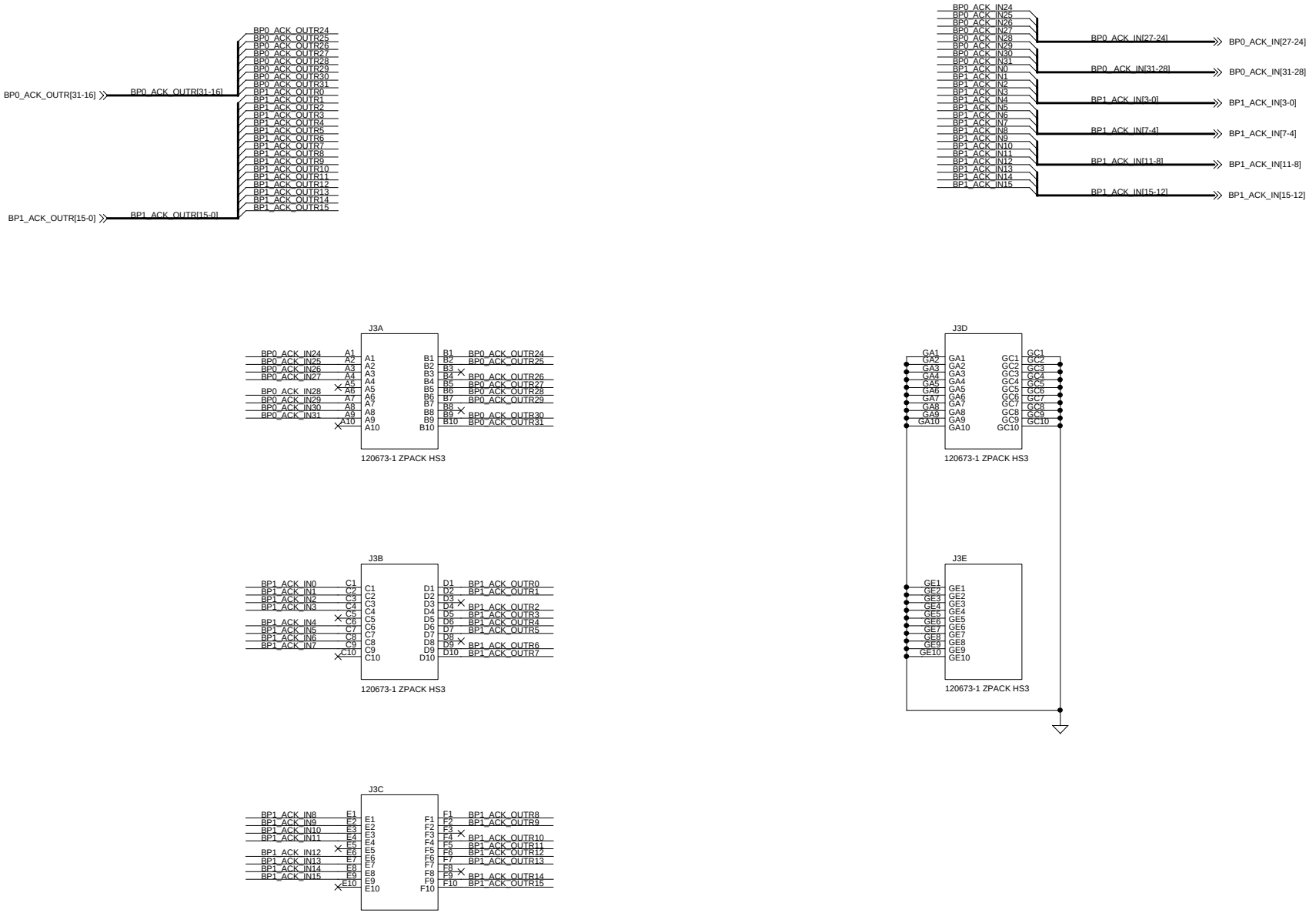

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Title	ACK CONNECTOR 2	
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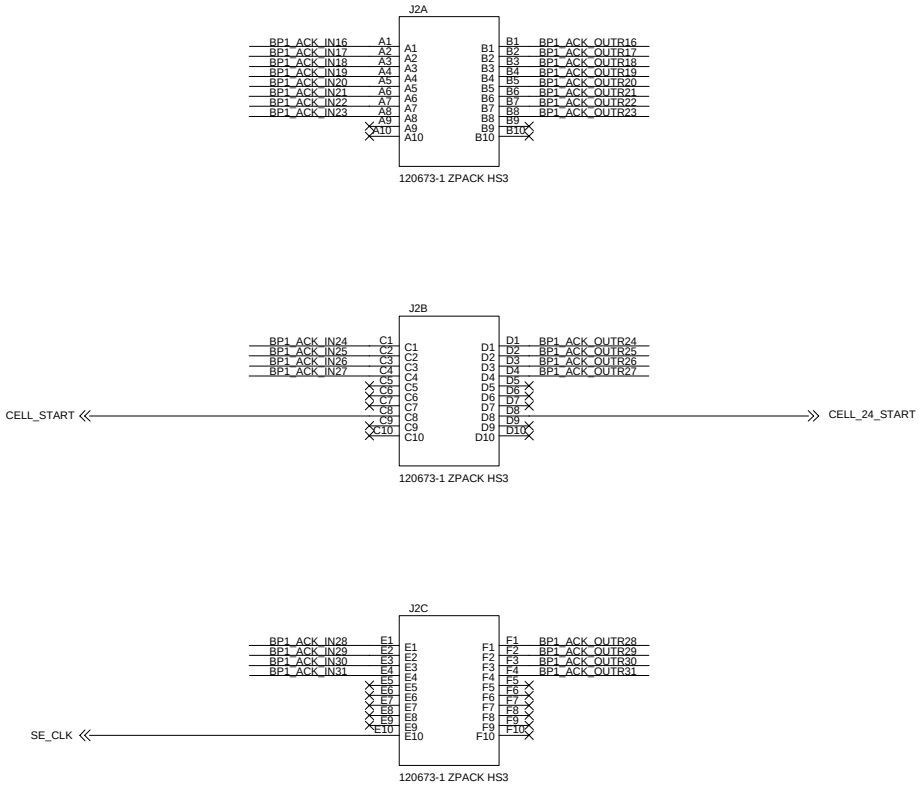

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Title: ACK CONNECTOR 3

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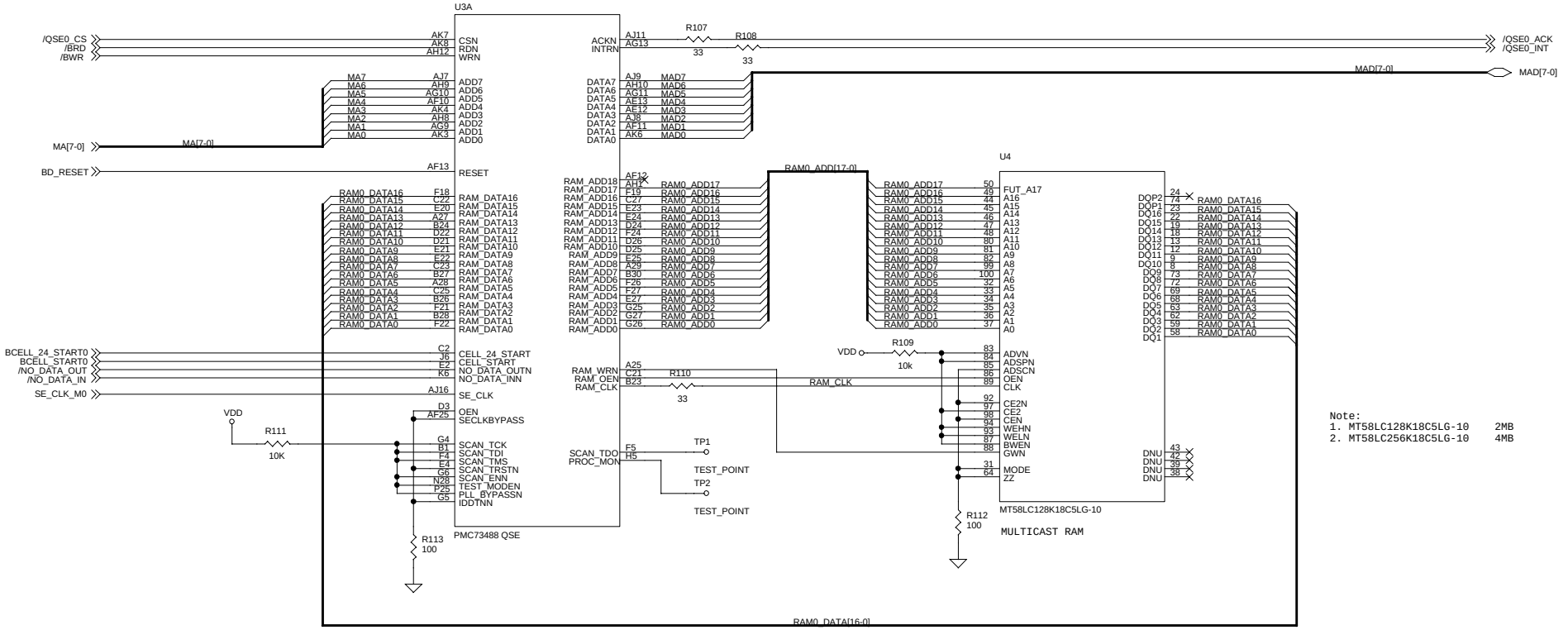

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Title	QSE0 CPU & MULTICAST CKT
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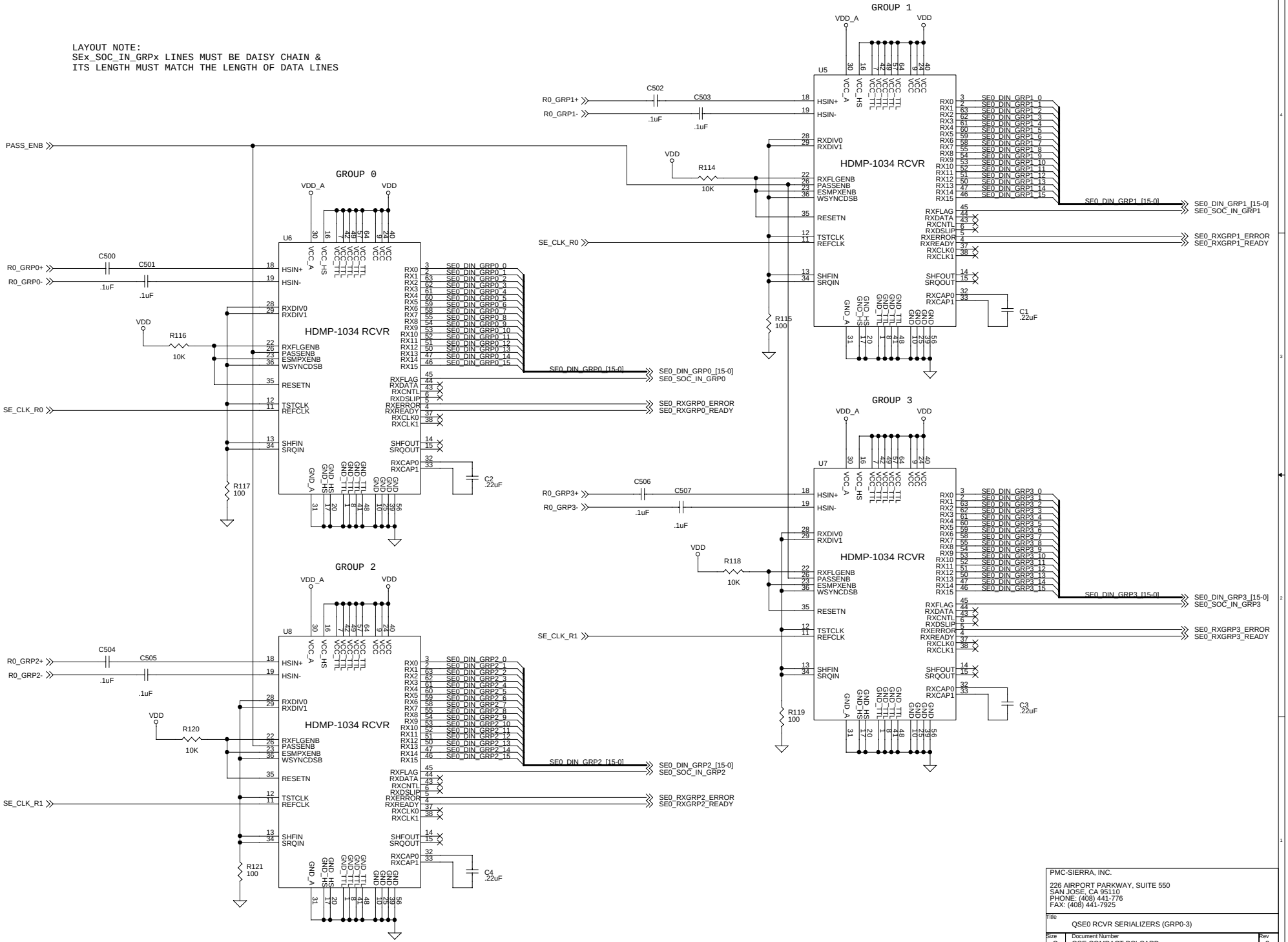
LAYOUT NOTE:
SEx_SOC_IN_GRPx LINES MUST BE DAISY CHAIN &
ITS LENGTH MUST MATCH THE LENGTH OF DATA LINES



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Title	QSE0 RCVR SERIALIZERS (GRP0-3)	
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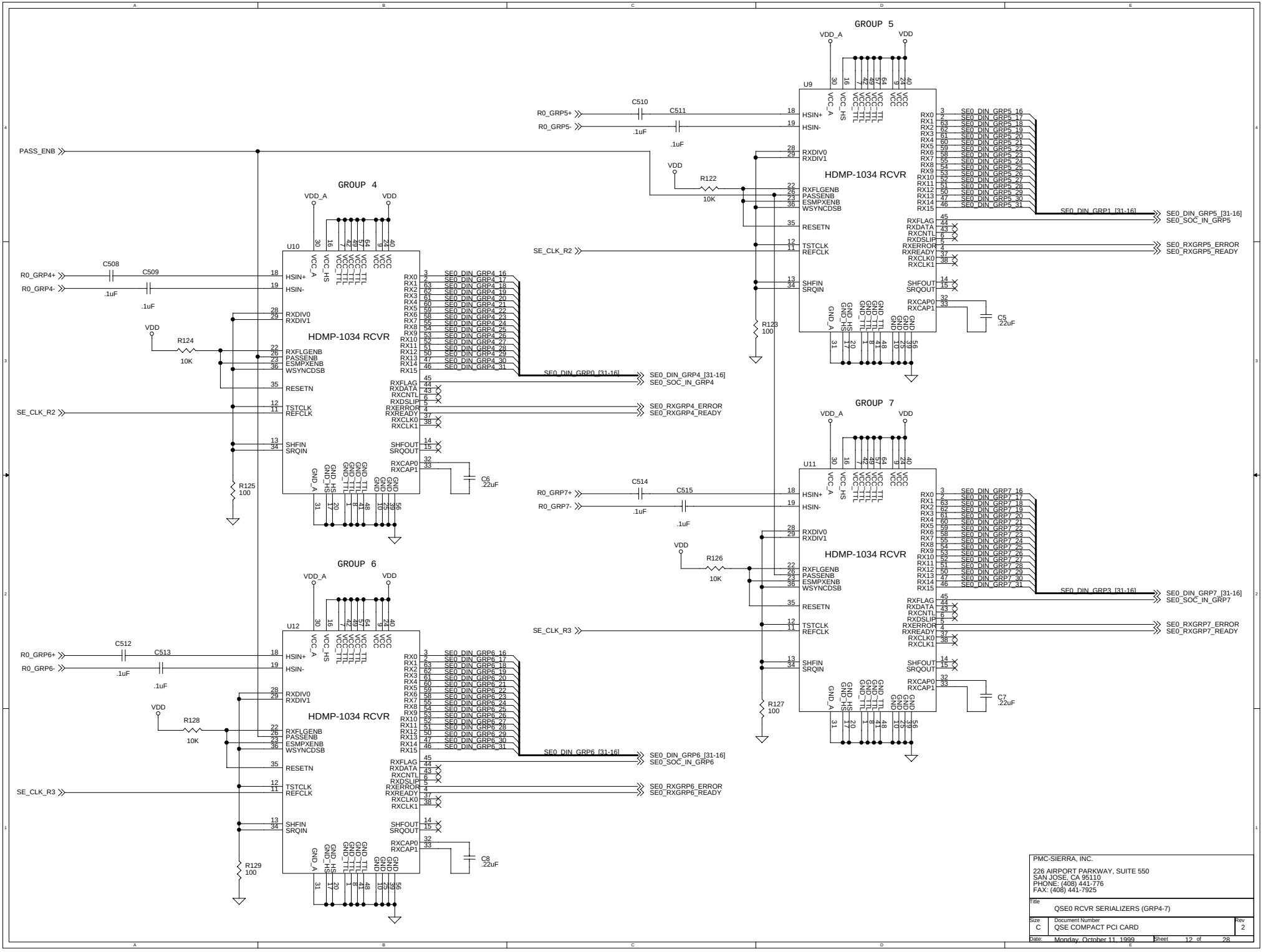

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Title	QSE0 RCVR SERIALIZERS (GRP4-7)	
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GROUP 0
U3B
SE0_SOC_IN_GRP0
BP0_ACK_IN[3-0]
SE0_DIN_GRP0_[15-0]
SE0_SOC_OUT_GRP0
BP0_ACK_OUT[3-0]
SE0_DOUT_GRP0_[15-0]
PMC73488 QSE
GROUP 1
U3C
SE0_SOC_IN_GRP1
BP0_ACK_IN[7-4]
SE0_DIN_GRP1_[15-0]
SE0_SOC_OUT_GRP1
BP0_ACK_OUT[7-4]
SE0_DOUT_GRP1_[15-0]
PMC73488 QSE
GROUP 2
U3D
SE0_SOC_IN_GRP2
BP0_ACK_IN[11-8]
SE0_DIN_GRP2_[15-0]
SE0_SOC_OUT_GRP2
BP0_ACK_OUT[11-8]
SE0_DOUT_GRP2_[15-0]
PMC73488 QSE
GROUP 3
U3E
SE0_SOC_IN_GRP3
BP0_ACK_IN[15-12]
SE0_DIN_GRP3_[15-0]
SE0_SOC_OUT_GRP3
BP0_ACK_OUT[15-12]
SE0_DOUT_GRP3_[15-0]
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Title
QSE0 SWITCH ELEMENTS (GRP0-3)
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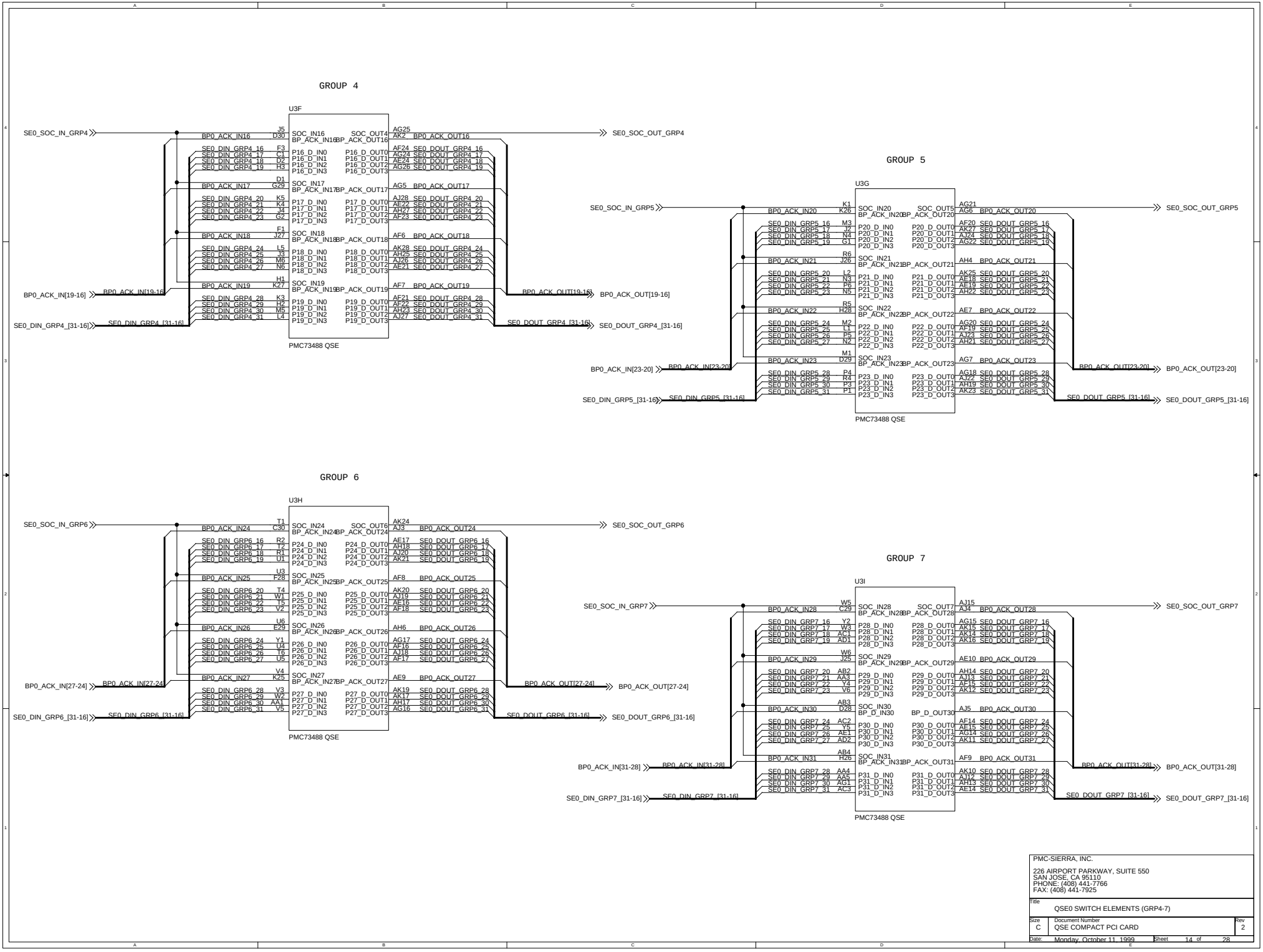

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Title: QSE0 SWITCH ELEMENTS (GRP4-7)

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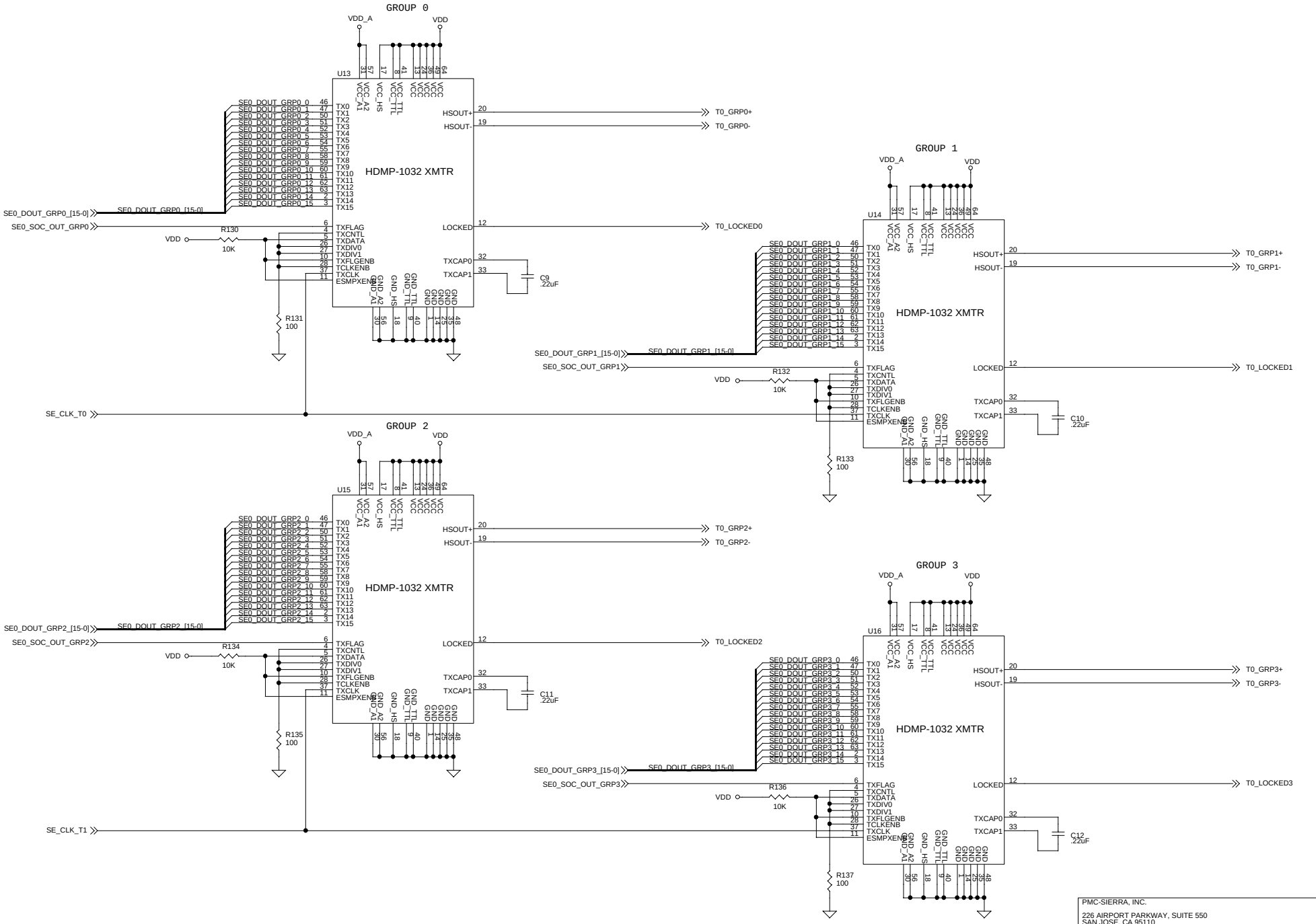

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Title: QSE0 XMTR SERIALIZERS (GRP0-3)

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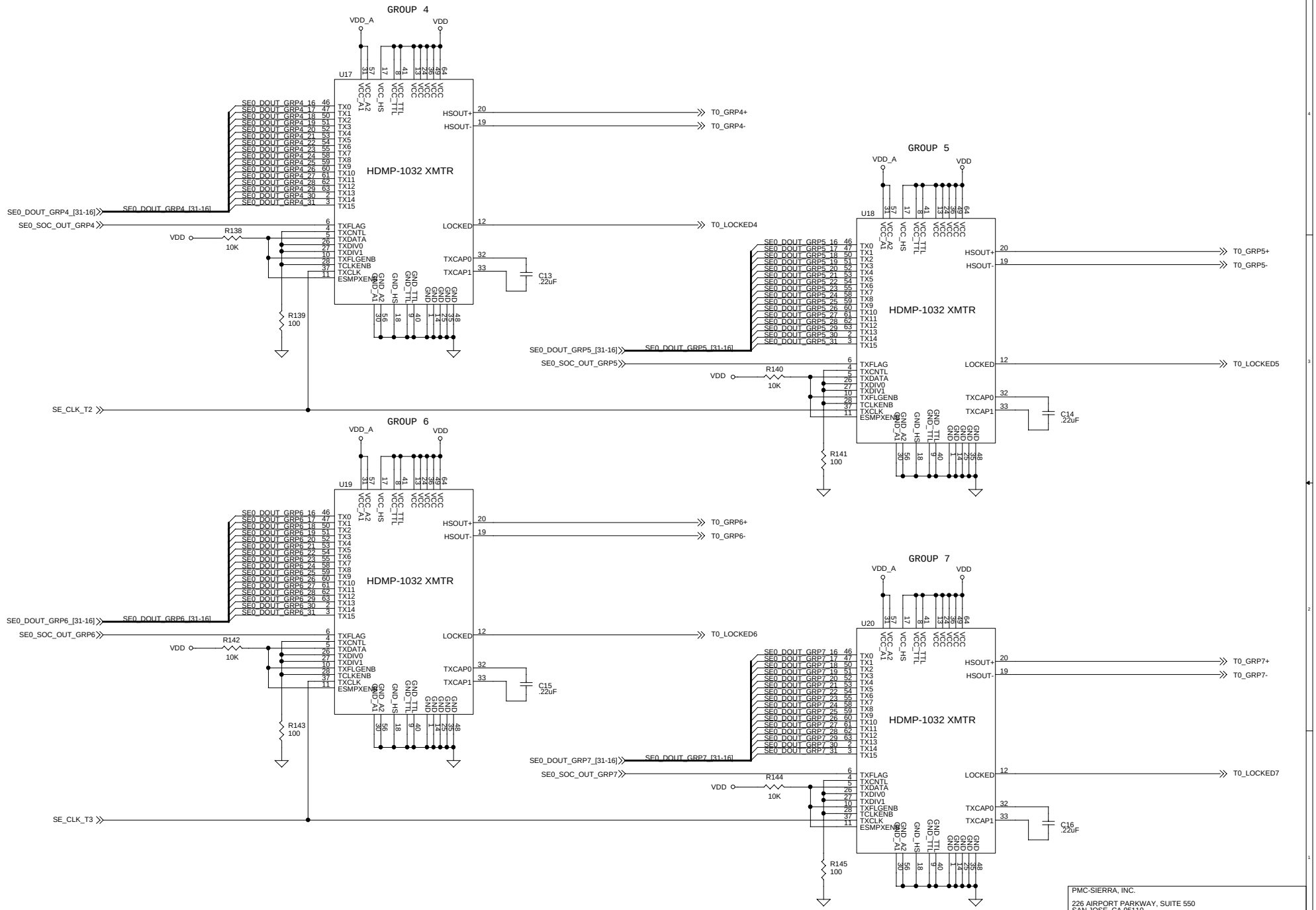

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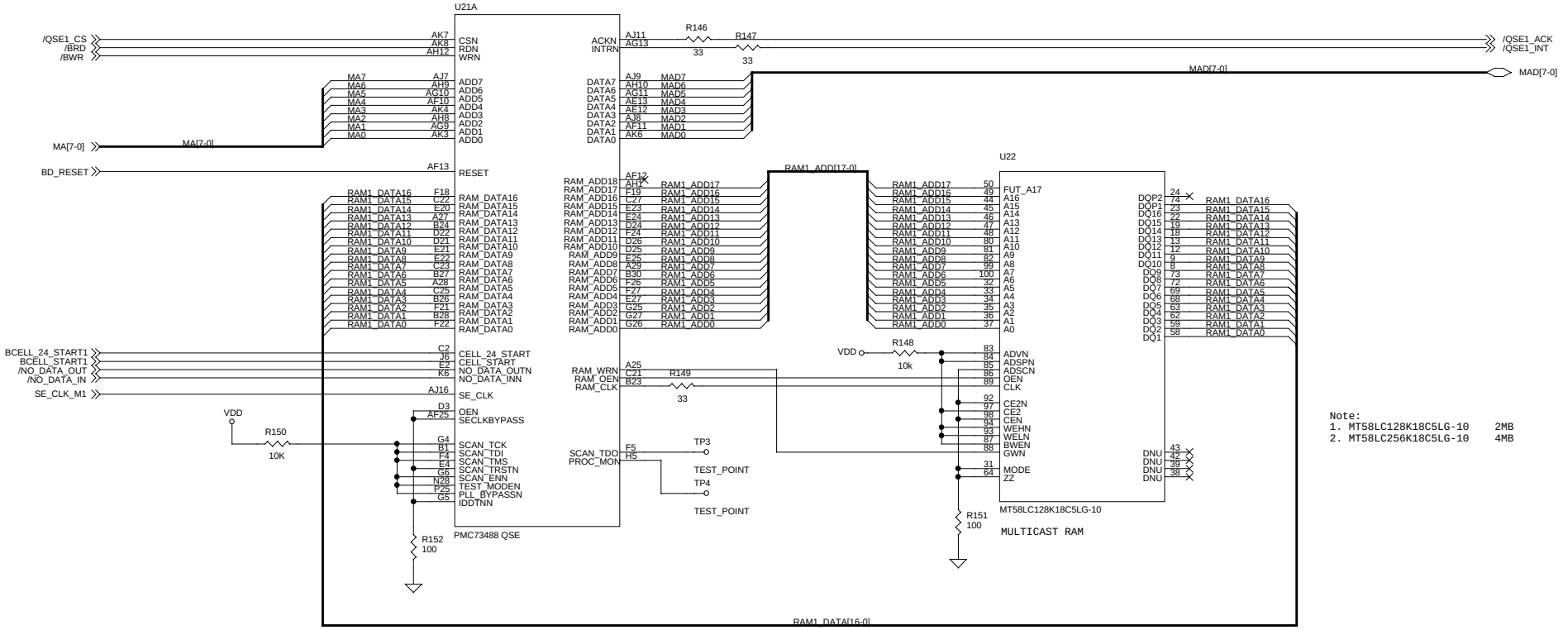
226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: QSE0 XMTR SERIALIZERS (GRP4-7)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 16 of 28



Note:
1. MT58LC128K18C5LG-10 2MB
2. MT58LC256K18C5LG-10 4MB

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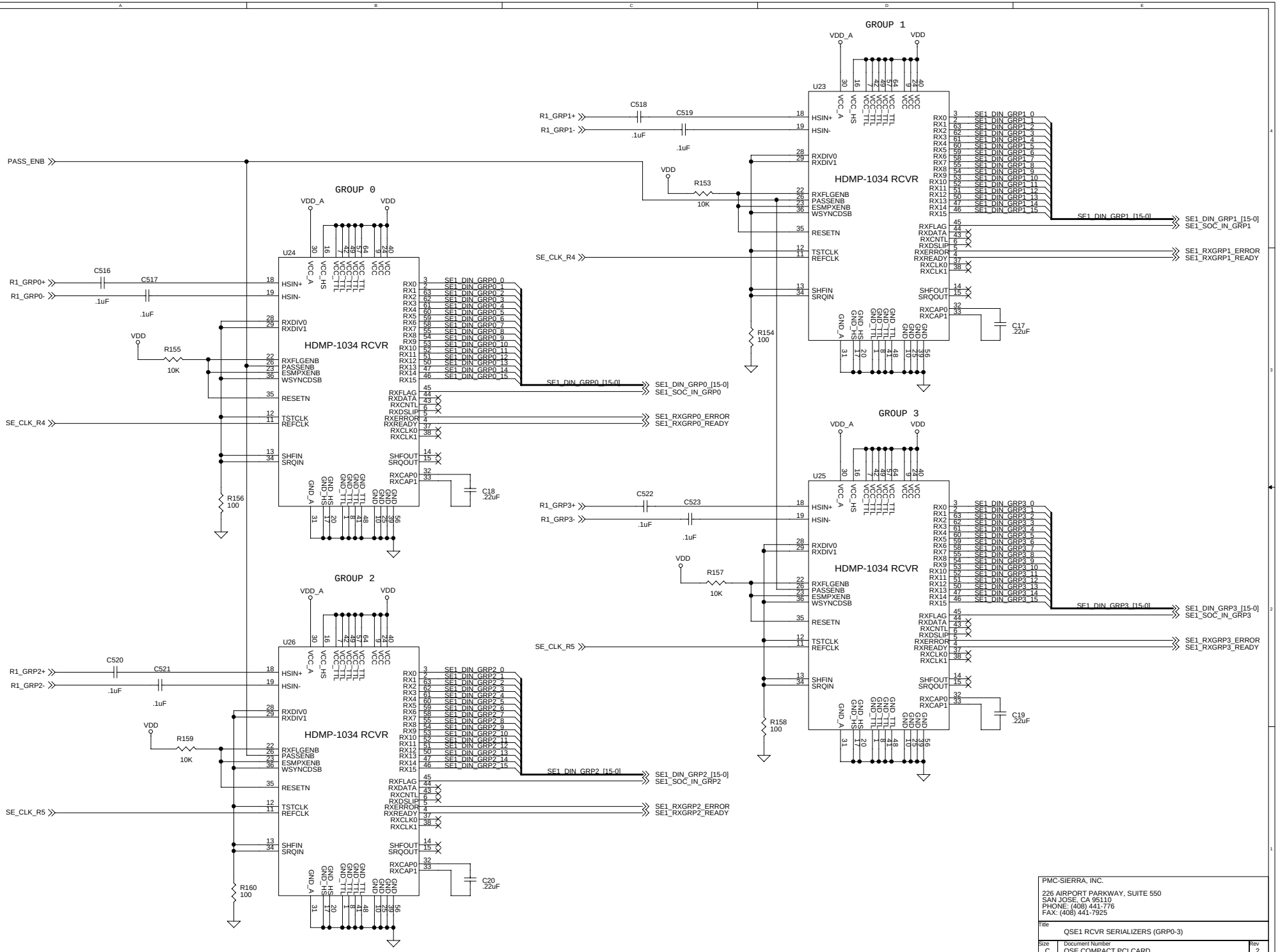
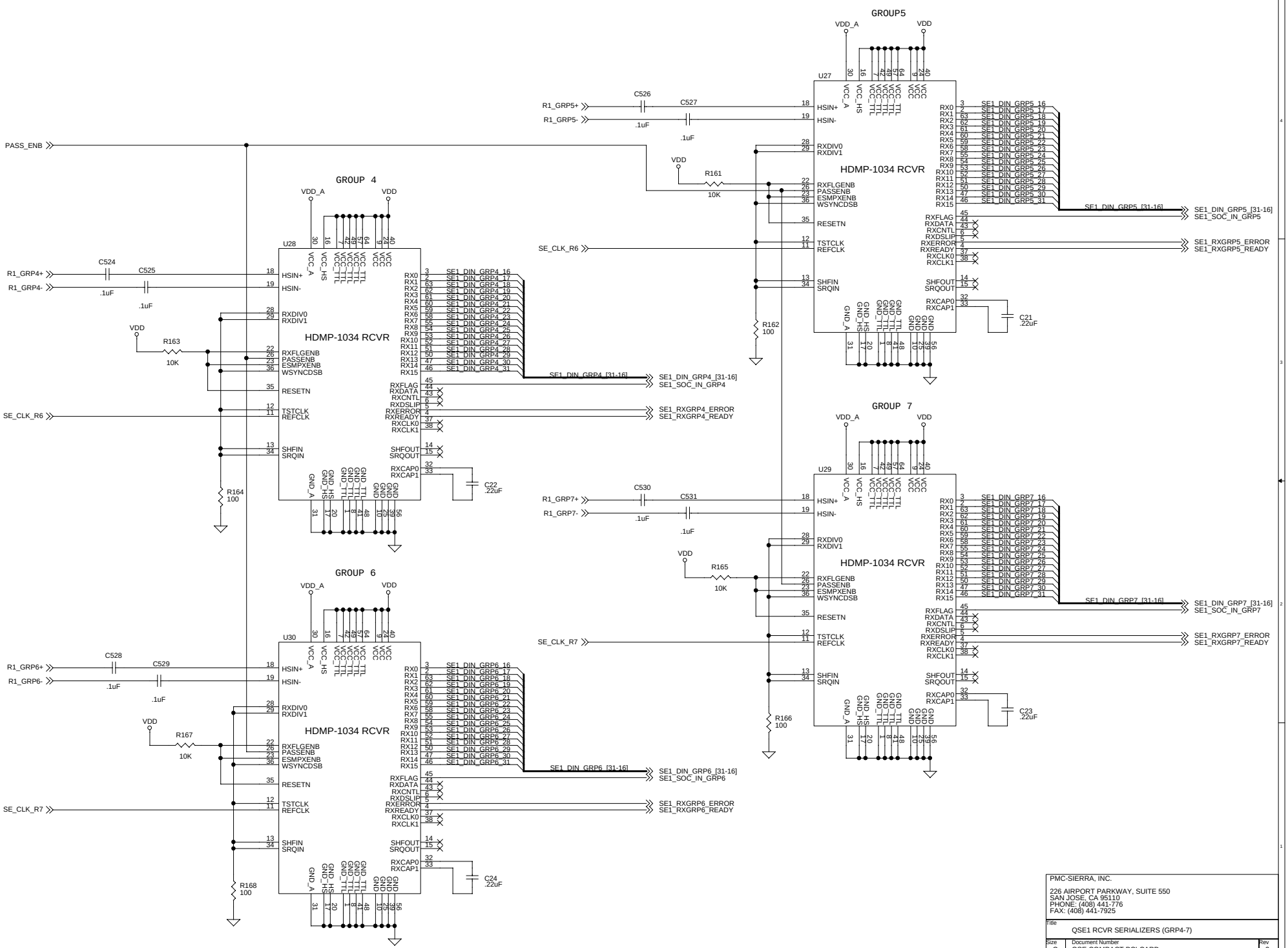
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title	QSE1 CPU & MULTICAST CKT
Size	C
Document Number	QSE COMPACT PCI CARD
Rev	2
Date:	Monday, October 11, 1999
Sheet	17 of 28



PMC-SIERRA, INC.	
226 AIRPORT PARKWAY, SUITE 550 SAN JOSE, CA 95110 PHONE: (408) 441-776 FAX: (408) 441-7925	
Title	QSE1 RCVR SERIALIZERS (GRP0-3)
Size: C	Document Number: QSE COMPACT PCI CARD
Rev: 2	
Date: Monday, October 11, 1999	Sheet 18 of 28



PMC-SIERRA, INC.

226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-776
FAX: (408) 441-7925

Title: QSE1 RCVR SERIALIZERS (GRP4-7)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 19 of 28

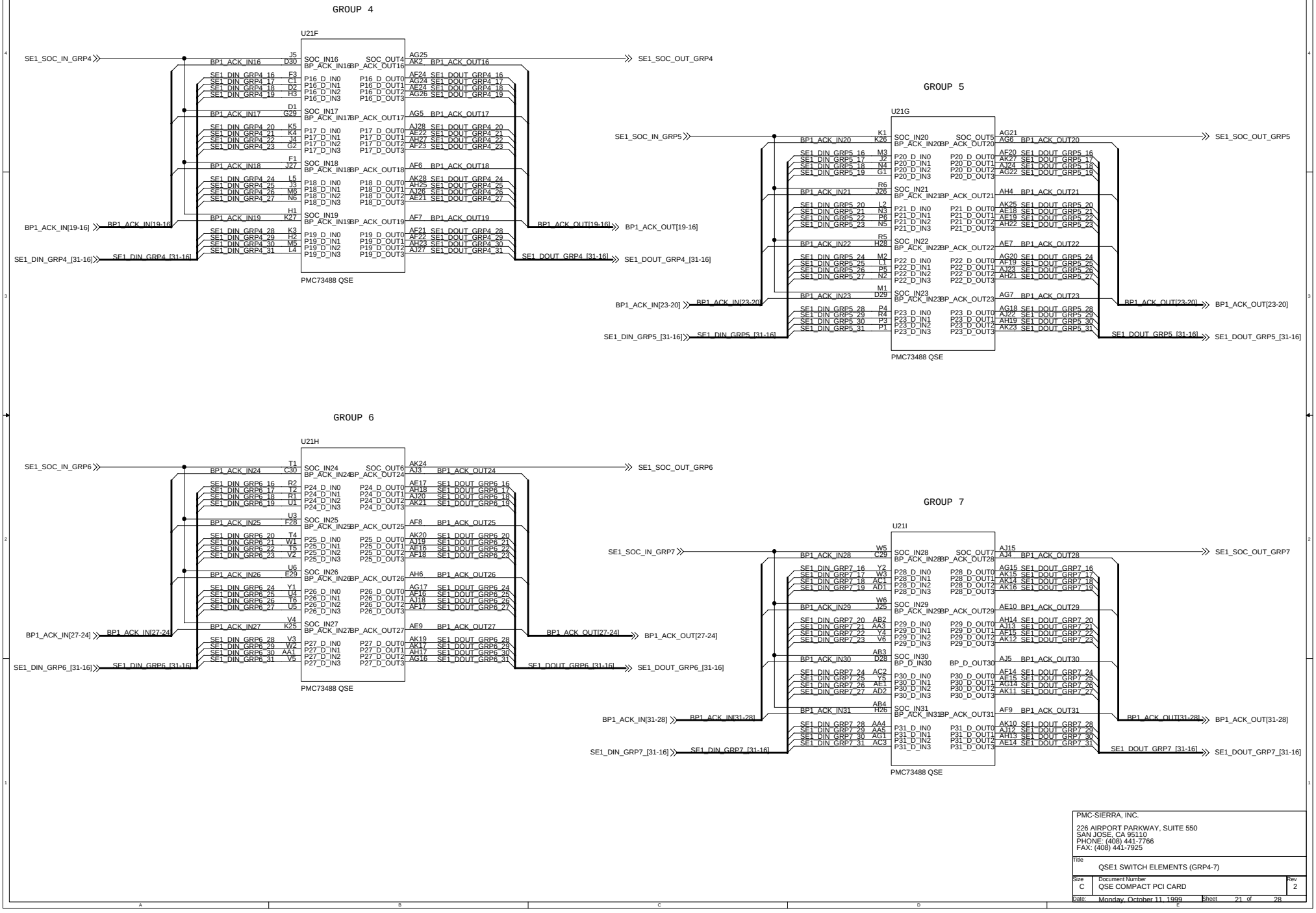
PMC-SIERRA, INC.

226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: QSE1 SWITCH ELEMENTS (GRP0-3)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 20 of 28


GROUP 4
U21F
SE1_SOC_IN_GRP4
SE1_SOC_OUT_GRP4
BP1_ACK_IN[19-16]
BP1_ACK_OUT[19-16]
SE1_DIN_GRP4_[31-16]
SE1_DOUT_GRP4_[31-16]
PMC73488 QSE
GROUP 5
U21G
SE1_SOC_IN_GRP5
SE1_SOC_OUT_GRP5
BP1_ACK_IN[23-20]
BP1_ACK_OUT[23-20]
SE1_DIN_GRP5_[31-16]
SE1_DOUT_GRP5_[31-16]
PMC73488 QSE
GROUP 6
U21H
SE1_SOC_IN_GRP6
SE1_SOC_OUT_GRP6
BP1_ACK_IN[27-24]
BP1_ACK_OUT[27-24]
SE1_DIN_GRP6_[31-16]
SE1_DOUT_GRP6_[31-16]
PMC73488 QSE
GROUP 7
U21I
SE1_SOC_IN_GRP7
SE1_SOC_OUT_GRP7
BP1_ACK_IN[31-28]
BP1_ACK_OUT[31-28]
SE1_DIN_GRP7_[31-16]
SE1_DOUT_GRP7_[31-16]
PMC73488 QSE
PMC-SIERRA, INC.
226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925
Title
QSE1 SWITCH ELEMENTS (GRP4-7)
Size
C
Document Number
QSE COMPACT PCI CARD
Rev
2
Date:
Monday, October 11, 1999
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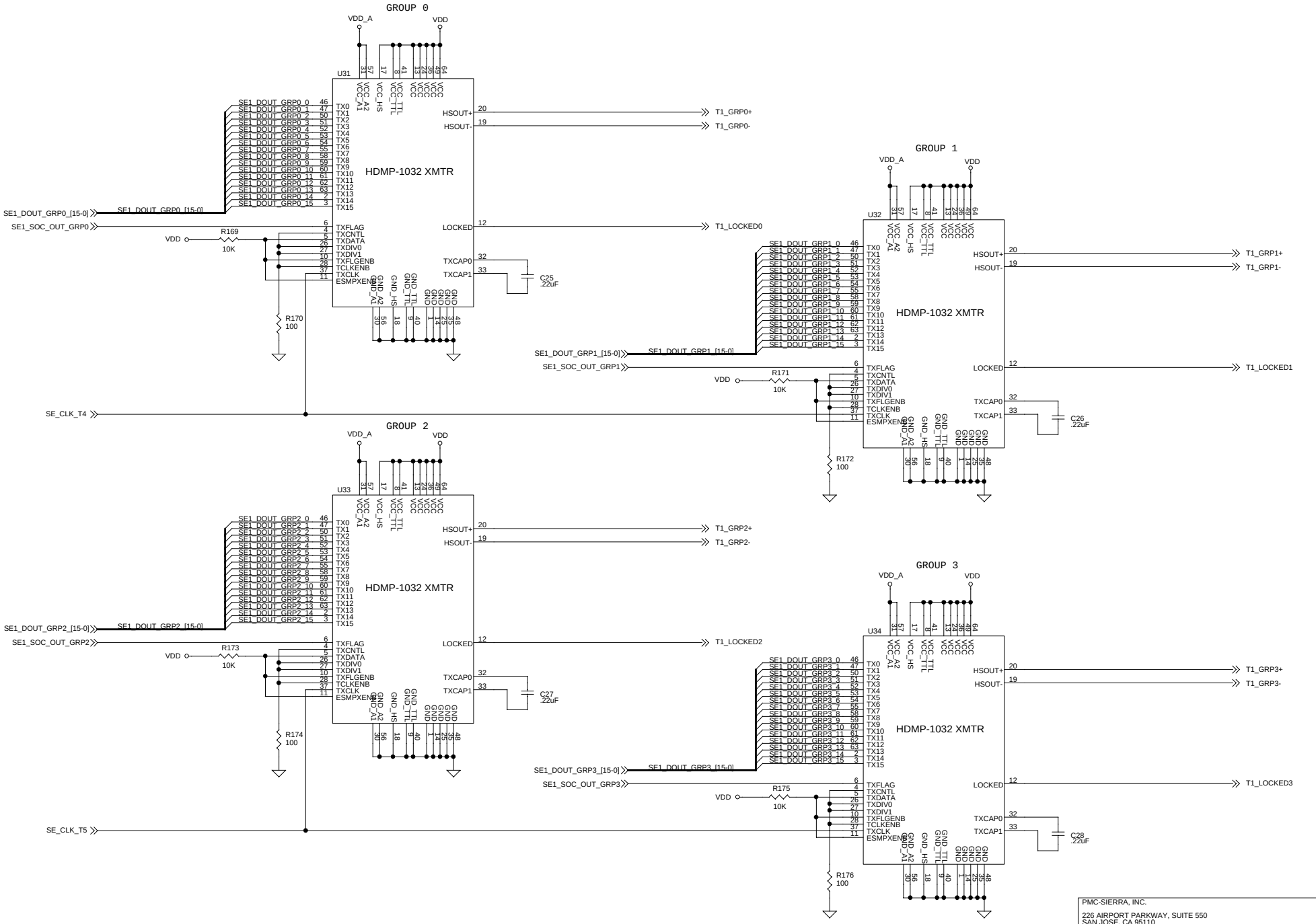
21
of
28



PMC-SIERRA, INC.

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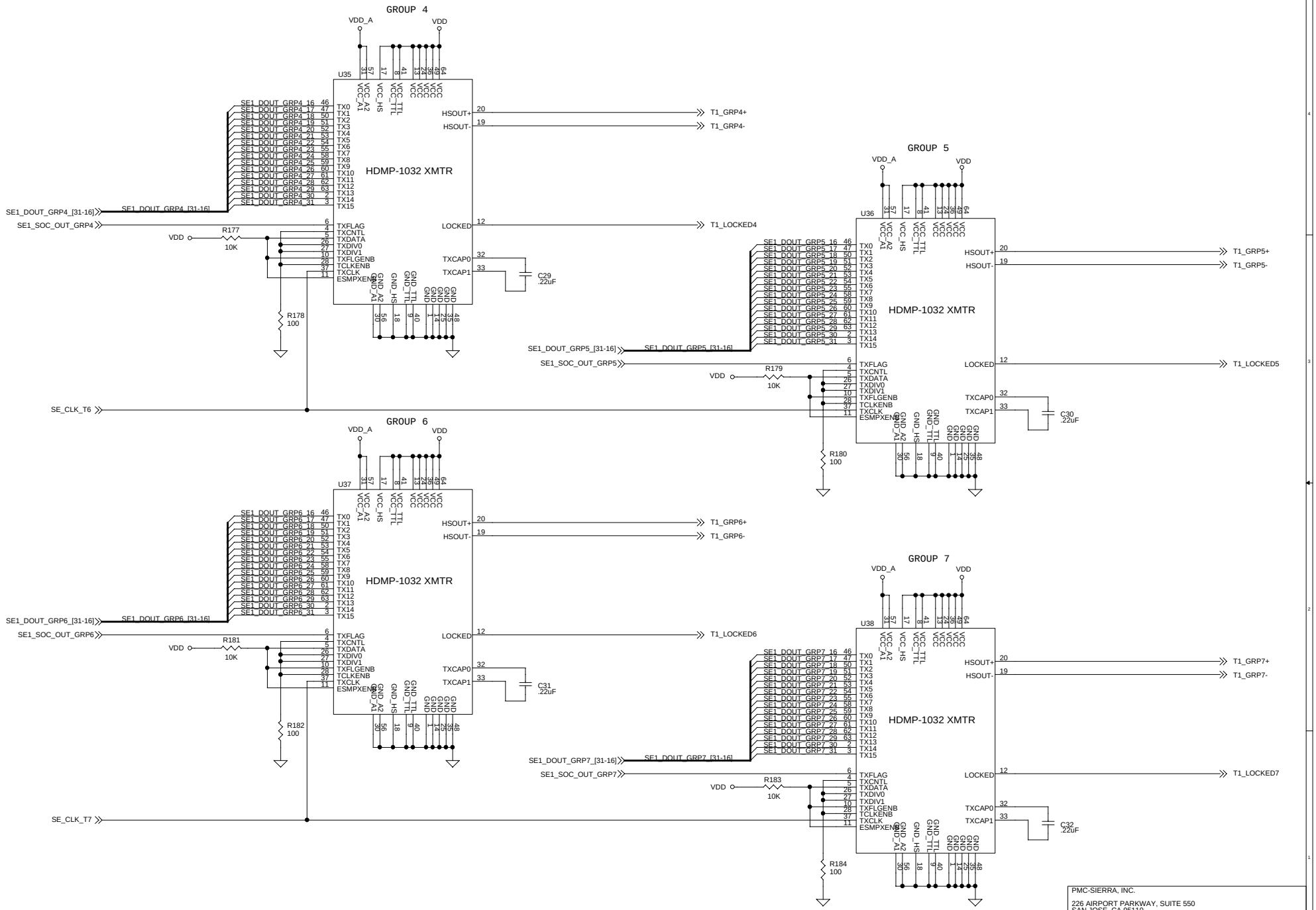
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: QSE1 XMTR SERIALIZERS (GRP0-3)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 22 of 28



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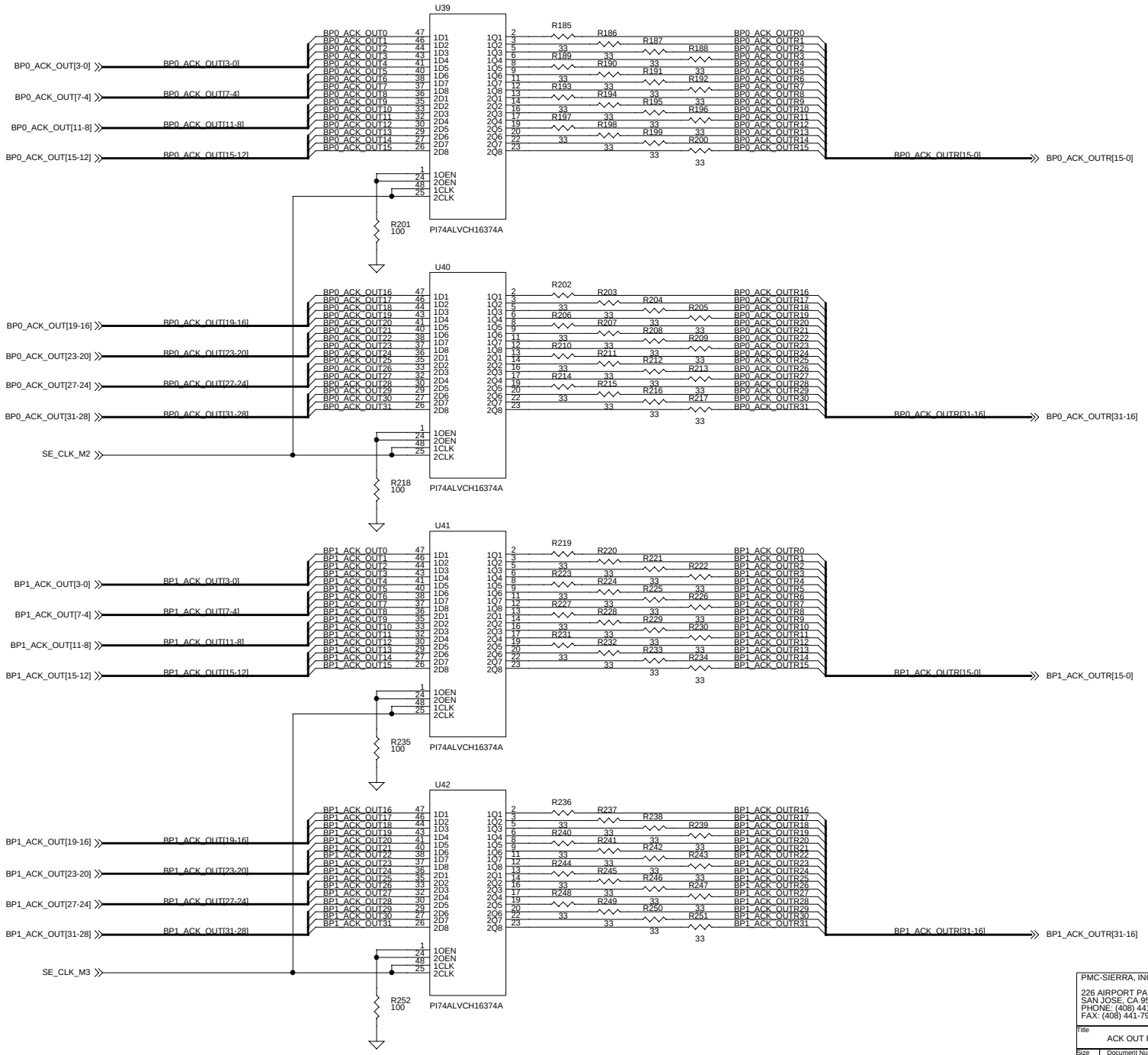
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: QSE1 XMTR SERIALIZERS (GRP4-7)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 23 of 28



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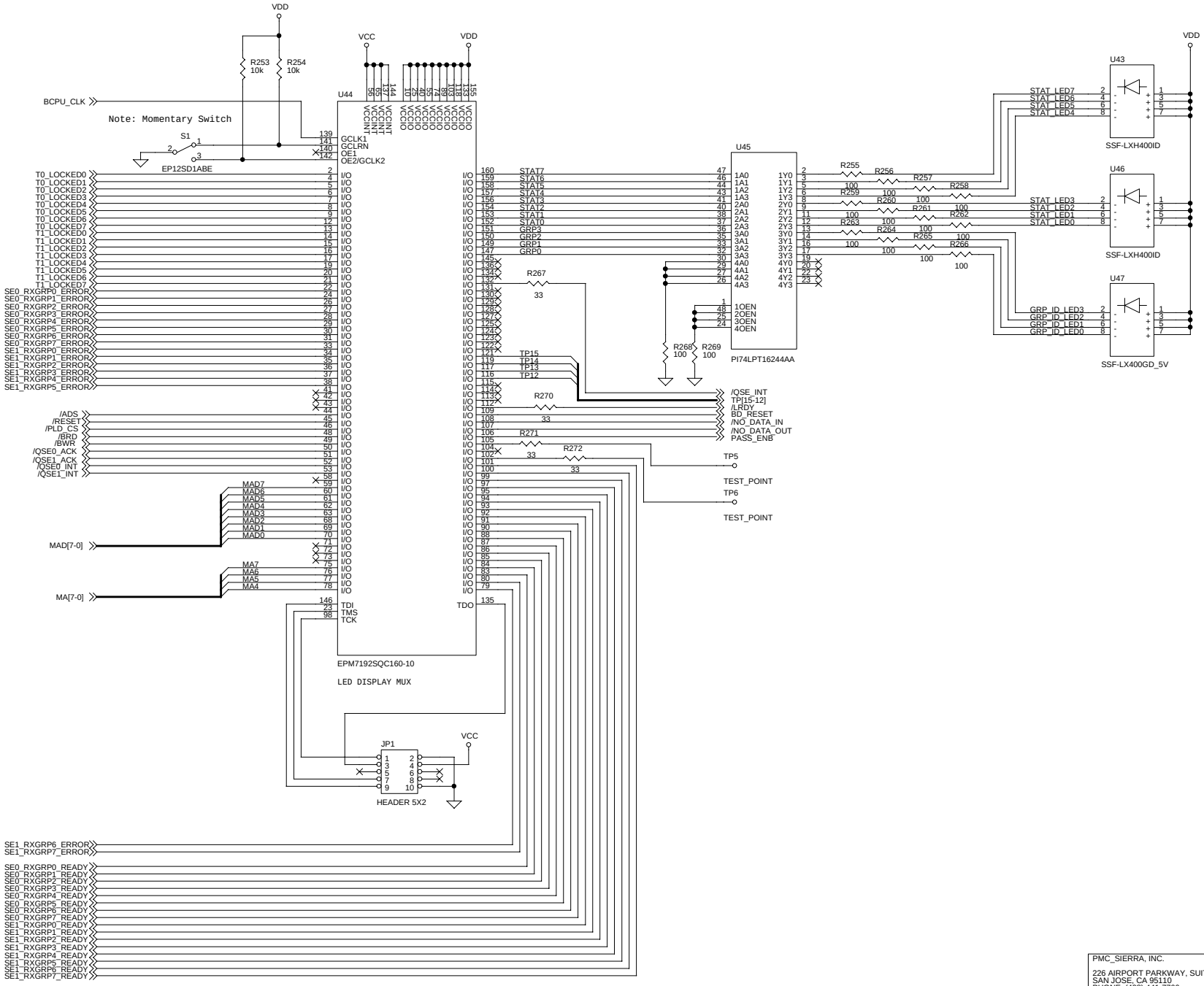
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

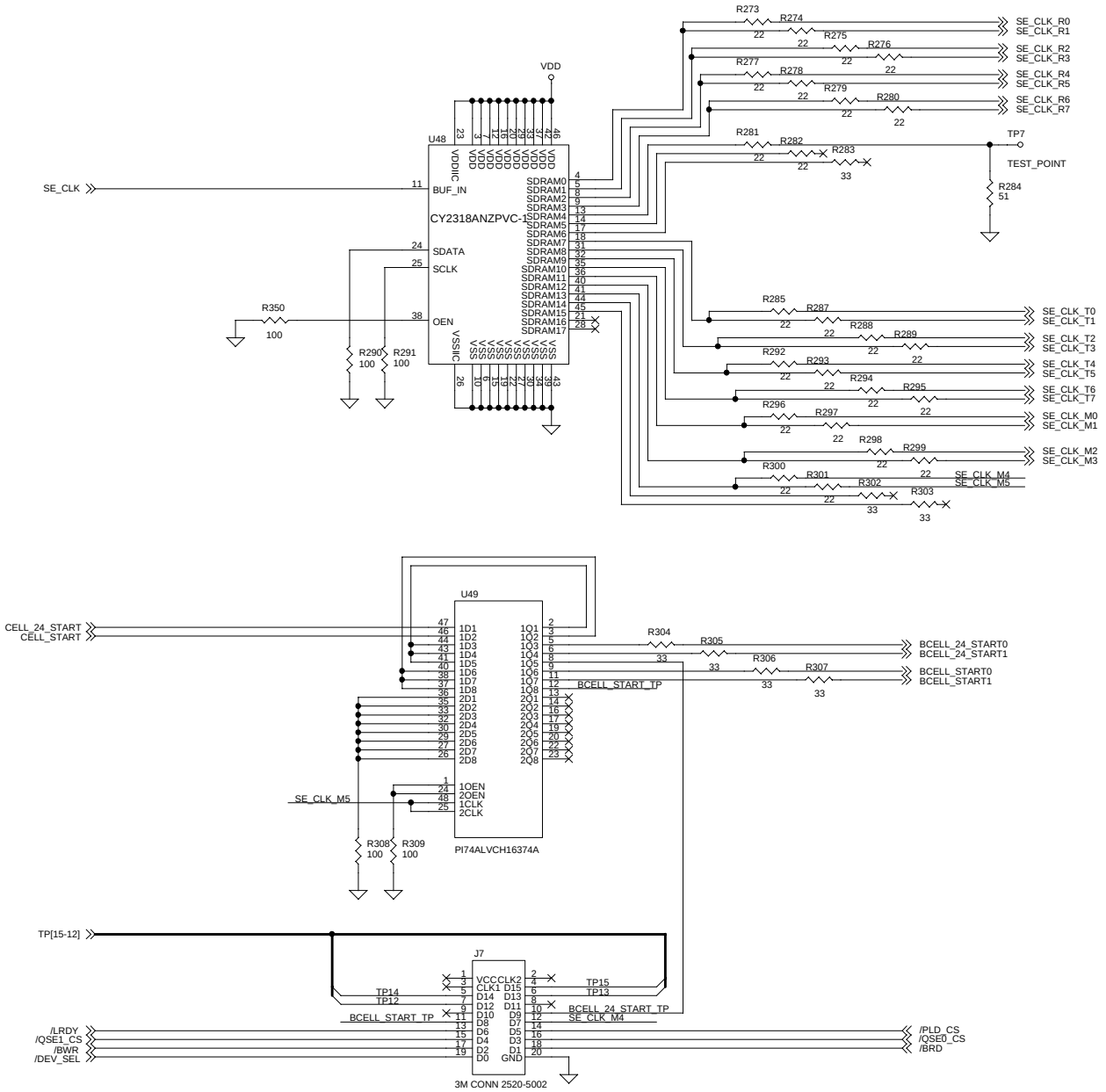
Title: ACK OUT REGISTERS

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 24 of 28



PMC_SIERRA, INC.	
226 AIRPORT PARKWAY, SUITE 550 SAN JOSE, CA 95110 PHONE: (408) 441-7766 FAX: (408) 441-7925	
Title: LED DISPLAY	
Size: C	Document Number: QSE COMPACT PCI CARD — Rev: 2
Date: Monday, October 11, 1999	Sheet 25 of 28

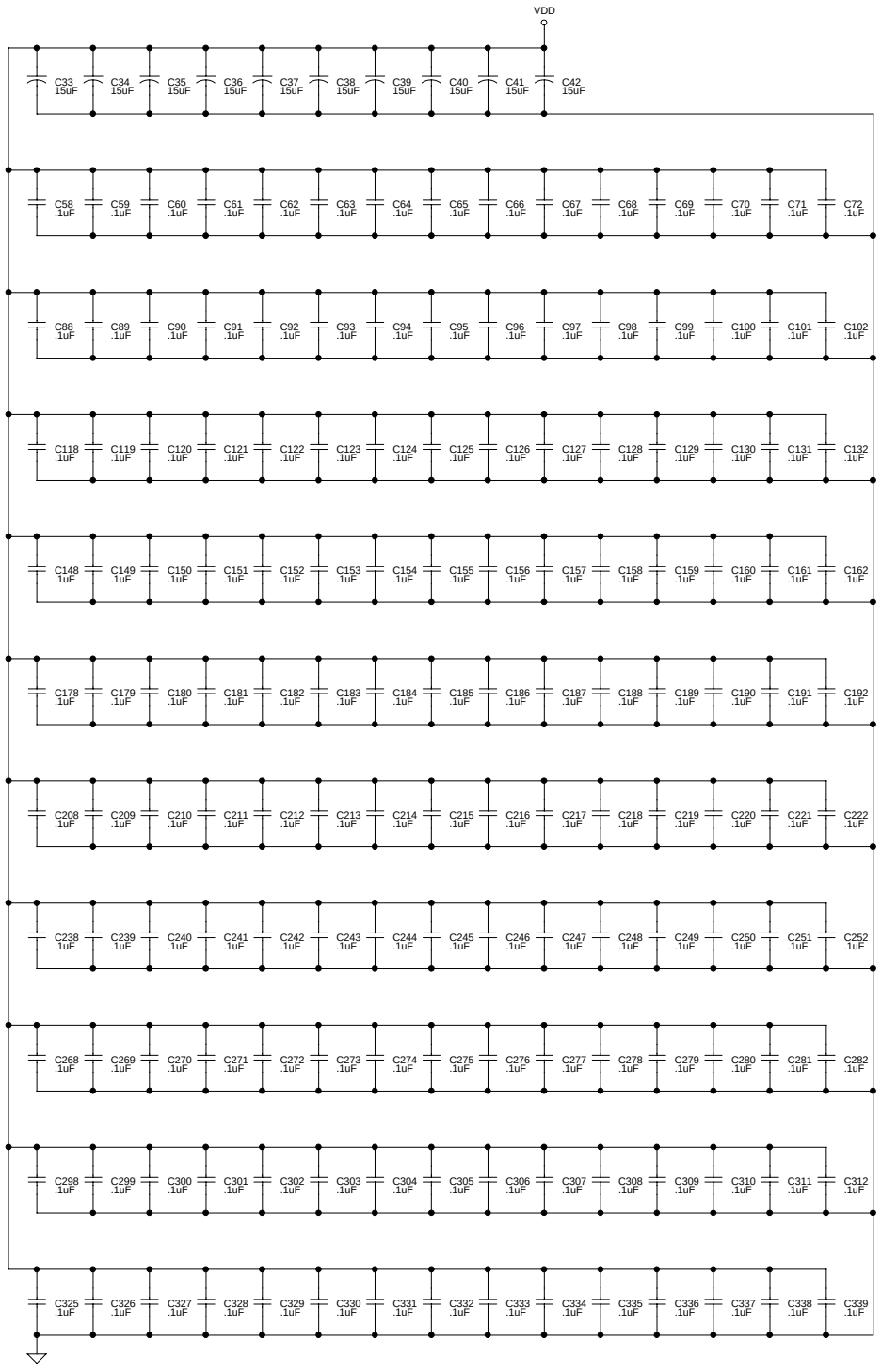


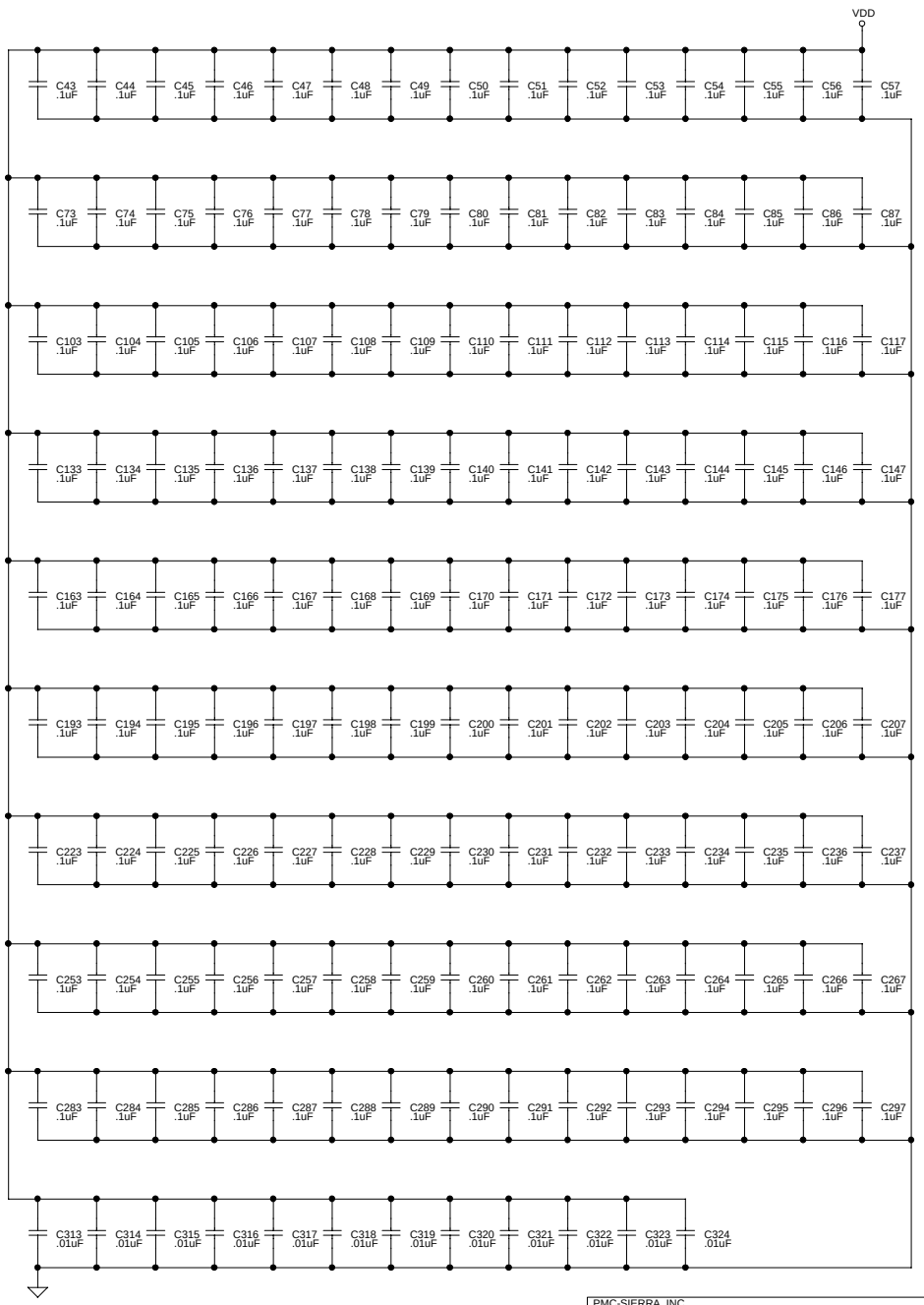
LOGIC ANALYZER CONN

PMC-SIERRA, INC.

226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title	MISC CIRCUITS	
Size: C	Document Number: QSE COMPACT PCI CARD	Rev: 2
Date: Monday, October 11, 1999	Sheet 26 of 28	





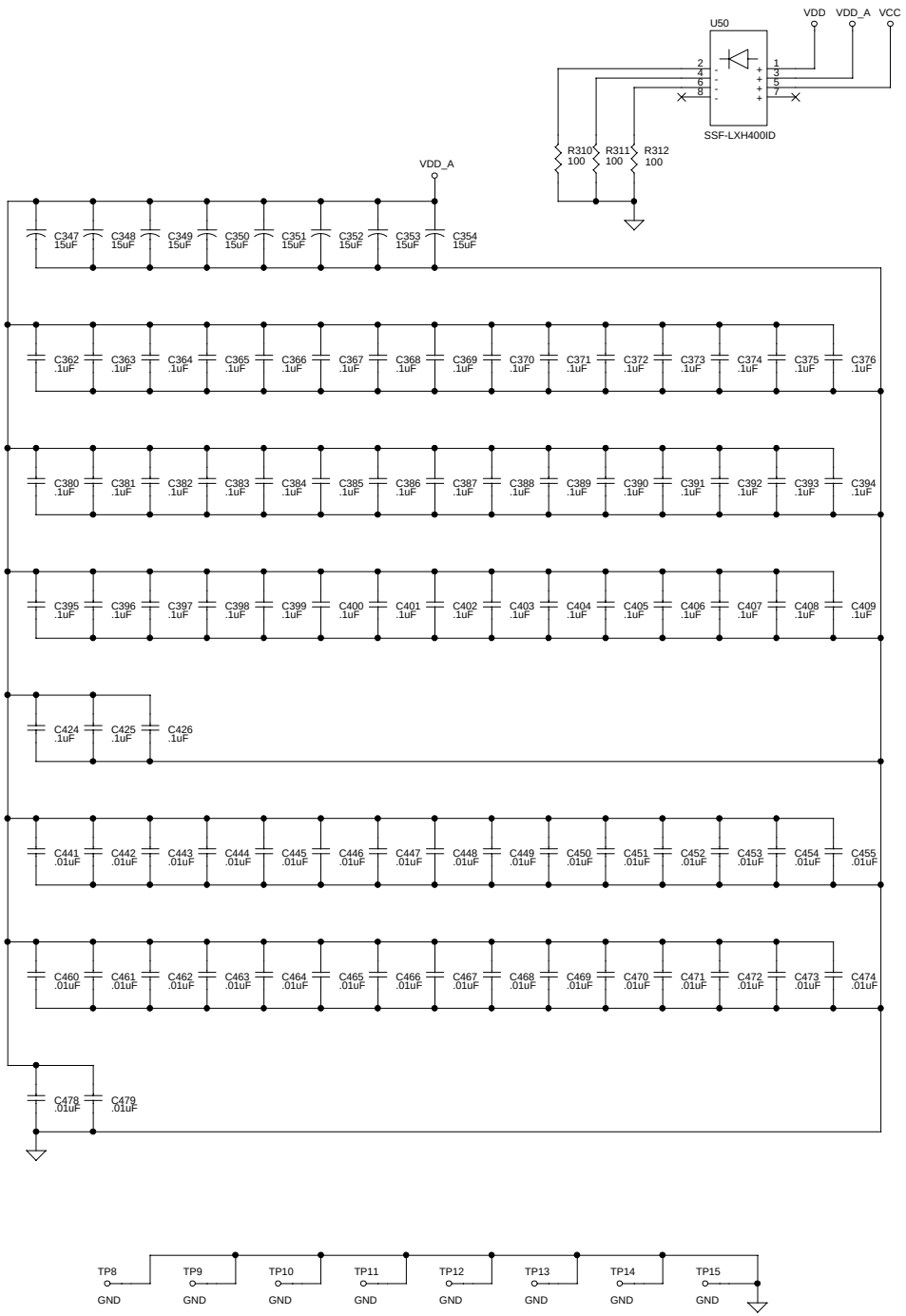
PMC-SIERRA, INC.

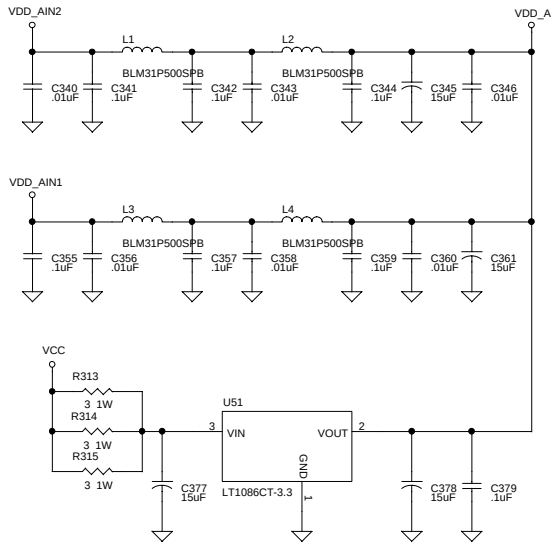
226 AIRPORT PARKWAY, SUITE 550
SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: POWER (VDD)

Size: C | Document Number: QSE COMPACT PCI CARD | Rev: 2

Date: Monday, October 11, 1999 | Sheet 27 of 28

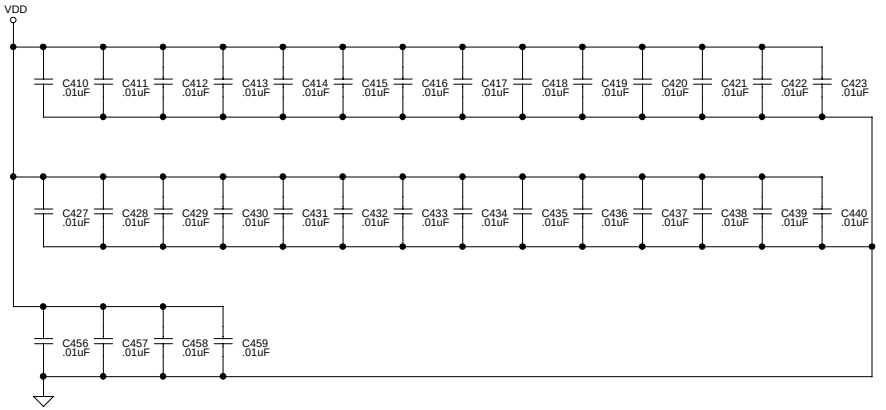


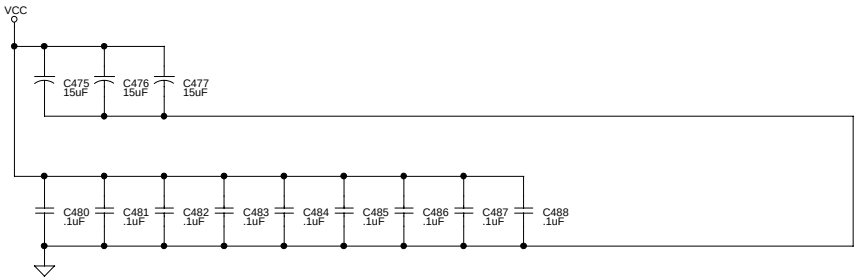


DEVICE BYPASS CAP GUIDLINES

Notes: VDD
- 8 .1uF CAP per 1032
- 1 .01uF CAP per 1032
- 7 .1uF CAP per 1034
- 1 .01uF CAP per 1034
- 6 .1uF cap per QSE
- 4 .01uF CAP per QSE
- 2 .1uF CAP per RAM
- 2 .01uF CAP per RAM
- 4 .1uF CAP per PLD
- 2 .1uF CAP per 16XXX
- 2 .1uF CAP per 3807

Notes: VDD_A
- 2 .1uF CAP per 1034
- 1 .01uF CAP per 1034
- 1 .1uF CAP per 1032
- 1 .01uF CAP per 1032





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SAN JOSE, CA 95110
PHONE: (408) 441-7766
FAX: (408) 441-7925

Title: POWER (VDD_A)		
Size: C	Document Number: QSE COMPACT PCI CARD	Rev: 2
Date: Monday, October 11, 1999	Sheet 28 of 28	

10 BILL OF MATERIALS

Table 1 - Bill of Materials

Item	Quantity	Reference	Part Number	Source	Description
1	32	C1 – C32	LMK107BJ224KA	TAIYO YUDEN	.22uF 10V 10% XR5 CER CAP 0603
2	25	C33 -C42, C345, C347 - C354, C361, C377, C378, C475 - C477	ECS-T1AX156	PANASONIC	15uF 10V 10% TANT. CAP B
3	381	C43 - C409, C424 - C426 C531	EMK107BJ104KA	TAIYO YUDEN	1uF 10V 10% X7R CER. CAP 0603
4	82	C313 - C324, C340,C343, C346,C356, C358,C360, C410 - C423,C427 - C474, C478,C479	ECU-V1H103KBV	PANASONIC	01uF 50V 10% CER. CAP 0603
5	1	JP1	PZC36DAAN	SULLINS	.025" SQUARE DOUBLE STRAIGHT HEADER
6	5	J2 – J6	120673-1	AMP	60 POS. 6-ROW ZPACK HS3
7	1	J7	2520-5002UB	3M	.100" X 100" RIGHT ANGLE 20PIN LOW PRO. HEADER
8	4	L1 – L4	BLM31P500SPB	MURATA	50 OHM IMPEDENCE FERRITE BEAD 1206
9	1	P1	352068-1	AMP	110 POS. TYPE B ZPACK

Item	Quantity	Reference	Part Number	Source	Description
10	91	R1 – R32, R62 – R69, R89 - R111, R114,R116, R118,R120, R122,R124, R126,R128, R130,R132, R134,R136, R138,R140, R142,R144, R148,R150, R153,R155, R157,R159, R161,R163, R165,R167, R169,R171, R173,R175, R177,R179, R181,R183, R253,R254	ERJ-3GSYJ10KV	PANASONIC	10K 1/16W 5% CHIP RES. 0603
11	48	R33 – R61, R70 - R88	ERJ-3GSYJ10V	PANASONIC	10 1/16W 5% CHIP RES. 0603
12	65	R101,R105, R106,R112, R113, R115,R117, R119,R121, R123,R125, R127,R129, R131,R133, R135,R137, R139,R141, R143,R145, R151,R152, R154,R156, R158,R160, R162,R164, R166,R168, R170,R172, R174,R176, R178,R180, R182,R184, R201,R218, R235,R252, R255 – R266,R268, R269,R290, R291, R308 - R312,R350	ERJ-3GSYJ100V	PANASONIC	100 1/16W 5% CHIP RES. 0603

Item	Quantity	Reference	Part Number	Source	Description
13	83	R102,R103, R107,R108, R110,R146, R147,R149, R185 - R200,R202, - R217,R219, R220 - R234,R236, R237 - R251,R267, R270,R271, R272,R283, R302,R303, R304,R305, R306,R307	ERJ-3GSYJ33V	PANASONIC	33 1/16W 5% CHIP RES. 0603
14	24	R273 - R282,R285, R287,R288, R289,R292, - R301	ERJ-3GSYJ22V	PANASONIC	22 1/16W 5% CHIP RES. 0603
15	1	R284	ERJ-3GSYJ51V	PANASONIC	51 1/16W 5% CHIP RES. 0603
16	3	R313,R314, R315	P3W-1TR-ND	DIGI-KEY	1W 5% METAL OXIDE FILM RES
17	1	S1	EP12SD1ABE	C&K	SPDT PUSHBUTTON SWITCH
18	7	TP1 – TP7	PZC36SAAN	SULLINS	.025" SQUARE SINGLE STRAIGHT HEADER
19	8	TP8 – TP15	PZC36SAAN	SULLINS	.025" SQUARE SINGLE STRAIGHT HEADER
20	1	U1	PCI 9050-1	PLX TECHNOLOGY	PCI BUS TARGET INTERFACE CHIP
21	1	U2	NM93CS46EN	FAIRCHILD	1024-BIT SERIAL EEPROM 8-PIN DIP
22	2	U3, U21	PM73488	PMC-Sierra, Inc	QUAD-SWITCH ELEMENT 596-PIN BGA
23	2	U4,U22	MT58LC128K18C 5LG-10	MICRON	28K X 18 SYNCBURST SRAM 100-PIN TQFP
24	16	U5 – U12, U23 – U30	HDMP-1034	HP	1.44GBD RECEIVER 64-PIN PQFP
25	16	U13 - U20, U31- U38	HDMP-1032	HP	1.44GBD TRANSMITTER 64-PIN PQFP
26	5	U39 - U49	PI74ALVCH16374 A	PERICOM	16-BIT EDGE TRIGGERED D-TYPE FLIP-FLOP 48-PIN TSSOP

Item	Quantity	Reference	Part Number	Source	Description
27	3	U43,U46, U50	SSF-LXH400ID		
28	1	U44	EPM7192SQC160 -10	ALTERA	PROGRAMMABLE LOGIC DEVICE 160-PIN PQFP
29	1	U45	PI74LPT16244AA	PERICOM	16-BIT BUFFER/LINE DRIVER 48-PIN TSSOP
30	1	U47	SSF-LX400GD_5V		
31	1	U48	CY2318ANZPVC-1	CYPRESS	18 OUTPUT, 3.3V SDRAM BUFFER 48 PIN SSOP
32	1	U51	LT1086CT-3.3	LINEAR TECHNOLOGY	1.5A LOW DROPOUT POS. REG. ADJTABLE TO-220

11 PLD CONTENTS

The following VHDL code is implemented in the LED_DSP PLD device. This device is an Altera 7000 family device.

```
-- ************************************************************************
-- The following VHDL code and related files are proprietary information of
■                                   PMC _Sierra
-- ************************************************************************
-- This PLD incorporates the following functions
--
-- LED DISPLAY
--      It will display 8 status inputs at a time on the status LEDs.
--      The GROUP LEDS will display which of the 8 groups are being displayed
--      GROUP 0     -QSE 0 XMTR   LOCKED LED 7-0
--      GROUP 1     -QSE 0 RCVR   ERROR  LED 7-0
--      GROUP 2     -QSE 0 RCVR   READY  LED 7-0
--      GROUP 3     -QSE 1 XMTR   LOCKED LED 7-0
--      GROUP 4     -QSE 1 RCVR   ERROR  LED 7-0
--      GROUP 5     -QSE 1 RCVR   READY  LED 7-0
--      GROUP 6     -ANY ERROR IN ANY OF THE 6 groups for that bit
--      GROUP 7     -ANY ERROR IN ANY OF THE 6 groups for that bit

-- CARD Control Register at addr 00
--      7           Not used
--      6           Not used
--      5           Not used
--      4           Not used
--      3           Not used
--      2-0         Group Select for readback

-- Mask Register  at addr 10
--      7           Not used
--      6           Not used
--      5           Not used
--      4           Not used
--      3           QSE1 ACK MASK
--      2           QSE0 ACK MASK
--      1           QSE1 INT MASK
--      0           QSE0 INT MASK

-- LED Status Register  at addr 20
--      7-0         Displays group selected by register 10
-- The pushbutton switch will run a 3 bit counter that will be used
```

- to select one of the groups for LED display
-

```
-- Not Implemented yet
--          Latches on the LEDs


------------------------------------------------------------------
LIBRARY std;
use std.all;

LIBRARY ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.CONV_INTEGER;
USE ieee.std_logic_arith.CONV_STD_LOGIC_VECTOR;
entity led_dsp is

 port(
          -- Timing signals
          clk_in:          in std_logic;
          -- For uP access
          reset_n:         in std_logic;
          cs_n:            in std_logic;
          wr_n:            in std_logic;
          rd_n:            in std_logic;
          data:            inout std_logic_vector(7 downto 0);
          addr:            in std_logic_vector(7 downto 4);
          ads_n:           in std_logic;      -- not used, since addr is not multiplexed
          switch_nc:       in std_logic;
          switch_no:       in std_logic;
          q0_t_locked:     in std_logic_vector(7 downto 0);
          q0_r_error:      in std_logic_vector(7 downto 0);
          q0_r_ready:      in std_logic_vector(7 downto 0);
          q1_t_locked:     in std_logic_vector(7 downto 0);
          q1_r_error:      in std_logic_vector(7 downto 0);
          q1_r_ready:      in std_logic_vector(7 downto 0);
          led_data_n:      out std_logic_vector(7 downto 0);
          led_grp_n:       out std_logic_vector(2 downto 0);
          led_grp3_n:      out std_logic;
          bd_reset:        out std_logic;
          nodata_out_n:    out std_logic;
          nodata_in_n:     out std_logic;
          pass_enb:        out std_logic;

          qse0_int_n:      in std_logic;
          qse1_int_n:      in std_logic;
```

```
        qse0_ack_n:     in std_logic;
        qse1_ack_n:     in std_logic;


        qse_int_n:      out std_logic;
        ack_n:          out std_logic
 );
end led_dsp;
architecture rtl of led_dsp is
        signal l_mux_out:       std_logic_vector(7 downto 0);
        signal r_mux_out:       std_logic_vector(7 downto 0);

        signal led_sel:         std_logic_vector(2 downto 0);
        signal read_sel:        std_logic_vector(2 downto 0);
        signal data_reg:        std_logic_vector(7 downto 0);
        signal mask_reg:        std_logic_vector(3 downto 0);

        signal cs:              std_logic;
        signal wr_clk:          std_logic;
        signal drive_bus:       std_logic;
        signal cntr_clk:        std_logic;
        signal load:            std_logic;
        signal advance_latq:    std_logic;
        signal advance_latq_n:  std_logic;
        signal err:             std_logic_vector(7 downto 0);
        signal qse0_int_mask:   std_logic;
        signal qse1_int_mask:   std_logic;
        signal qse0_ack_mask:   std_logic;
        signal qse1_ack_mask:   std_logic;
        signal qse_int:         std_logic;
        signal qse0_ack:        std_logic;
        signal qse1_ack:        std_logic;
        signal ack:             std_logic;

begin
        -- concurrent assignments
        led_data_n <=  not(l_mux_out);
        led_grp_n  <=  not(led_sel);
        led_grp3_n <= '1';          -- not used led
        -- for now
        cntr_clk <= advance_latq;
        load <= cs;
        bd_reset <= data_reg(7);
        nodata_out_n <= data_reg(6);
        nodata_in_n <= data_reg(5);
        pass_enb <= data_reg(4);
```

```
        read_sel <= data_reg(2 downto 0);
        qse0_int_mask <= mask_reg(0);
        qse1_int_mask <= mask_reg(1);
        qse0_ack_mask <= mask_reg(2);
        qse1_ack_mask <= mask_reg(3);
        -- interrupt equation
        qse_int <= (not(qse0_int_n) and not(qse0_int_mask)) or
                        (not(qse1_int_n) and not(qse1_int_mask));

        qse_int_n <= not(qse_int);

-- ack equation
        qse0_ack <= not(qse0_ack_n);
        qse1_ack <= not(qse1_ack_n);

        ack <= (qse0_ack and not qse0_ack_mask) or
                        (qse1_ack and not qse1_ack_mask);

        cs <= not cs_n;
        wr_clk    <= '1' when (cs = '1' and wr_n = '0') else '0';
        drive_bus <= '1' when (cs = '1' and rd_n = '0') else '0';

        -- hook up the cross coupled nand gates for the switch debouncer
        advance_latq <= switch_nc nand advance_latq_n;
        advance_latq_n <= switch_no nand advance_latq;

        -- For write cycle...
        -- 1) Chip selected
        -- 2) Write cycle

        -- process(wr_clk, reset_n)
                process(wr_clk)
                begin
--              if reset_n = '0' then
--                      data_reg(7 downto 0) <= "00000000";
--                      mask_reg(3 downto 0) <= "0000";
--              elsif wr_clk'EVENT and wr_clk = '1'  then
                if wr_clk'EVENT and wr_clk = '1'  then
                        case addr(5 downto 4) is
                                when "00" =>
                                        data_reg(7 downto 0) <= data(7 downto 0);
                                when "01" =>
                                        mask_reg(3 downto 0) <= data(3 downto 0);
                                when others =>null;
                        end case;
                end if;
```

```
        end process;

--      Implement the LED MUX

process(q0_t_locked, q0_r_error, q0_r_ready, q1_t_locked, q1_r_error, q1_r_ready, read_sel, err,
led_sel)

        begin

                -- implement led driver mux
                case led_sel(2 downto 0) is
                        when "000" =>
                                l_mux_out <= q0_t_locked;
                        when "001" =>
                                l_mux_out <= q0_r_error;
                        when "010" =>
                                l_mux_out <= q0_r_ready;
                        when "011" =>
                                l_mux_out <= q1_t_locked;
                        when "100" =>
                                l_mux_out <= q1_r_error;
                        when "101" =>
                                l_mux_out <= q1_r_ready;
                        when others =>
                                l_mux_out <= err;
                end case;


                -- implement read back mux
                case read_sel(2 downto 0) is
                        when "000" =>
                                r_mux_out <= q0_t_locked;
                        when "001" =>
                                r_mux_out <= q0_r_error;
                        when "010" =>
                                r_mux_out <= q0_r_ready;
                        when "011" =>
                                r_mux_out <= q1_t_locked;
                        when "100" =>
                                r_mux_out <= q1_r_error;
                        when "101" =>
                                r_mux_out <= q1_r_ready;
                        when others =>
                                r_mux_out <= err;
                end case;
        end process ;
```

```
-- implement the 3 bit counter which is driven by the pushbutton
-- by the momentary switch. It will rollover after 7.

--      process(cntr_clk, reset_n)
        process(cntr_clk)
        begin
--              if reset_n = '0' then
--                      led_sel <= "000";
--              elsif cntr_clk'EVENT and cntr_clk = '1' then
                if cntr_clk'EVENT and cntr_clk = '1' then
                        led_sel(2 downto 0) <=
                        CONV_STD_LOGIC_VECTOR(conv_integer(led_sel) + 1 , 3);
                end if;
        end process ;


-- this process ors all of the error conditions together so they can be monitored at one time

        process(q0_r_error, q1_r_error, q0_t_locked, q1_t_locked, q0_r_ready, q1_r_ready)
        begin
        for n in 0 to 7 loop
                err(n) <= q0_r_error(n) or q1_r_error(n)
                        or (not q0_t_locked(n)) or (not q1_t_locked(n))
                        or (not q0_r_ready(n)) or (not q1_r_ready(n));
                end loop;
        end process ;

-- drive ad bus on read cycles
        process(drive_bus, r_mux_out, data_reg, addr, mask_reg)
        begin
                if drive_bus = '1' and addr(5 downto 4) = "00"  then
                        data(7 downto 0) <= data_reg;
                elsif  drive_bus = '1' and addr(5 downto 4) = "01"   then
                        data(7 downto 0) <= "0000" & mask_reg;
                elsif  drive_bus = '1' and addr(5 downto 4) = "10"   then
                        data(7 downto 0) <= r_mux_out;
                else
                        data(7 downto 0) <= "ZZZZZZZZ";
                end if;
        end process;

--=========================================================
        -- cpu clock process
        -- this process synchronizes the ack to the cpci_clk
        process( clk_in )
        begin
```

```
            if clk_in'event and clk_in = '1' then
                ack_n <= not(ack);
            end if;
        end process ;

end rtl;
```

NOTES

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