

PM5356

S/UNI-622-MAX

**SATURN USER NETWORK INTERFACE
(622-MAX)**

ERRATA

ISSUE 5: APRIL 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
5	April 2000	This document contains errata information corresponding to the issue 5 datasheet and device revision E.
4	February 2000	This document contains errata information corresponding to the issue 5 datasheet and device revision B, including: -The revision history for datasheet issue 4. -S1 byte in transmit direction does not work for non-zero value.
3	September 1999	This document contains errata information corresponding to the issue 4 datasheet and device revision B.
2	July 1999	This document contains errata information corresponding to the issue 4 datasheet and device revision B.
1	Mar 1999	This document contains errata information corresponding to the issue 4 datasheet and device revision A.

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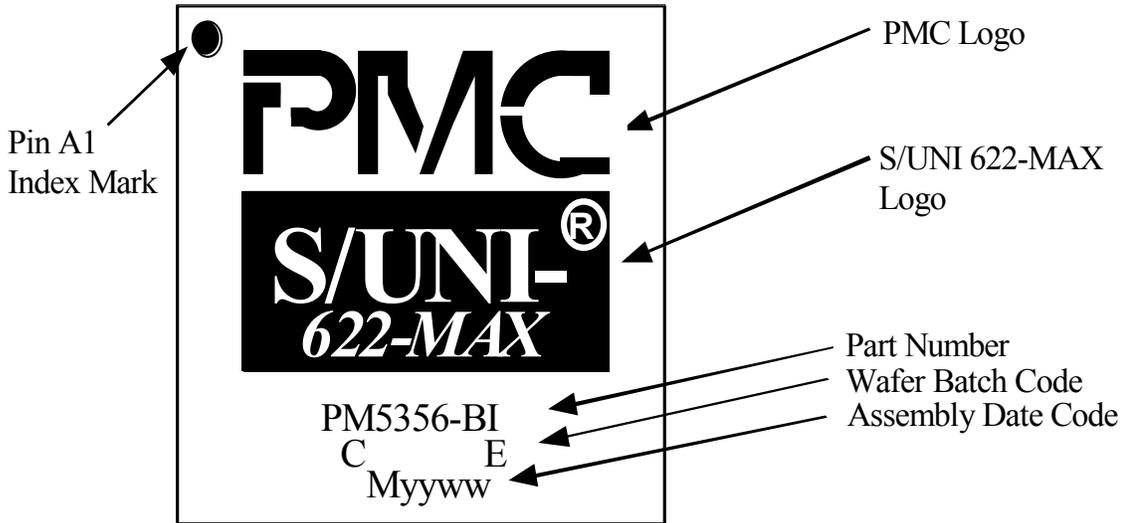
1 ISSUE 5 ERRATA

This issue 5 contains errata applied to the PMC-1980589 S/UNI-622-MAX Issue 5 datasheet. The issue 5 datasheet and issue 5 errata supersede all prior editions and versions.

1.1 Device Identification

The information contains in this document applies to the PM5356 S/UNI-622-MAX revision E device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5356 S/UNI-622-MAX revision E is packaged in a 304 pin Super BGA package.

Figure 1: PM5356 S/UNI-622-MAX Branding Format



TOP VIEW
SCALE : 2:1
(APPROX.)

2 S/UNI-622-MAX DATASHEET DISCREPANCIES

2.1 Datasheet Revision History

ISSUE	DATE	DETAIL
5	Dec, 1999	<p>#1 Modified section 9.4 (UTOPIA pin description) and section 14.2 (Functional timing) to reflect operation of the RCA signal</p> <p>#2 DC characteristics update (Section 16)</p> <p>#3 Registers updated with correct defaults and descriptions: Register 0X01, Bit 4 (TFPEN), Defaults To 1, Not 0 Register 0X08, Description Incorrect Register 0X09 Description Incorrect New Register 0XFC: Concatenation Status And Enable New Register 0XFD: Concatenation Interrupt Status New Register Bit Required For OC-3 Operation (Register 0X07) Register 0X5E Bit 5 (RTYPE) should be set to zero for improved Jitter Tolerance Register 0X00 Type Bits Incorrect Loss Of Multi-frame Tributary AIS (LOMTUAIS) Bit 2 Incorrectly Stated In Register 0X0D</p> <p>#4 APS pin description modified</p> <p>#6 Updated TFCLK timing specifications, RFCLK timing specifications</p> <p>#7 Diagnostic Loop-back Clarification</p> <p>#8 Bit Error Rate Monitor Table Update</p> <p>#9 Receive Data Requires 3 RFCLK Cycles Before Becoming Valid (Utopia Level 3 Only)</p> <p>#11 Receive Line AIS Insertion Is Not Gated By ALLONES</p> <p>#12 Large Power Supply Glitch (Beyond Specification) Can Cause Clock Synthesis Unit To Lose Lock To Reference.</p>
4	January 4, 1999	Corrected wrong pin number assignments in pin description.

ISSUE	DATE	DETAIL
3	Dec 15, 1999	General update
2	Aug 30, 1998	Re-organized registers. Removed UDF. Update pin list and block diagram. Add preliminary simulation and test sections text.
1	Jan 5, 1998	Created document

2.2 PECL Interface Resistor Value Incorrect (Section 13.11):

The pull down for 3.3V PECL interface is shown as 330 ohm. The correct recommended value is 150 ohm.

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