

RM5231A

RM5231A™ Microprocessor with 32-Bit System Bus

Data Sheet

Proprietary and Confidential

Preliminary

Issue 3, February 2002

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Revision History

Issue No.	Issue Date	Details of Change
3	February 2002	<p>Modified features list to include 400 MHz operating frequency, 560 Drystone MIPS, 800 MFLOPS floating-point unit.</p> <p>Modified system interface description to read rates of 500 Mbytes/sec with 125 MHz SysClock.</p> <p>Modified recommended operating conditions table.</p> <p>Modified power consumption table.</p> <p>Modified clock parameters table.</p> <p>Modified system interface parameters.</p> <p>Added RM5231A-400-H to the Valid Combinations.</p>
2	September 2001	<p>Added 1.8 V to the feature: 1.65 V or 1.8 V core with 3.3 V or 2.5 V I/O (p9). Changed recommended operating conditions VccInt to 1.57 V to 1.85 V and VccP to 1.57 V to 1.85 V. Added VssP commercial and industrial values. Modified Note 4.</p> <p>Added reference to VccInt to Power Consumption table. Changed standby modes to 350. Modified Note 1.</p> <p>Modified SysClock Frequency and SysClock Period values in the Clock Parameters table.</p>
1	March 2001	<p>Applied PMC-Sierra template to existing MPD (QED) FrameMaker document.</p> <p>Revised the Absolute Maximum Ratings table to include industrial operating temperatures. Revised the Recommended Operating conditions table (VccIO). Revised the DC Electrical Characteristics section. Included 350 MHz Power CPU Speed Power Consumption and Clock Parameter values. Revised the System Interface Parameters table.</p>

Document Conventions

The following conventions are used in this datasheet:

- All signal, pin, and bus names described in the text, such as **ExtRqst***, are in boldface typeface.
- All bit and field names described in the text, such as ***Interrupt Mask***, are in an italic-bold typeface.
- All instruction names, such as MFHI, are in san serif typeface.

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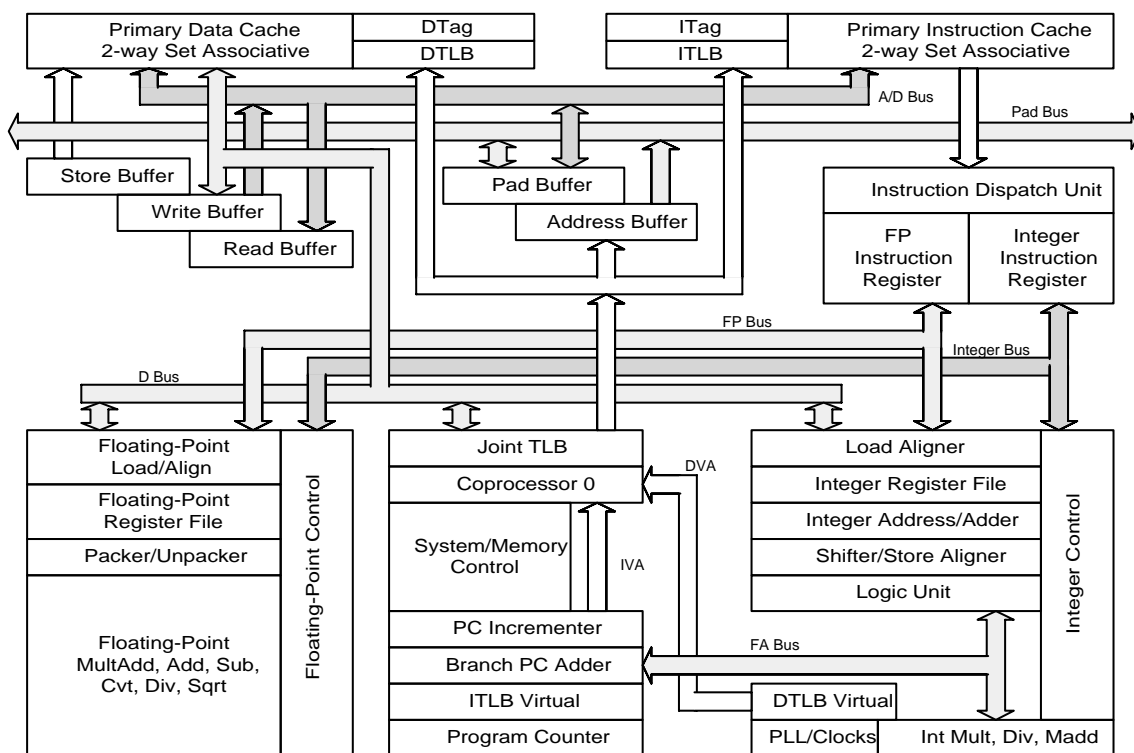
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1 Features

- Dual Issue superscalar microprocessor
 - 250, 300, 350, and 400 MHz operating frequencies
 - Up to 560 Dhrystone 2.1 MIPS
- System interface optimized for embedded applications
 - 32-bit system interface lowers total system cost
 - High-performance write protocols maximize uncached write bandwidth
 - Processor clock multipliers: 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9
 - IEEE 1149.1 JTAG boundary scan
- Integrated on-chip caches
 - 32 KB instruction and 32 KB data — 2 way set associative
 - Per set locking
 - Virtually indexed, physically tagged
 - Write-back and write-through on a per page basis
 - Pipeline restart on first doubleword for data cache misses
- Integrated memory management unit
 - Fully associative joint TLB (shared by I and D translations)
 - 48 dual entries map 96 pages
 - Variable page size (4 KB to 16 MB in 4x increments)
- High-performance floating-point unit — up to 800 MFLOPS
 - Single cycle repeat rate for common single-precision operations and some double precision operations
 - Two cycle repeat rate for double-precision multiply and double precision combined multiply-add operations
 - Single cycle repeat rate for single-precision combined multiply-add operation
- MIPS IV instruction set
 - Floating point multiply-add instruction increases performance in signal processing and graphics applications
 - Conditional moves to reduce branch frequency
 - Index address modes (register + register)
- Embedded application enhancements
 - Specialized DSP integer Multiply-Accumulate instructions and 3-operand multiply instruction
 - I and D cache locking by set
 - Optional dedicated exception vector for interrupts
- Fully static 0.18 micron CMOS design with power down logic
 - Standby reduced power mode with WAIT instruction
 - 1.65 V or 1.8 V core with 3.3 V or 2.5 V I/O
- 128-pin QFP package

2 Block Diagram

Figure 1 Block Diagram



3 Hardware Overview

The RM5231A offers a high-level of integration targeted at high-performance embedded applications. The key elements of the RM5231A are briefly described below.

3.1 Superscalar Dispatch

The RM5231A has an asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. Integer instructions include alu, branch, load/store, and floating-point load/store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, and converts. In combination with its high-throughput fully pipelined floating-point execution unit, the superscalar capability of the RM5231A provides unparalleled price/performance in computationally intensive embedded applications.

3.2 CPU Registers

The RM5231A contains 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits. Figure 2 shows the user visible state.

Figure 2 CPU Registers

General Purpose Registers

63 0

0
r1
r2
•
•
•
•
r29
r30
r31

Multiply/Divide Registers

63 0

HI
63 0
LO

Program Counter

63 0

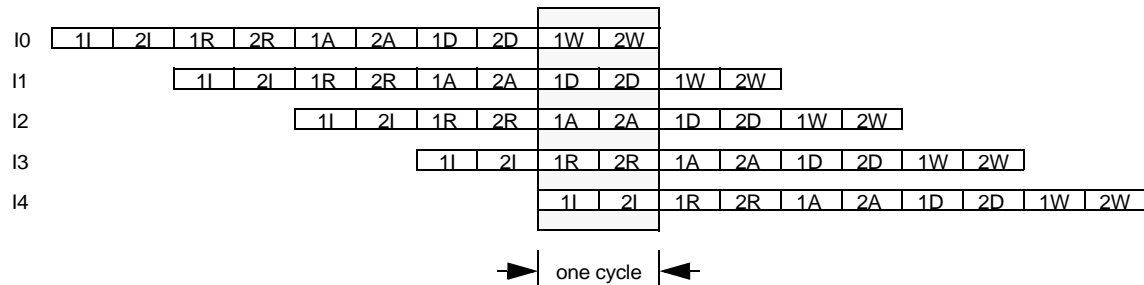
PC

3.3 Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the RM5231A uses the 5-stage pipeline. In addition to the integer pipeline, the RM5231A uses an extended 7-stage pipeline for floating-point operations.

Figure 3 shows the RM5231A integer pipeline. As illustrated in the figure, up to five integer instructions can be executing simultaneously.

Figure 3 Pipeline



- 1I-1R: Instruction cache access
- 2I: Instruction virtual to physical address translation
- 2R: Register file read, Bypass calculation, Instruction decode, Branch address calculation
- 1A: Issue or slip decision, Branch decision
- 1A: Data virtual address calculation
- 1A-2A: Integer add, logical, shift
- 2A: Store Align
- 2A-2D: Data cache access and load align
- 1D: Data virtual to physical address translation
- 2W: Register file write

3.4 Integer Unit

The RM5231A integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/divide operations, and the program counter (PC).

The RM5231A implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets.

3.5 Register File

The RM5231A has thirty-two general purpose registers with register location 0 (r0) hard wired to a zero value. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

3.6 ALU

The RM5231A ALU consists of an integer adder/subtractor, a logic unit, and a shifter. The adder performs address calculations in addition to arithmetic operations. The logic unit performs all logical and zero shift data moves. The shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle.

3.7 Integer Multiply/Divide

The RM5231A has a dedicated integer multiply/divide unit optimized for high-speed multiply and multiply-accumulate operations. Table 1 shows the performance of the multiply/divide unit on each operation

Table 1 Integer Multiply/Divide Operations

Opcode	Operand Size	Latency	Repeat Rate	Stall Cycles
MULT/U, MAD/U	16 bit	3	2	0
	32 bit	4	3	0
MUL	16 bit	3	2	1
	32 bit	4	3	2
DMULT, DMULTU	any	7	6	0
DIV, DIVD	any	36	36	0
DDIV, DDIVU	any	68	68	0

The baseline MIPS IV ISA specifies that the results of a multiply or divide operation be placed in the *Hi* and *Lo* registers. These values can then be transferred to the general purpose register file using the Move-from-Hi and Move-from-Lo (MFHI/MFLO) instructions.

In addition to the baseline MIPS IV integer multiply instructions, the RM5231A also implements the 3 operand multiply instruction, **MUL**. This instruction specifies that the multiply result go directly to the integer register file rather than the *Lo* register. The portion of the multiply that would have normally gone into the *Hi* register is discarded. For applications where it is known that the upper half of the multiply result is not required, using the **MUL** instruction eliminates the necessity of executing an explicit **MFLO** instruction.

Also included in the RM5231A are the multiply-add instructions, **MADU/MAD**. This instruction multiplies two operands and adds the resulting product to the current contents of the *Hi* and *Lo* registers. The multiply-accumulate operation is the core primitive of almost all signal processing algorithms allowing the RM5231A to eliminate the need for a separate DSP engine in many embedded applications.

3.8 Floating-Point Co-Processor

The RM5231A incorporates a high-performance fully pipelined floating-point co-processor which includes a floating-point register file and autonomous execution units for multiply/add/convert and divide/square root. The floating-point coprocessor is a tightly coupled execution unit, decoding and executing instructions in parallel with, and in the case of floating-point loads and stores, in cooperation with the integer unit. The superscalar capabilities of the RM5231A allow floating-point computation instructions to issue concurrently with integer instructions.

3.9 Floating-Point Unit

The RM5231A floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate divide/square root unit and a pipelined multiply/add unit. Overlap of the divide/square root and multiply/add operations is supported.

The RM5231A maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in object-oriented programming environments and highly desirable for debugging in any environment.

Floating-point operations includes:

- add
- subtract
- multiply
- divide
- square root
- reciprocal
- reciprocal square root
- conditional moves
- conversion between fixed-point and floating-point format
- conversion between floating-point formats, and floating-point compare.

Table 2 gives the latencies of the floating-point instructions in internal processor cycles.

Table 2 Floating-Point Instruction Cycles

Operation	Latency	Repeat Rate
fadd	4	1
fsub	4	1
fmult	4/5	1/2
fmadd	4/5	1/2
fmsub	4/5	1/2
fdiv	21/36	19/34
fsqrt	21/36	19/34

Operation	Latency	Repeat Rate
frecip	21/36	19/34
frsqr	38/68	36/66
fcvt.s.d	4	1
fcvt.s.w	6	3
fcvt.s.l	6	3
fcvt.d.s	4	1
fcvt.d.w	4	1
fcvt.d.l	4	1
fcvt.w.s	4	1
fcvt.w.d	4	1
fcvt.l.s	4	1
fcvt.l.d	4	1
fcmp	1	1
fmov	1	1
fmovc	1	1
fabs	1	1
fneg	1	1

Notes:

1. Numbers are represented as single/double precision format.

3.10 Floating-Point General Register File

The floating-point general register file (FGR) is made up of thirty-two 64-bit registers. With the floating-point load and store double instructions (LDC1 and SDC1), the floating-point unit can take advantage of the 64-bit wide data cache and issue a floating-point co-processor load or store doubleword instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily used for diagnostic software, exception handling, state saving and restoring, and control of rounding modes. To support superscalar operation, the FGR has four read ports and two write ports, and is fully bypassed to minimize operation latency in the pipeline. Three of the read ports and one write port are used to support the combined multiply-add instruction while the fourth read and second write port allows a concurrent floating-point load or store.

3.11 System Control Coprocessor (CP0)

The system control coprocessor, also called coprocessor 0 or CP0 in the MIPS architecture, is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor.

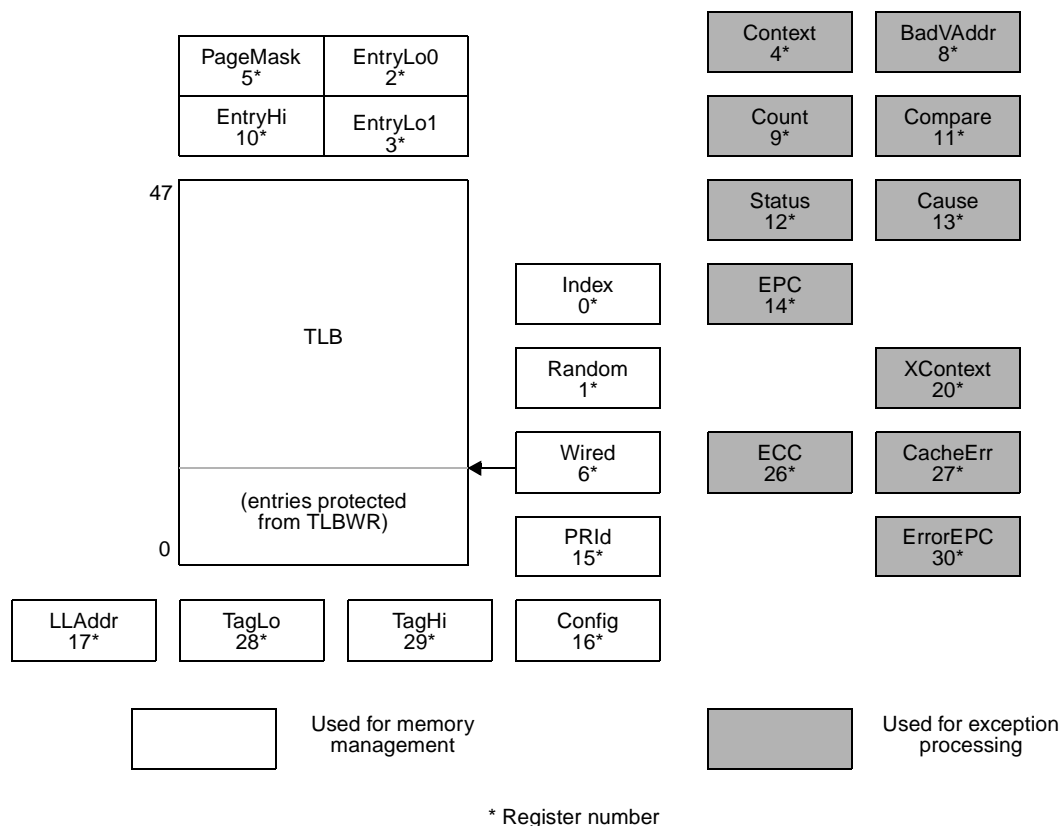
The memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer, ITLB, a data address translation buffer, DTLB, a Joint instruction and data address translation buffer, JTLB, and co-processor registers used by the virtual memory mapping sub-system.

3.12 System Control Co-Processor Registers

The RM5231A incorporates all system control coprocessor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and modified, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the RM5231A includes registers to implement a real-time cycle counting facility to aid in cache diagnostic testing and to assist in data error detection.

Figure 4 shows the CP0 registers.

Figure 4 CP0 Registers



3.13 Virtual to Physical Address Mapping

The RM5231A provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in the CP0 *Status* register determine which virtual addressing mode is used. In the user mode, the RM5231A provides a single, uniform virtual address space of 1TB (2 GB in 32-bit mode).

When operating in the kernel mode, four distinct virtual address spaces, totalling over 2.5 TB (4 GB in 32-bit mode), are simultaneously available and are differentiated by the high-order bits of the virtual address.

The RM5231A processor also supports a supervisor mode in which the virtual address space over 2 TB (2.5 GB in 32-bit mode), divided into three regions based on the high-order bits of the virtual address.

When the RM5231A is configured as a 64-bit microprocessor, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout.

Figure 5 shows the address space layout for 32-bit operation.

Figure 5 Kernel Mode Virtual Addressing (32-bit)

0xFFFFFFFF	Kernel virtual address space
	(kseg3)
0xE0000000	Mapped, 0.5GB
0xDFFFFFFF	Supervisor virtual address space
	(ksseg)
0xC0000000	Mapped, 0.5GB
0xBFFFFFFF	Uncached kernel physical address space
	(kseg1)
0xA0000000	Unmapped, 0.5GB
0x9FFFFFFF	Cached kernel physical address space
	(kseg0)
0x80000000	Unmapped, 0.5GB
0x7FFFFFFF	User virtual address space
	(kuseg)
	Mapped, 2.0GB
0x00000000	

3.14 Joint TLB

For fast virtual-to-physical address translation, the RM5231A uses a large, fully associative TLB that maps 96 virtual pages to their corresponding physical addresses. As indicated by its name, the joint TLB (JTLB) is used for both instruction and data translations. The JTLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64 GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to use page sizes in the range of 4 KB to 16 MB (in multiples of 4). The CP0 Page Mask register is loaded with the desired page size of a mapping, and that size is stored into the TLB along with the virtual address when a new entry is written. Thus, operating systems can create special purpose maps; for example, an entire frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The RM5231A provides a random replacement algorithm to select a TLB entry to be written with a new mapping. However, the processor also provides a mechanism whereby a system specific number of mappings can be locked into the TLB, thereby avoiding random replacement. This mechanism uses the Wired register to 'lock' certain TLB entries and allows the operating system to guarantee that certain pages are always mapped for performance reasons and for deadlock avoidance. This mechanism also facilitates the design of real-time systems by allowing deterministic access to critical software.

The JTLB also contains information that controls the cache coherency protocol for each page. Specifically, each page has attribute bits to determine the following coherency algorithms:

- uncached
- non-coherent write-back
- non-coherent write-through with write-allocate
- non-coherent write-through without write-allocate
- sharable
- exclusive
- update

The non-coherent protocols are used for both code and data on the RM5231A, with data using write-back or write-through depending on the application. The coherency attributes generate coherent transaction types on the system interface. However, in the RM5231A cache coherency is not supported, hence the coherency attributes should never be used.

3.15 Instruction TLB

The RM5231A implements a 2-entry instruction TLB (ITLB) to minimize contention for the JTLB, eliminate the timing critical path of translating through a large associative array, and save power. Each ITLB entry maps a 4 KB page. The ITLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation by the ITLB, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is completely transparent to the user.

3.16 Data TLB

The RM5231A implements a 4-entry data TLB (DTLB) for the same reasons cited above for the ITLB. Each DTLB entry maps a 4 KB page. The DTLB improves performance by allowing data address translation to occur in parallel with instruction address translation. When a miss occurs on a data address translation by the DTLB, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used pair of entries is filled. The operation of the DTLB is completely transparent to the user.

3.17 Cache Memory

The RM5231A incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and both caches can be accessed simultaneously. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of over 3 GB per second at an internal clock frequency of 200 MHz.

3.18 Instruction Cache

The RM5231A incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 32 KB in size and is protected with word parity.

Since the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing these two operations to occur simultaneously. The cache tag contains a 24-bit physical address, a valid bit, and has a single parity bit.

The instruction cache is 64-bits wide and can be accessed each processor cycle. Accessing 64 bits per cycle allows the instruction cache to supply two instructions per cycle to the superscalar dispatch unit. For typical code sequences where a floating-point load or store and a floating-point computation instruction are being issued together in a loop, the entire bandwidth available from the instruction cache is consumed.

Cache miss refill writes 64 bits per cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize the performance of communication between the processor and the memory system.

The RM5231A supports instruction cache locking. The contents of one set of the cache, set A, can be locked by setting a bit in the coprocessor 0 Status register. Locking the set prevents its contents from being overwritten by a subsequent cache miss. A refill occurs only into set B. This mechanism allows the programmer to lock critical code into the cache thereby guaranteeing deterministic behavior for the locked code sequence.

3.19 Data Cache

For fast, single cycle data access, the RM5231A includes a 32KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

Cache protocols supported for the data cache are:

1. Uncached

Data loads and instruction fetches from uncached memory space are brought in from main memory to the register file and the execution unit, respectfully. The caches are not accessed. Data stores to uncached memory space go directly to the main memory without updating the data cache.

2. Write-back

Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if the target address is cache resident. If it is resident, the cache contents are updated, and the cache line is marked for later write-back. If the cache lookup misses, the target cache line is first brought into the cache and then the write is performed as above.

3. Write-through with write allocate

Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if the target address is cache resident. If it is resident, the cache contents are updated and main memory is written, leaving the *write-back* bit of the cache line unchanged. If the cache lookup misses, the target line is first brought into the cache and then the write is performed as above.

4. Write-through without write allocate

Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if the target address is cache resident. If it is resident, the cache contents are updated and main memory is written, leaving the *write-back* bit of the cache line unchanged. If the cache lookup misses, then only main memory is written.

The most commonly used write policy is write-back, where a store to a cache line does not immediately cause main memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can, however, select write-through on a per-page basis when appropriate, such as for frame buffers.

Associated with the data cache is the store buffer. When the RM5231A executes a store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the data cache in the next cycle that the data cache is not accessed (the next non-load cycle). The store buffer allows the RM5231A to execute a store every processor cycle and to perform back-to-back stores without penalty. In the event of a store immediately followed by a load to the same address, a combined merge and cache write occurs such that no penalty is incurred.

The RM5231A cache attributes for both the instruction and data caches are summarized in Table 3.

Table 3 Cache Attributes

Characteristics	Instruction	Data
Size	32 KB	32 KB
Organization	2-way set associative	2-way set associative
Line size	32B	32B
Index	vAddr _{11..0}	vAddr _{11..0}
Tag	pAddr _{31..12}	pAddr _{31..12}
Write policy	n.a.	write-back/write-through
Read order	sub-block	sub-block
write order	sequential	sequential
miss restart after transfer of	entire line	first double
Parity	per-word	per-byte
Cache locking	set A	set A

3.20 Write Buffer

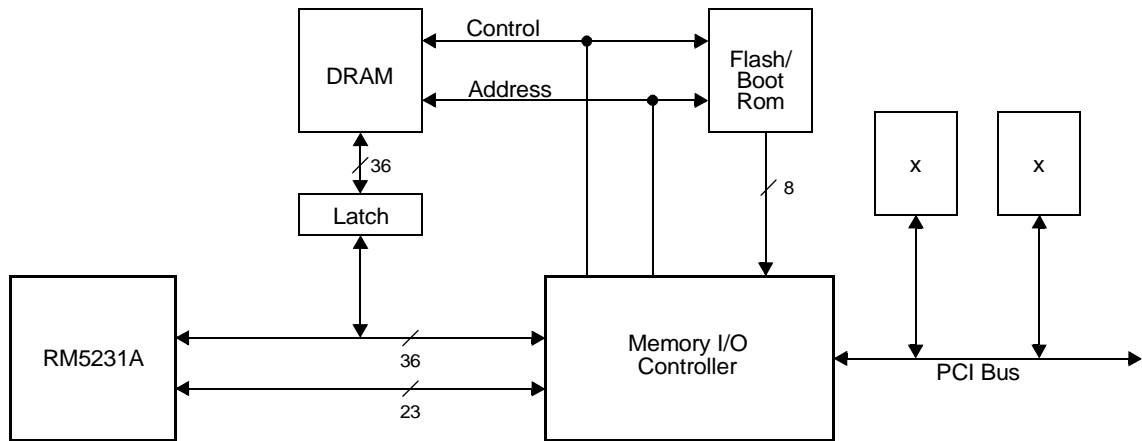
Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four 64-bit address and data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with the memory update. For uncached and write-through stores, the write buffer significantly increases performance by decoupling the **SysAD** bus transfers from the instruction execution stream.

3.21 System Interface

The system interface consists of a 32-bit Address/Data bus with 4 parity check bits and a 9-bit command bus. In addition, there are 6 handshake signals and 6 interrupt inputs. The interface is capable of transferring data between the processor and memory at a peak rate of 500 MB/sec with a 125 MHz SysClock.

Figure 6 shows a typical embedded system using the RM5231A. In this example, a bank of DRAMs and a memory controller ASIC share the processor's **SysAD** bus while the memory controller provides separate ports to a boot ROM and an I/O system.

Figure 6 Typical Embedded System Block Diagram



3.22 System Address/Data Bus

The 32-bit System Address Data (**SysAD**) bus is used to transfer addresses and data between the RM5231A and the rest of the system. It is protected with a 4-bit parity check bus (**SysADC**).

The system interface is configurable to allow easy interfacing to memory and I/O systems of varying frequencies. The Block Write data rate, Non-blocking Write protocol, and the Output Drive strength are programmable at Boot time via the **Mode Control** bits. The rate at which the processor receives data is also fully controlled by the external device.

3.23 System Command Bus

The RM5231A interface has a 9-bit System Command (**SysCmd**) bus. The command bus indicates whether the **SysAD** bus carries address or data information on a per-clock basis. If the **SysAD** carries address, then the **SysCmd** bus also indicates what type of transaction is to take place (for example, a read or write). If the **SysAD** carries data, then the **SysCmd** bus also gives information about the data (for example, this is the last data word transmitted, or the data contains an error). The **SysCmd** bus is bidirectional to support both processor requests and external requests to the RM5231A. Processor requests are initiated by the RM5231A and responded to by an external device. External requests are issued by an external device and require the RM5231A to respond.

The RM5231A supports one- to four-byte transfers as well as block transfers on the **SysAD** bus. In the case of a sub-word transfer, the two low-order address bits give the byte address of the transfer, and the **SysCmd** bus indicates the number of bytes being transferred.

3.24 Handshake Signals

There are six handshake signals on the system interface. Two of these, **RdRdy*** and **WrRdy***, are used by an external device to indicate to the RM5231A whether it can accept a new read or write transaction. The RM5231A samples these signals before deasserting the address on read and write requests.

ExtRqst* and **Release*** are used to transfer control of the **SysAD** and **SysCmd** buses from the processor to an external device. When an external device needs to control the interface, it asserts **ExtRqst***. The RM5231A responds by asserting **Release*** to release the system interface to slave state.

ValidOut* and **ValidIn*** are used by the RM5231A and the external device respectively to indicate that there is a valid address, a command, or data on the **SysAD** and **SysCmd** buses. The RM5231A asserts **ValidOut*** when it is driving these buses with a valid address, a command or data, and the external agent drives **ValidIn*** when it has control of the buses and is driving a valid address, a command, or data.

3.25 Non-overlapping System Interface

The RM5231A requires a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the RM5231A issues another request. The RM5231A can issue read and write requests to an external device, whereas an external device can issue null and write requests to the RM5231A.

For processor reads the RM5231A asserts **ValidOut*** and simultaneously drives the address and read command on the **SysAD** and **SysCmd** buses respectively. If the system interface has **RdRdy*** asserted, then the processor tristates its drivers and releases the system interface to the slave state by asserting **Release***. The external device can then begin sending data to the RM5231A.

Figure 7 shows a processor block read request and the external agent read response. The read latency is four cycles (**ValidOut*** to **ValidIn***), and the response data pattern is “WWWWWWWW”, indicating that data can be transferred on every clock with no wait states in-between. Figure 8 shows a processor block write using write response pattern “WWWWWWWW”, or code 0, of the boot time mode select options.

Figure 7 Processor Block Read

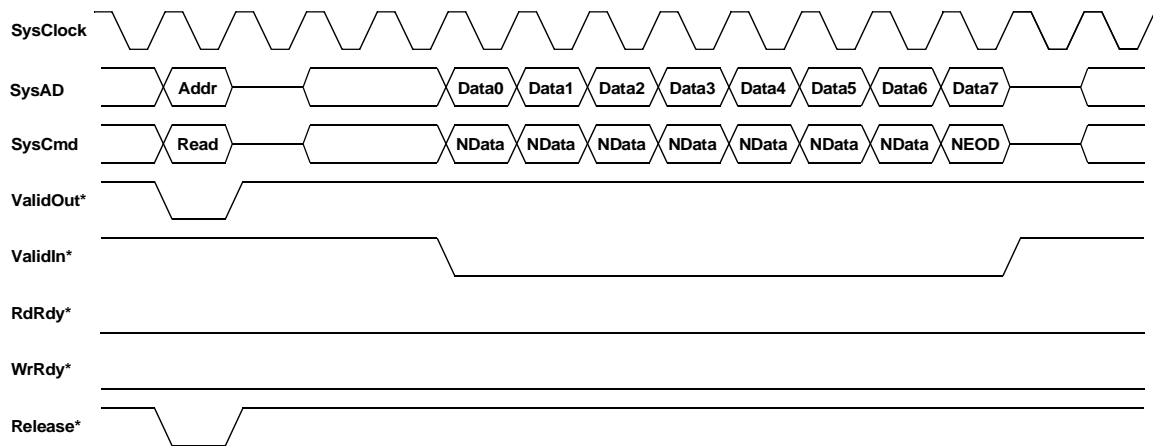
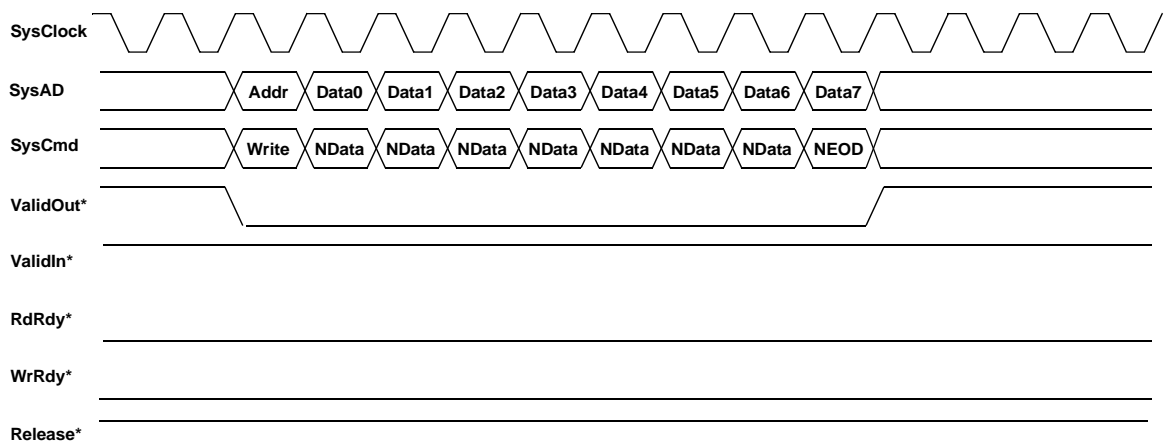


Figure 8 Processor Block Write



3.26 Enhanced Write Modes

The RM5231A implements two enhancements to the original R4000 write mechanism: Write Reissue and Pipeline Writes. The original R4000 allowed a write address cycle on the **SysAD** bus only once every four SysClock cycles. Hence for a non-block write, this meant that two out of every four cycles were wait states.

Pipelined write mode eliminates these two wait states by allowing the processor to drive a new write address onto the bus immediately after the previous write data cycle. This allows for higher **SysAD** bus utilization. However, at high bus frequencies the processor may drive a subsequent write onto the bus prior to the time the external agent deasserts **WrRdy***, indicating that it can not accept another write cycle. This can cause the write cycle to be missed.

Write reissue mode is an enhancement to pipelined write mode and allows the processor to reissue missed write cycles. If **WrRdy*** is deasserted during the issue phase of a write operation, the cycle is aborted by the processor and reissued at a later time.

In write reissue mode, a write rate of one write every two bus cycles can be achieved. Pipelined writes have the same two bus cycle write repeat rate, but can issue one additional write following the deassertion of **WrRdy***.

3.27 External Requests

The External Request pin, **ExtRqst***, is asserted by the external agent when it requires mastership of the system interface, either to perform an independent transfer or to write to the interrupt register within the RM5231A. An independent transfer is a data transfer between two external agents or between an external agent and memory or peripheral on the system interface. Following the asserting of the **ExtRqst***, the RM5231A tri-states its drivers allowing the external agent to use the system interface buses to complete an independent transfer. The external agent is responsible for returning mastership of the system interface to the RM5231A when it has completed the independent transfer and does so by executing an External Null cycle.

3.28 Interrupt Handling

The RM5231A supports a dedicated interrupt vector for real time interrupt handling. When enabled by the real time executive by setting a bit in the Cause register, interrupts vector to a specific address which is not shared with any of the other exception types. This capability eliminates the need to go through the normal software routine for exception decode and dispatch, thereby lowering interrupt latency.

3.29 Standby Mode

The RM5231A provides a means to reduce the amount of power consumed by the internal core when the CPU is not performing any useful operations. This state is known as Standby Mode.

Executing the WAIT instruction enables interrupts causes the processor to enter Standby Mode. When the WAIT instruction completes the W pipe stage, and if the **SysAD** bus is currently idle, the internal processor clocks stop, thereby freezing the pipeline. The phase lock loop, or PLL, internal timer/counter, and the “wake up” input pins: **Int[5:0]***, **NMI***, **ExtReq***, **Reset***, and **ColdReset*** continue to operate in their normal fashion. If the **SysAD** bus is not idle when the WAIT instruction completes the W pipe-stage, then the WAIT is treated as a NOP until the bus operation is completed. Once the processor is in Standby, any interrupt, including the internally generated timer interrupt, causes the processor to exit Standby and resume operation where it left off. The WAIT instruction is typically inserted in the idle loop of the operating system or real time executive.

3.30 JTAG Interface

The RM5231A interface supports JTAG Test Access Port (TAP) boundary scan in conformance with the IEEE 1149.1 specification. The JTAG interface is especially helpful for checking the integrity of the processors pin connections.

3.31 Boot-Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. This serial interface operates at a very low frequency (SysClock divided by 256). The low frequency operation allows the initialization information to be kept in a low cost EPROM or a system interface ASIC.

Immediately after the **V_{CC}OK** signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all the fundamental operational modes. ModeClock runs continuously from the assertion of **V_{CC}OK**.

3.32 Boot-Time Modes

The boot-time serial mode stream is defined in Table 4. Bit 0 is the bit presented to the processor as the first bit in the stream when **V_{CC}OK** is asserted. Bit 255 is the last bit transferred.

Table 4 Boot Time Mode Bit Stream

Mode bit	Description	Mode bit	Description
0	Reserved: Must be zero	15	Reserved: Must be zero
4:1	Write-back data rate (W = write data transfer, x = wait state) 0: WWWWWWWW 1: WWxWWxWWxWWx 2: WWxxWWxxWWxxWWxx 3: WxWxWxWxWxWxWxWx 4: WWxxxWWxxxWWxxxWWxxx 5: WWxxxxWWxxxxWWxxxxWWxxxx 6: WxxWxxWxxWxxWxxWxxWxxWxx 7: WWWxxxxxWWxxxxxxWWxxxxxxWWxxxxxx 8: WxxxWxxxWxxxWxxxWxxxWxxxWxxxWxxx 9-15 reserved	17:16	System configuration identifiers - software visible in Config[21..20] register
7:5	Pclock to SysClock Multiplier <u>Mode Bits 7:5</u> <u>Mode Bit 20=0</u> <u>Mode Bit 20=1</u> 000 Multiply by 2 n/a 001 Multiply by 3 n/a 010 Multiply by 4 n/a 011 Multiply by 5 Multiply by 2.5 100 Multiply by 6 n/a 101 Multiply by 7 Multiply by 3.5 110 Multiply by 8 n/a 111 Multiply by 9 Multiply by 4.5	19:18	Reserved: Must be zero
8	Specifies byte ordering. Logically ORed with BigEndian input signal. 0: Little endian 1: Big endian	20	Select SysClock to PClock Multiply Mode 0: Integer Multipliers 1: Half-Integer Multipliers
10:9	Non-Block Write Protocol 00: R4000 compatible 01: reserved 10: pipelined 11: write re-issue	21	Reserved: Must be one
11	Timer Interrupt Enable/Disable 0: Enable the timer interrupt on Int5* 1: Disable the timer interrupt on Int5*	22	V _{CCIO} Setting 0: V _{CCIO} = 3.3V 1: V _{CCIO} = 2.5V
12	Reserved: Must be zero	255:23	Reserved: Must be zero
14:13	Output driver strength - 100% = fastest 00: 67% strength 01: 50% strength 10: 100% strength 11: 83% strength		

4 Pin Descriptions

The following is a list of interface, interrupt, and miscellaneous pins available on the RM5231A. An '*' at the end of the signal name denotes an active low signal.

Table 5 System Interface

Pin Name	Type	Description
ExtRqst*	Input	External Request Signals that the system interface is submitting an external request.
Release*	Output	Release Interface Signals that the processor is releasing the system interface to slave state.
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid Output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD[31:0]	Input/Output	System Address/Data bus A 32-bit address and data bus for communication between the processor and an external agent.
SysADC[3:0]	Input/Output	System Address/Data check bus A 4-bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmd[8:0]	Input/Output	System Command/Data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved for system Command/Data identifier bus parity For the RM5231A, unused on input and zero on output.

Table 6 Clock/Control Interface

Pin Name	Type	Description
SysClock	Input	System Clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
V_{CC}P	Input	Quiet V_{CC} for PLL Quiet V_{CC} for the internal phase locked loop. Must be connected to V_{CC}Int through a filter circuit.
V_{SS}P	Input	Quiet V_{SS} for PLL Quiet V_{SS} for the internal phase locked loop. Must be connected to V_{SS} through a filter circuit.

Table 7 Interrupt Interface

Pin Name	Type	Description
Int[5:0]*	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Table 8 JTAG Interface

Pin Name	Type	Description
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.

Table 9 Initialization Interface

Pin Name	Type	Description
BigEndian	Input	Allows the system to change the processor addressing mode without rewriting the mode ROM.
V_{CC}OK	Input	V_{CC} is OK When asserted, this signal indicates to the RM5231A that both power supplies has been above the recommended value for more than 100 milliseconds and remains stable. The assertion of V_{CC}OK initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock .
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with SysClock .
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by 256
ModeIn	Input	Boot mode data in Serial boot-mode data input.

Table 10 Power Supply

Pin Name	Type	Description
V_{CC}Int	Input	Power supply for core.
V_{CC}IO	Input	Power supply for I/O.
V_{SS}	Input	Ground return.

5 Absolute Maximum Ratings¹

Symbol	Rating	Limits	Unit
V_{TERM}	Terminal Voltage with respect to GND	-0.5 ² to +3.9	V
T_{CASE}	Operating Temperature		
	Commercial	0 to +85	°C
	Industrial	-45 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{IN}	DC Input Current	$\pm 20^3$	mA
I_{OUT}	DC Output Current	$\pm 20^4$	mA

Notes:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = -2.0 V for pulse width less than 15 ns. V_{IN} should not exceed 3.9 Volts.
3. When $V_{\text{IN}} < 0\text{V}$ or $V_{\text{IN}} > V_{\text{CCIO}}$.
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

6 Recommended Operating Conditions

Grade	CPU Speed	Case Temperature	V _{SS}	V _{CCInt}	V _{CCIO}	V _{CCP}	V _{SSP}
Commercial	250 – 350 MHz	0°C to +85°C	0 V	1.57 V to 1.85 V	3.15 V to 3.45 V or 2.3 V to 2.7 V	1.57 V to 1.85 V	0 V
	400 MHz	0°C to 70°C	0 V	1.8 V ± 50 mV	3.15 V to 3.45 V	1.8 V ± 50 mV	0 V
Industrial	300 MHz	-45°C to +85°C	0 V	1.57 V to 1.85 V	3.15 V to 3.45 V or 2.3 V to 2.7 V	1.57 V to 1.85 V	0 V

Notes:

1. **V_{CCIO}** should not exceed **V_{CCInt}** by greater than 2.0 V during the power-up sequence.
2. Applying a logic high state to any I/O pin before **V_{CCInt}** becomes stable is not recommended.
3. As specified in IEEE 1149.1 (JTAG), the **JTMS** pin must be held high during reset to avoid entering JTAG test mode.
4. **V_{CCP}** must be connected to **V_{CCInt}** through a passive filter circuit. **V_{SSP}** must be connected to **V_{SS}** through a passive filter circuit. See the RM5200 User's Manual for the recommended filter circuit.

7 DC Electrical Characteristics

$V_{CCIO} = 3.15\text{ V} - 3.45\text{ V}$

Parameter	Minimum	Maximum	Conditions
V_{OL}		0.2 V	$ I_{OUT} = 100\text{ }\mu\text{A}$
V_{OH}	$V_{CCIO} - 0.2\text{ V}$		
V_{OL}		0.4 V	$ I_{OUT} = 2\text{ mA}$
V_{OH}	2.4 V		
V_{IL}	-0.3 V	0.8 V	
V_{IH}	2.0 V	$V_{CCIO} + 0.3\text{ V}$	
I_{IN}		$\pm 15\text{ }\mu\text{A}$	$V_{IN} = 0$
		$\pm 15\text{ }\mu\text{A}$	$V_{IN} = V_{CCIO}$

$V_{CCIO} = 2.3\text{ V} - 2.7\text{ V}$

Parameter	Minimum	Maximum	Conditions
V_{OL}		0.2 V	$ I_{OUT} = 100\text{ }\mu\text{A}$
V_{OH}	2.1 V		
V_{OL}		0.4 V	$ I_{OUT} = 1\text{ mA}$
V_{OH}	2.0		
V_{OL}		0.7 V	$ I_{OUT} = 2\text{ mA}$
V_{OH}	1.7		
V_{IL}	-0.3 V	0.7 V	
V_{IH}	1.7 V	$V_{CCIO} + 0.3\text{ V}$	
I_{IN}		$\pm 15\text{ }\mu\text{A}$	$V_{IN} = 0$
		$\pm 15\text{ }\mu\text{A}$	$V_{IN} = V_{CCIO}$

8 Power Consumption

Parameter		Conditions	CPU Speed			
			250 MHz	300 MHz	350 MHz	400 MHz
			Max ¹	Max ¹	Max ¹	Max ¹
V _{CCInt} Power (mWatts) ³	standby		350	350	350	400
	active	Maximum with no FPU operation ²	900	1100	1200	1500
		Maximum worst case instruction mix	950	1150	1350	1700

Notes:

1. Maximum supply voltage (**V_{CCInt}**) with maximum temperature (TCase).
2. Dhrystone 2.1 instruction mix.
3. **V_{CCIO}** supply power is application dependant, but typically <20% of **V_{CCInt}**.

9 AC Electrical Characteristics

9.1 Capacitive Load Deration

Parameter	Symbol	Min	Max	Units
Load Derate	C _{LD}	—	2	ns/25pF

9.2 Clock Parameters

Parameter	Symbol	Test Conditions	CPU Speed								Units
			250 MHz		300 MHz		350 MHz		400 MHz		
			Min	Max	Min	Max	Min	Max	Min	Max	
SysClock High	t _{SCH}	Transition ≤ 2ns	3		3		3		3		ns
SysClock Low	t _{SCL}	Transition ≤ 2ns	3		3		3		3		ns
SysClock Frequency			33	125	33	125	33	125	33	133	MHz
SysClock Period	t _{SCP}		8	30	8	30	8	30	7.5	30	ns
Clock Jitter for SysClock	t _{Jl}			±150		±150		±150		±150	ps
SysClock Rise Time	t _{CR}			2		2		2		2	ns
SysClock Fall Time	t _{CF}			2		2		2		2	ns
ModeClock Period	t _{ModeCKP}			256		256		256		256	t _{SCP}
JTAG Clock Period	t _{JTAGCKP}		4		4		4		4		t _{SCP}

Notes:

- Operation of the RM5231A is only guaranteed with the Phase Lock Loop enabled.

9.3 System Interface Parameters¹

Parameter ¹	Symbol	Conditions	CPU Speed				Units
			250 to 350 MHz		400 MHz		
			Min	Max	Min	Max	
Data Output ^{2,3}	t _{DO}	mode14..13 = 10 ^{5,6} (fastest)	1.0	5.0	1.0	4.75	ns
		mode14..13 = 01 ^{5,6} (slowest)	1.0	6.0	1.0	5.75	ns
Data Setup ⁴	t _{DS} ⁶	t _{rise} = see above table	2.5		2.0		ns
Data Hold ⁴	t _{DH}	t _{fall} = see above table	1.0		1.0		ns

Notes:

1. Timings are measured from 0.425 x V_{CCIO} of clock to 0.425 x V_{CCIO} of signal for 3.3V I/O. Timings are measured from 0.48 x V_{CCIO} of clock to 0.48 x V_{CCIO} of signal for 2.5V I/O.
2. Capacitive load for all maximum output timings is 50 pF. Minimum output timings are for theoretical no load condition-untested.
3. Data Output timing applies to all signal pins whether tristate I/O or output only.
4. Setup and Hold parameters apply to all signal pins whether tristate I/O or input only.
5. Only mode 14:13 = 10 is tested and guaranteed.
6. Data shown is for 3.3 V I/O. For 2.5 V I/O (250 to 350 MHz CPU speeds only) derate all times by .5 nS.

9.4 Boot-Time Interface Parameters

Parameter	Symbol	Min	Max	Units
Mode Data Setup	t _{DS}	4		SysClock cycles
Mode Data Hold	t _{DH}	0		SysClock cycles

10 Timing Diagrams

Figure 9 Clock Timing



10.1 System Interface Timing (SysAD, SysCmd, ValidIn*, ValidOut*, etc.)

Figure 10 Input Timing

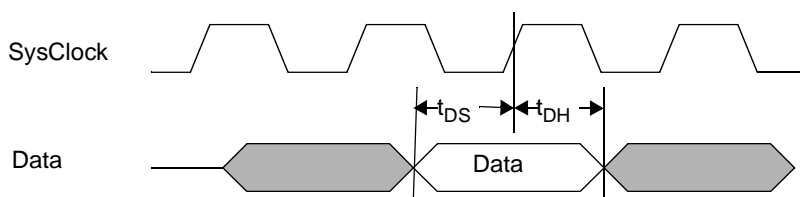
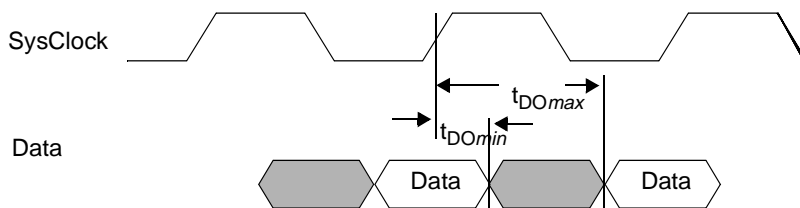
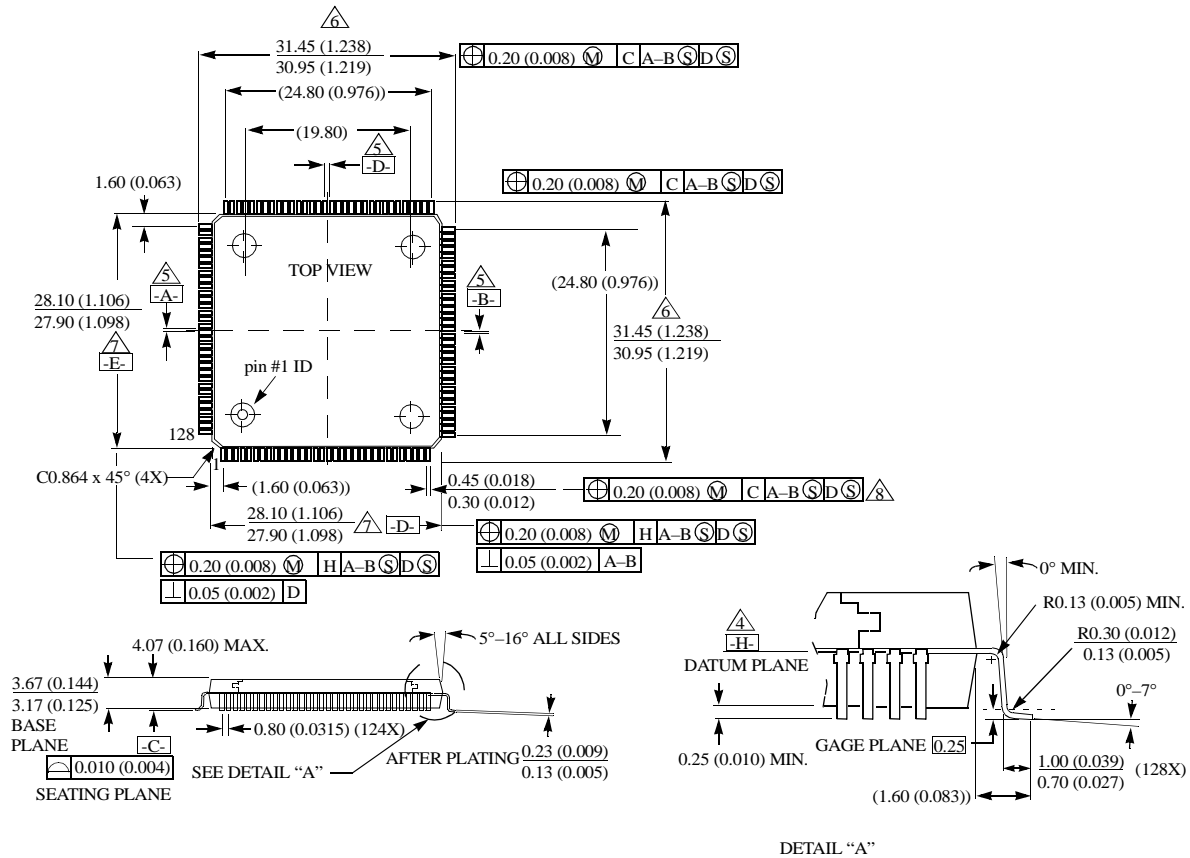


Figure 11 Output Timing



11 Packaging Information



Notes

- Package dimensions conform to JEDEC MO-108(DB-1).
- Controlling dimensions: millimeters. Dimensions in inches are shown in parentheses.
- Dimensions and tolerancing per ANSI Y14.5 – 1982.
- Datum plane "H" is located at the mold parting line and is coincident with the lead exits the plastic body at bottom of the parting line.
- Datums "A-B" and "D" to be determined at datum plane "H".
- To be determined at the seating plane "C".
- These dimensions to be determined at datum plane "H". Dimensions "D" and "E" do not include mold protrusion. Allowable protrusion is 0.25/0.10" per side.
- Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm/0.003" total in excess of this dimension at the maximum material condition. Dambar cannot be located on the lower radius of the foot.
- Pin numbers start with Pin #1 and continue counter clockwise to pin #128 when viewed from the top.

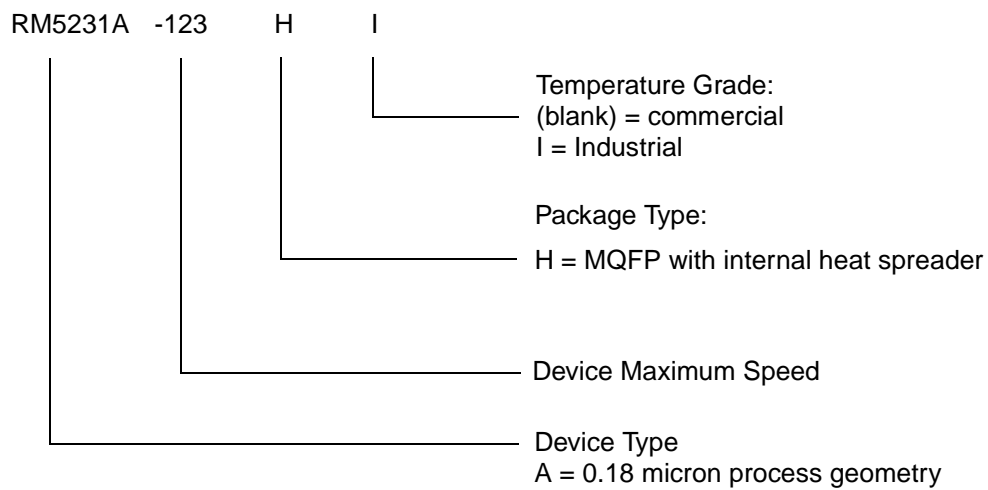
12 RM5231A 128-QFP Package Numerical Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	NC	33	ModelIn	65	NMI*	97	NC
2	NC	34	RdRdy*	66	ExtRqst*	98	NC
3	V _{CC} IO	35	WrRdy*	67	Reset*	99	NC
4	V _{SS}	36	ValidIn*	68	ColdReset*	100	NC
5	SysAD4	37	ValidOut*	69	V _{CC} OK	101	V _{CC} IO
6	SysAD5	38	Release*	70	BigEndian	102	V _{SS}
7	V _{CC} Int	39	V _{CC} P	71	V _{CC} IO	103	SysAD28
8	V _{SS}	40	V _{SS} P	72	V _{SS}	104	SysAD29
9	SysAD6	41	SysClock	73	SysAD16	105	V _{CC} Int
10	SysAD7	42	V _{CC} Int	74	V _{CC} Int	106	V _{SS}
11	SysAD8	43	V _{SS}	75	V _{SS}	107	SysAD30
12	SysAD9	44	SysCmd0	76	SysAD17	108	SysAD31
13	V _{CC} IO	45	SysCmd1	77	SysAD18	109	SysADC2
14	V _{SS}	46	SysCmd2	78	SysAD19	110	V _{CC} Int
15	SysAD10	47	SysCmd3	79	V _{CC} Int	111	V _{SS}
16	SysAD11	48	V _{CC} IO	80	V _{SS}	112	SysADC3
17	V _{CC} Int	49	V _{SS}	81	SysAD20	113	V _{CC} IO
18	V _{SS}	50	SysCmd4	82	SysAD21	114	V _{SS}
19	SysAD12	51	SysCmd5	83	V _{CC} IO	115	SysADC0
20	SysAD13	52	V _{SS}	84	V _{SS}	116	SysADC1
21	SysAD14	53	SysCmd6	85	SysAD22	117	SysAD0
22	V _{CC} Int	54	SysCmd7	86	SysAD23	118	SysAD1
23	V _{SS}	55	SysCmd8	87	SysAD24	119	V _{CC} Int
24	SysAD15	56	SysCmdP	88	SysAD25	120	V _{SS}
25	V _{CC} IO	57	V _{CC} Int	89	V _{CC} Int	121	SysAD2
26	V _{SS}	58	V _{SS}	90	V _{SS}	122	SysAD3
27	ModeClock	59	Int0*	91	SysAD26	123	V _{CC} IO
28	JTDO	60	Int1*	92	SysAD27	124	V _{SS}
29	JTDI	61	Int2*	93	V _{CC} IO	125	NC
30	JTCK	62	Int3*	94	V _{SS}	126	NC
31	JTMS	63	Int4*	95	NC	127	NC
32	V _{CC} IO	64	Int5*	96	NC	128	NC

13 RM5231A 128-QFP Package Alphabetical Pinout

Function	Pin	Function	Pin	Function	Pin	Function	Pin
BigEndian	70	SysAD1	118	SysADC1	116	V _{CC} IO	71
ColdReset*	68	SysAD2	121	SysADC2	109	V _{CC} IO	83
ExtRqst*	66	SysAD3	122	SysADC3	112	V _{CC} IO	93
Int0*	59	SysAD4	5	SysClock	41	V _{CC} IO	101
Int1*	60	SysAD5	6	SysCmd0	44	V _{CC} IO	113
Int2*	61	SysAD6	9	SysCmd1	45	V _{CC} IO	123
Int3*	62	SysAD7	10	SysCmd2	46	V _{CC} OK	69
Int4*	63	SysAD8	11	SysCmd3	47	V _{CC} P	39
Int5*	64	SysAD9	12	SysCmd4	50	V _{SS}	4
JTCK	30	SysAD10	15	SysCmd5	51	V _{SS}	8
JTDI	29	SysAD11	16	SysCmd6	53	V _{SS}	14
JTDO	28	SysAD12	19	SysCmd7	54	V _{SS}	18
JTMS	31	SysAD13	20	SysCmd8	55	V _{SS}	23
ModeClock	27	SysAD14	21	SysCmdP	56	V _{SS}	26
ModeIn	33	SysAD15	24	ValidIn*	36	V _{SS}	43
NC	1	SysAD16	73	ValidOut*	37	V _{SS}	49
NC	2	SysAD17	76	V _{CC} Int	7	V _{SS}	52
NC	95	SysAD18	77	V _{CC} Int	17	V _{SS}	58
NC	96	SysAD19	78	V _{CC} Int	22	V _{SS}	72
NC	97	SysAD20	81	V _{CC} Int	42	V _{SS}	75
NC	98	SysAD21	82	V _{CC} Int	57	V _{SS}	80
NC	99	SysAD22	85	V _{CC} Int	74	V _{SS}	84
NC	100	SysAD23	86	V _{CC} Int	79	V _{SS}	90
NC	125	SysAD24	87	V _{CC} Int	89	V _{SS}	94
NC	126	SysAD25	88	V _{CC} Int	105	V _{SS}	102
NC	127	SysAD26	91	V _{CC} Int	110	V _{SS}	106
NC	128	SysAD27	92	V _{CC} Int	119	V _{SS}	111
NMI*	65	SysAD28	103	V _{CC} IO	3	V _{SS}	114
RdRdy*	34	SysAD29	104	V _{CC} IO	13	V _{SS}	120
Release*	38	SysAD30	107	V _{CC} IO	25	V _{SS}	124
Reset*	67	SysAD31	108	V _{CC} IO	32	V _{SS} P	40
SysAD0	117	SysADC0	115	V _{CC} IO	48	WrRdy*	35

14 Ordering Information



Valid Combinations

RM5231A-250-H
 RM5231A-300-H
 RM5231A-300-HI (contact sales prior to design)
 RM5231A-350-H
 RM5231A-400-H