CY2308: Zero Delay Buffer

Introduction to Cypress Zero Delay Buffers

What is a Zero Delay Buffer?

A zero delay buffer is a device that can fan out one clock signal into multiple clock signals with zero delay and very low skew between the outputs. This device is well suited for a variety of clock distribution applications requiring tight input-output and output-output skews. A simplified diagram of a zero delay buffer is shown in *Figure 1*. A zero delay buffer is built with a PLL that uses a reference input and a feedback input. The feedback input is driven by one of the outputs. The phase detector adjusts the output frequency of the VCO so that its two inputs have no phase or frequency difference. Since the PLL control loop includes one of the outputs and its load, it will dynamically compensate for the load placed on that output. This means that it will have zero delay from the input to the output that drives feedback, irrespective of the loading on that output. Please note that this is only the case for the output being monitored by the Feedback input; all other outputs have a input to output delay that is affected by the differences in the output loads. Please see the section "*Lead or Lag Adjustment*" for a discussion of this topic.

What is the CY2308?

The Cypress CY2308 is a dual bank general purpose zero-delay buffer providing multiple (8) copies of a single input clock with zero delay from input to output and low skew between outputs. This is designed for use in a variety of clock distribution applications. The capability to externally close the feedback path on the device provides skew-control, and opens up opportunities for some interesting applications.

Closing Feedback Loop

The CY2308 is an open feedback device. To function as a zero delay buffer, the feedback loop must be closed. Any of the 8 outputs can be fed back into the feedback pin to close the loop and form a simple zero delay buffer. Loading on the output which is fed back can be used for simple lead or lag adjustments as detailed in the section "*Lead or Lag Adjustment*". Certain amount of lead/lag or output-output skew could be inadvertently introduced by improperly loading the outputs. Refer to the section "*Lead or Lag Adjustment*" to understand and avoid such a situation.

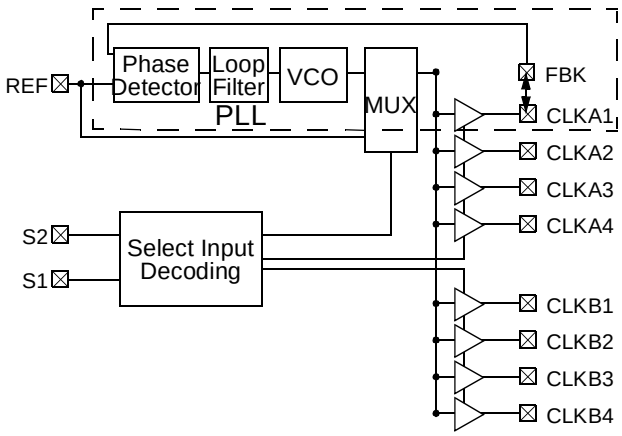

Figure 1. Simplified Block Diagram of CY2308-1

Drive Capability

The CY2308 has high drive outputs designed to drive 30 pF capacitance each. Since the typical CMOS input is 7 pF and the CY2308 is designed to drive up to 30 pF; this means that up to 4 CMOS inputs can be driven from a single output of a CY2308. However the output loading on the CY2308 must be equal on all outputs to maintain zero delay from the input. The 30pF load capacitance drive capability meets the JEDEC SDRAM specification of 30pF capacitance on each DIMM clock input. CY2305 and CY2309 are closed loop, zero delay buffers, designed specifically for the SDRAM DIMM applications. For more information on these devices refer to the application note: *"CY2305 and CY2309 as PCI and SDRAM Buffers"*

Special Power Down Feature

The CY2308 has a unique power-down mode: if the input reference is stopped, the part automatically enters a shutdown state, shutting down the PLL and three-stating the outputs. When the part is in shutdown mode it draws less than 50 μA, and can come out of shutdown mode with the PLL locked in less than 1 ms. This power down mode can also be entered by three-stating the input reference driver and allowing the internal pull-down resistor to pull the input LOW (the input does not have to go LOW, it only has to stop).

The outputs are treated as two banks of 4 outputs each and two Select lines are provided to individually three-state the two banks of 4 outputs, and even powerdown the PLL for low power operation.

Special test mode can be implemented by bypassing the PLL completely and driving the reference through the device. Refer to *Table 1* for various operating configurations using Select lines.

Table 1. Select Input Decoding

S2	S1	CLK A1-A4	CLK B1-B4	Output Source	PLL
0	0	OFF	OFF	PLL	OFF
0	1	Driven	OFF	PLL	ON
1	0	Driven	Driven	Ref	OFF
1	1	Driven	Driven	PLL	ON

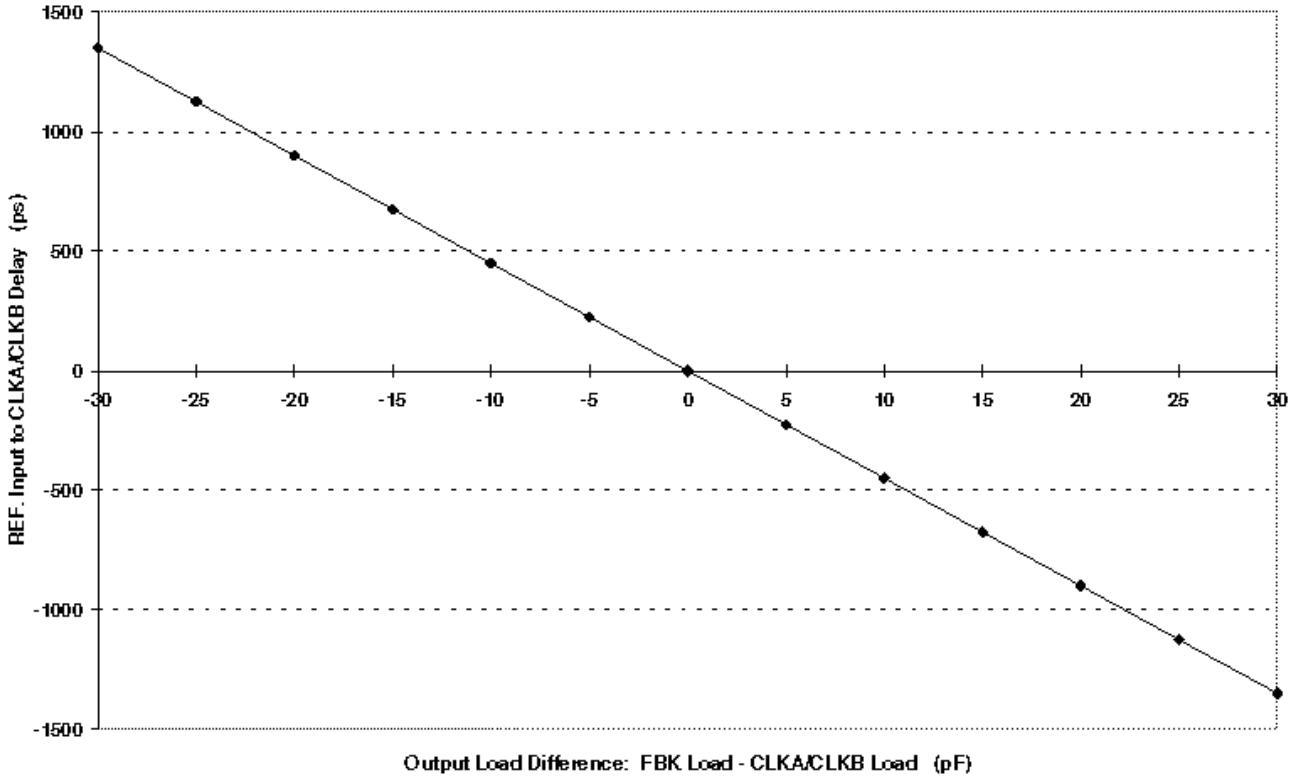

Figure 2. Lead Lag Adjustments

Lead or Lag Adjustments

To adjust the lead or lag of the outputs on the CY2308, one must understand the relationships between REF and FBK, and the relationship between output driving FBK and the other outputs. To understand the relationships, first we need to understand a few properties of the CY2308 Phase Locked Loops. The PLL senses the phase of the FBK pin at a threshold of $V_{DD}/2$ and compares it to the REF pin at the same $V_{DD}/2$ threshold. All the outputs start their transition at the same time (including the output driving FBK). Changing the load on an output changes its rise time and therefore how long it takes the output to get to the $V_{DD}/2$ threshold. Using these properties to our advantage, we can then adjust the time when the outputs reach the $V_{DD}/2$ threshold relative to when the REF input reaches the $V_{DD}/2$ threshold. The output driving FBK however cannot be adjusted: it will always have zero delay from the REF input at $V_{DD}/2$. The outputs can be advanced by loading this output more heavily than the other outputs or can be delayed by loading it more lightly than the other outputs. The chart in *Figure 2*, "*REF.Input to CLKA/CLKB Delay v/s Loading Difference between FBK and CLKA/CLKB pins,*" shows how many picoseconds the outputs are moved vs. the difference in the loading between the feedback output and the other outputs. As a rough guideline, the adjustment is 50 ps/pF of loading difference. Note: The zero delay buffer will always adjust itself to keep the $V_{DD}/2$ point of the output at zero delay from the $V_{DD}/2$ point of the reference. If the application requires the outputs of the zero delay buffer to have zero delay from another output of the reference clock chip, the output of the clock chip that is driving the zero delay buffer must be loaded the same as the other outputs of the clock chip or the outputs of the zero delay buffer will be advanced/delayed with reference to those other outputs. The circuit shown in *Figure 3* can be used to advance or delay any output with respect to the output driving feedback, by changing the value of the capacitive loads.

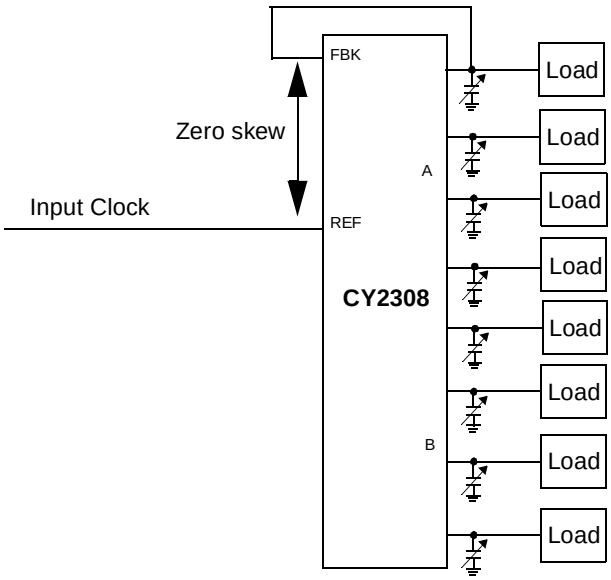

Figure 3. Test Circuit: Lead Lag Adjustments

Output To Output Skew

The skew between the feedback output and the other outputs is not dynamically adjusted. All MUST have the same load on them to achieve zero output to output skew. *Figure 4*, "CY2308 Timing Diagram With Different Loading Configurations" shows how output loading affects output-output skew. Here, FBK is assumed to be driven by CLKA1, however any output can be used to drive FBK. As seen in the diagram if the other outputs are less loaded than CLKA1, they will lead it; and if the other outputs are more loaded, they will lag CLKA1. The relationship that exists between CLKA1 and the rest of the outputs is that they all start the rising edge at the same time, but different loads will cause them to have different rise times and different times crossing the measurement thresholds. Since CLKA1, in this case, is the only output that is monitored, it will be the output that has zero delay from the reference and the other clocks will be relative to CLKA1 and their loading differences.

Zero Delay Buffer Timing diagrams with different loading configurations.

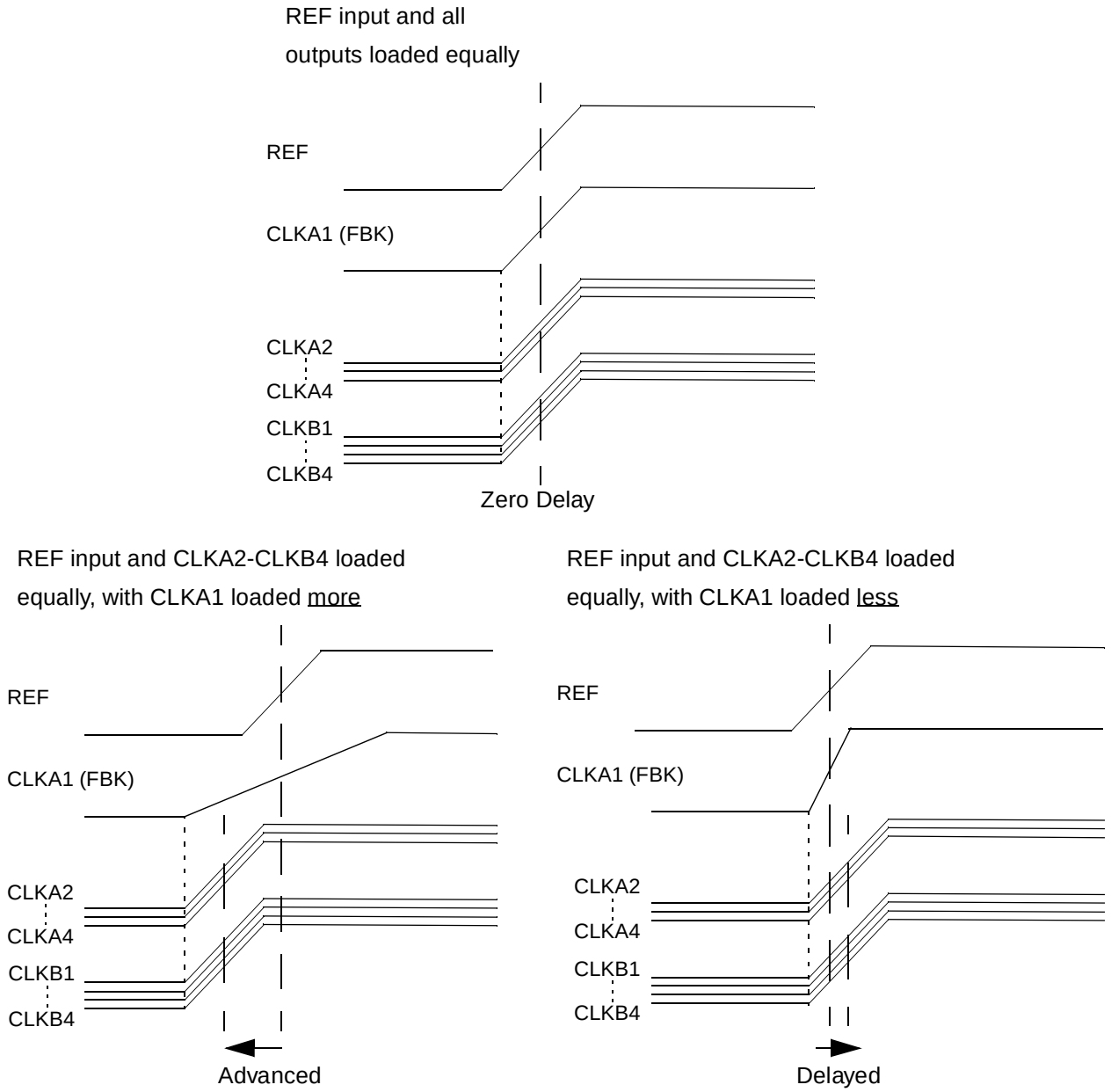

Figure 4. CY2308 Timing Diagram With Different Loading Configurations, and CLKA1 Driving FBK

Applications

Increasing Fanout (Buffering) of a Clock Signal Without Skew Penalty

Increasing fanout, increasing drive strength or simply re-establishing a weak clock signal on a long trace requires the use of clock buffers. Traditional high-speed buffers have a propagation delay associated with them which designers have to account for (and live with) while performing timing analyses on the design. As shown in *Figure 5*, phase lock loop based zero delay buffers like the CY2308 provide required buffering without the associated penalty of propagation delay.

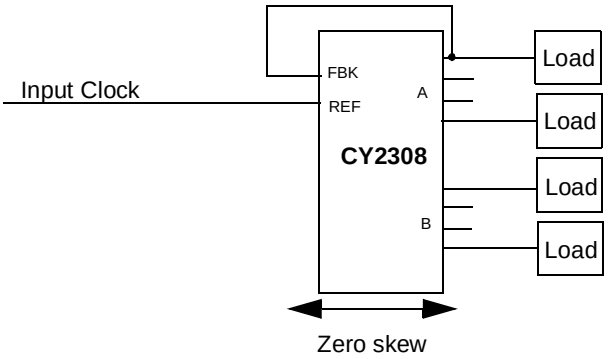

Figure 5. Clock Buffering

5 Volt to 3.3 Volt Level Shifting

The CY2308 can act as a 5-volt to 3.3-volt level shifter. The reference input pad is 5-volt signal-compatible. Since many system components still operate at 5 volts, this feature provides the capability to generate multiple 3.3-volt clocks from a single 5-volt reference clock, again without any propagation delay introduced in the level shifting. This 5-volt signal-compatibility is only available on the reference pad; the select inputs on the CY2308 are not 5-volt compatible. However a large resistor (>100KOhms) can be used to connect the select pins to a 5V supply. Also the select lines have weak internal pull-ups and can be left floating. See *Figure 6*.

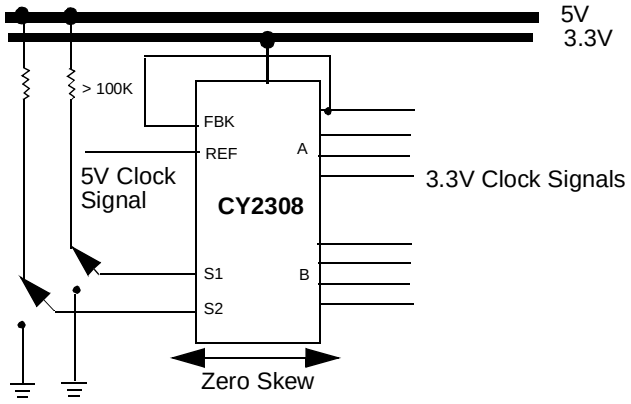

Figure 6. Voltage Level Shifting

Reducing EMI/EMC in Clock Distribution by Level Shifting

Electromagnetic interference (EMI) and Electromagnetic coupling (EMC) are caused by high energy Electromagnetic Fields (EMF) travelling around the system. This is caused by high frequency switching signals on a system. Long transmission lines distributing these high frequency signals are an automatic cause of EMC and EMI. Using proper termination and impedance matching on these lines helps reduce this problem by properly dissipating the transmitted energy (For more information on this, refer to the appnote *"Layout and Termination Techniques for Cypress Clock Generators"*). Another technique to control EMI and EMC is to reduce the actual energy of the high frequency signal. The CY2308 can be used to do just that. As shown in the previous example, the CY2308 can be used to convert 5V clock signals into 3.3V clock signals on the output. In *Figure 7* below, these 3.3V signals are distributed over long transmission lines instead of 5V signals, and the energy in the generated EMF is substantially reduced. The output of the CY2308 is 3.3V, swinging rail to rail, making it 5V TTL compliant. Hence at the load, it can be driven into a 5V device. The only requirement here is the presence of a 3.3V supply.

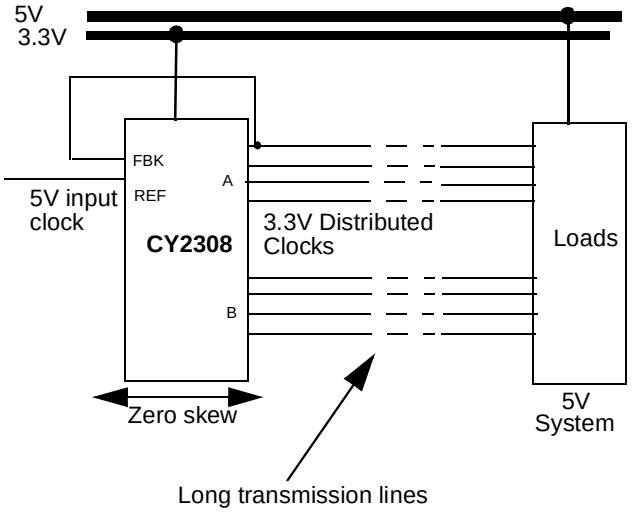

Figure 7. Reducing EMI

Eliminating Output to Output Skew by Ganging Outputs

The CY2308 has specified output to output skew of no greater than 250 ps.

An innovative approach to reducing output to output skew is to gang multiple outputs together. This method has been used to both increase drive to a particular input as well as eliminate the output to output skews associated with multiple outputs**.**

In *Figure 8*, three outputs are shown ganged together, and then distributed to three different loads. This will reduce the skew between the clocks delivered to those loads. Note that three separate series termination resistors are shown for the three loads.

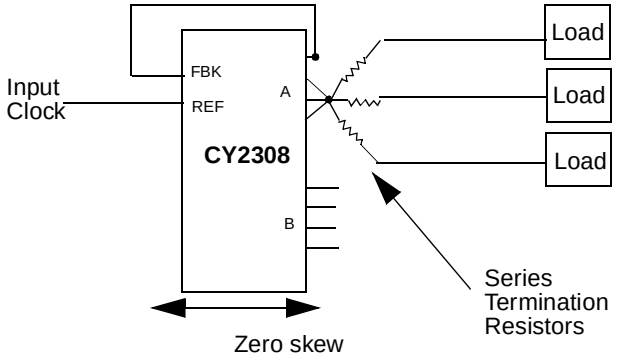

Figure 8. Ganged Outputs

Using external feedback

CY2308 has an open feedback path which is simply closed (by driving any output into the FBK pin) for zero delay buffer operation. However, the feedback path can be used for other interesting applications. We will discuss a few of those here:

Generation of 'Early' Clocks

Using a discrete delay element in the feedback path will generate 8 outputs which lead the input signal. These outputs are 'Early' as compared to the input clock. Certain chipsets require some copies of the host clock, which are early compared to the rest of the copies of the host clock. *Figure 9* suggests a circuit implementation to generate such early clocks.

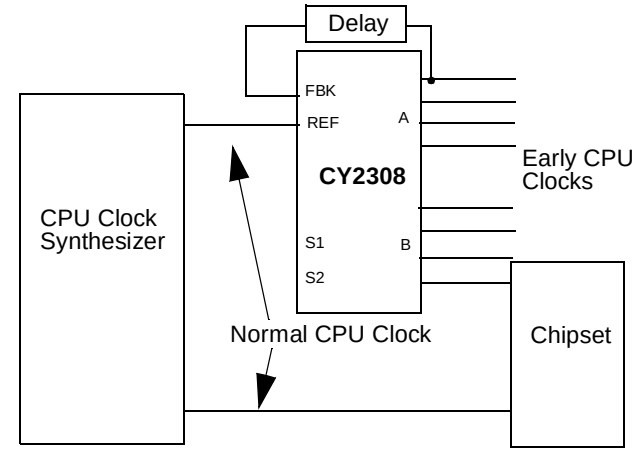

Figure 9. Early Clock

Using Variable Loading to Create Leading or Lagging Clocks

A simple approach can be incorporated in the CY2308 to create leading or lagging clock edges with respect to the REF clock. As discussed earlier, by adjusting the load on the clock being fed back to the FBK pin, we can alter and adjust the time when the output clock reaches $V_{DD}/2$ by varying its load. In the following example we use a variable trace length to alter the load on the output. If we assume a load of 3.0 pF/inch of trace and a delay of 50 ps/pF, then we can easily predict how much lead or lag we can induce on our output clocks.

In *Figure 10* we have controlled the trace lengths of the outputs to be a nominal length. We have also controlled the output of Clock A1, which is fed back to the FBK pin, to be 5 inches shorter than nominal. We can predict that clocks A2-B4 will lag the REF and Clock A1 output by 750 ps.

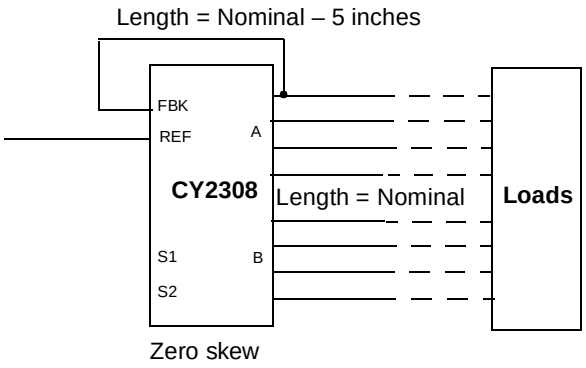

Figure 10. Leading / Lagging Clocks: Varying Feedback Length

Likewise, the outputs can be advanced with respect to the clock chosen as the FBK input. The same method of varying the load can be incorporated. The trace length can be increased by a number of inches or a variable length capacitor can be added to the feedback path. In *Figure 11* we add a 20-pF capacitor to create a series of output clocks which lead clock A by 1 ns.

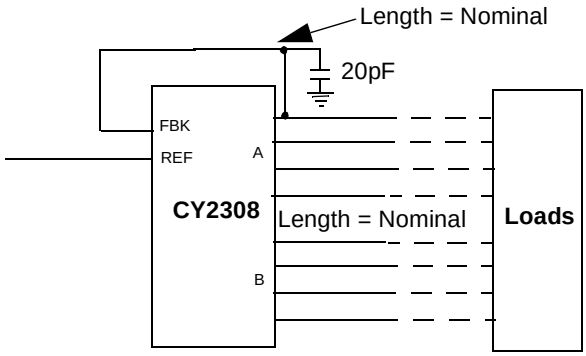

Figure 11. Leading / Lagging Clocks: Varying Capacitance

Frequency Multiplier

Using an external divider in the feedback path can create a frequency multiplier out of the CY2308. As shown in *Figure 12*, a /N divider in the feedback path will cause all outputs to run at a frequency which is XN times the input frequency. Whatever the multiplication factor, input and output frequencies must be in the 10–130 MHz range, which means the divider cannot be larger than 13.

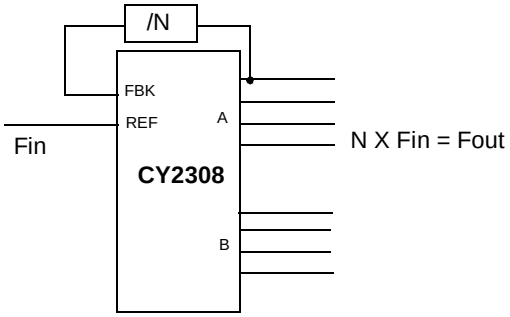

Figure 12. Frequency Multiplier

Zero Delay Frequency Multiplier/Divider Using Internal Feedback: The Extended Family of Zero Delay Buffers

How do you get simple multiply/divide functions, with zero propagation delay and with a single device? To answer this question, the family of zero delay buffers was expanded to include dividers internal to the CY2308. The block diagrams of the CY2308-2, -3, -4 are shown in *Figure 13*. Driving FBK from the correct output bank can generate the required functions on the outputs. *Table 2* defines the outputs to be used for feedback and can be used as a reference while deriving functions.

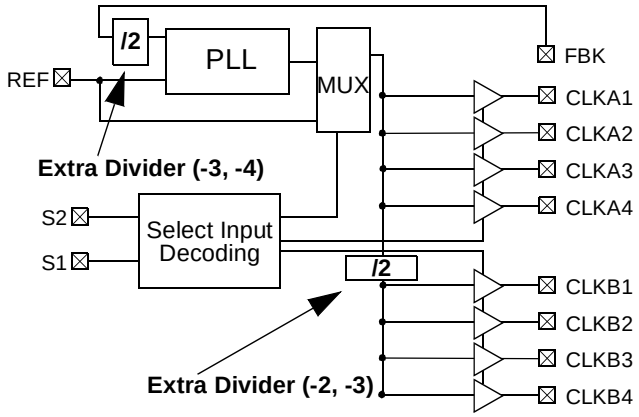

Figure 13. Simplified Block Diagram of CY2308-2,-3,-4

Table 2. CY2308-2,-3,-4 configurations

P/N	FBK	Outputs	
	Output	Bank A	Bank B
CY2308-1	A or B	X1	X1
CY2308-2	A	X1	X0.5
CY2308-2	B	X2	X1
CY2308-3	A	X2	X1
CY2308-3	B	X4	X2
CY2308-4	A or B	X2	X2

Sample Application

A sample application for the CY2308-2 is shown in *Figure 14*. Here a PCI Clock (33.33 MHz) on a plug-in card is used to generate copies of both CPU(66.66 MHz) and PCI (33.33 MHz) clocks (with zero delay). Here feedback is taken from Bank B. If feedback is taken from Bank A instead of Bank B, a CPU input clock of frequency 66.66 MHz can be used to generate the same outputs.

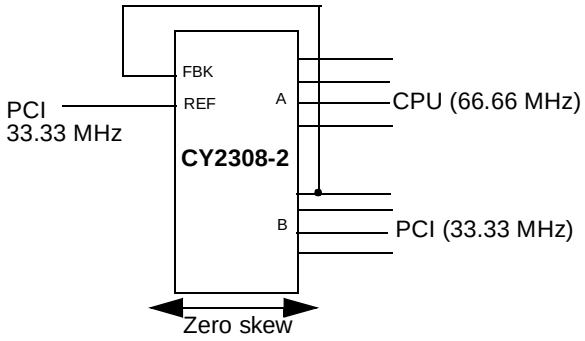

Figure 14. Sample Application: CY2308-2

Multiple Frequency Clock Distribution Network Using Cascaded CY2308-x

Cascading CY2308-2,3,4s can create some interesting clock distribution networks with multiple frequencies having low skew between them. An example is shown in *Figure 15*. Here a 20 MHz input signal is used to generate multiple copies of 10, 20, 40 and 80 MHz signals, all phase aligned with each other and with zero skew between them. Cascading PLLs in this fashion may increase jitter on a system. However good V_{DD} filtering as described in the section on “Suggested Layout” will reduce this problem. With three CY2308s cascaded on our test boards, short term (cycle to cycle) jitter was found to be within specification.

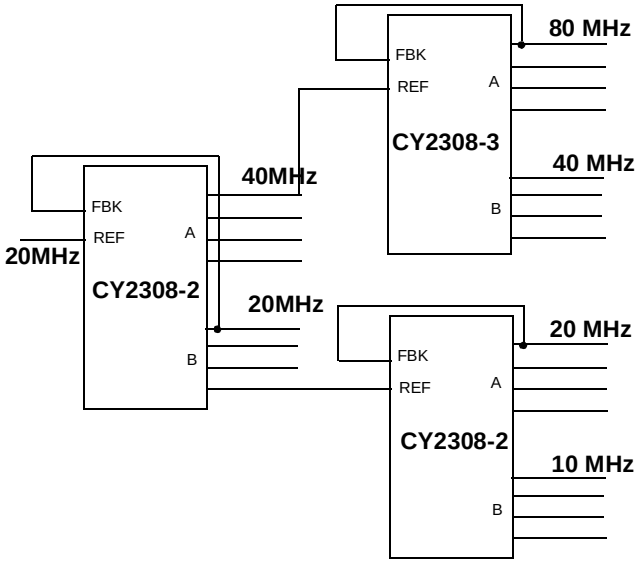

Figure 15. CY2308-x Clock Tree

Reducing EMI/EMC Using CY2308-2,-3,-4:

In an earlier application we discussed reducing EMI/EMC, by reducing the swing from 5V (rail-to-rail) to 3.3V (rail-to-rail) with a CY2308. The CY2308-2,-3,-4 provide an additional way to reduce EMI/EMC from long transmission lines, by reducing the frequency of distributed signals.

Say, for example, a certain load requires a high frequency like 100 MHz and the load is physically located far from the clock source. Normally, to provide the clock, a 100 MHz signal would need to be generated at the source and delivered to the load over a long transmission line (switching at 100 MHz and generating substantial EMI/EMC). An alternate solution, shown in *Figure 16*, is to generate a 25/50 MHz signal at the source, transmit this lower frequency over the transmission line and multiply the frequency up to 100 MHz at the load using the CY2308-2,-3,-4. The EMI/EMC would be reduced since the long traces are now switching at a lower frequency.

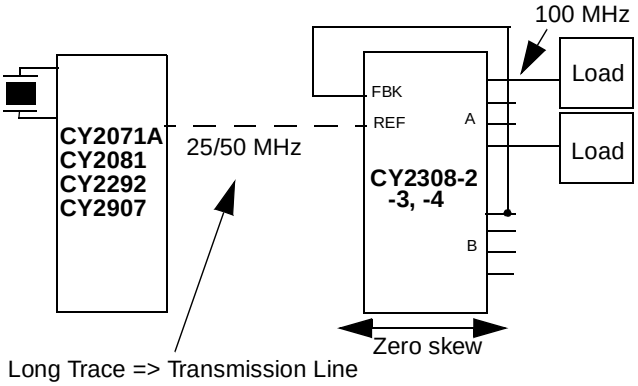

Figure 16. Reducing EMI with CY2308-2,3,4

Synthesizing/Generating Frequencies Greater than 80 MHz at 3.3V

Cypress General purpose clock synthesizers need to be driven from a 5V supply to generate an output frequency above 80 MHz. With 3.3V applications now running at high frequencies, there is a need to generate these frequencies with a 3.3V supply.

The application in *Figure 17* is similar to the previous example and shows how a CY2308-2,-3,-4 can be used to multiply frequencies up and generate frequencies greater than 80 MHz at 3.3V.

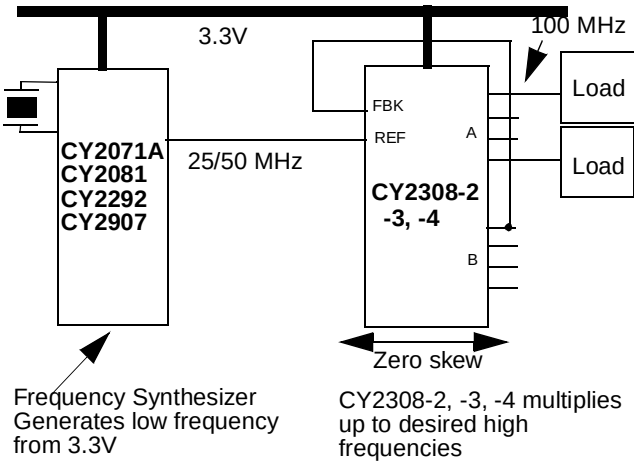

Figure 17. Frequencies Greater than 80 MHz at 3.3V

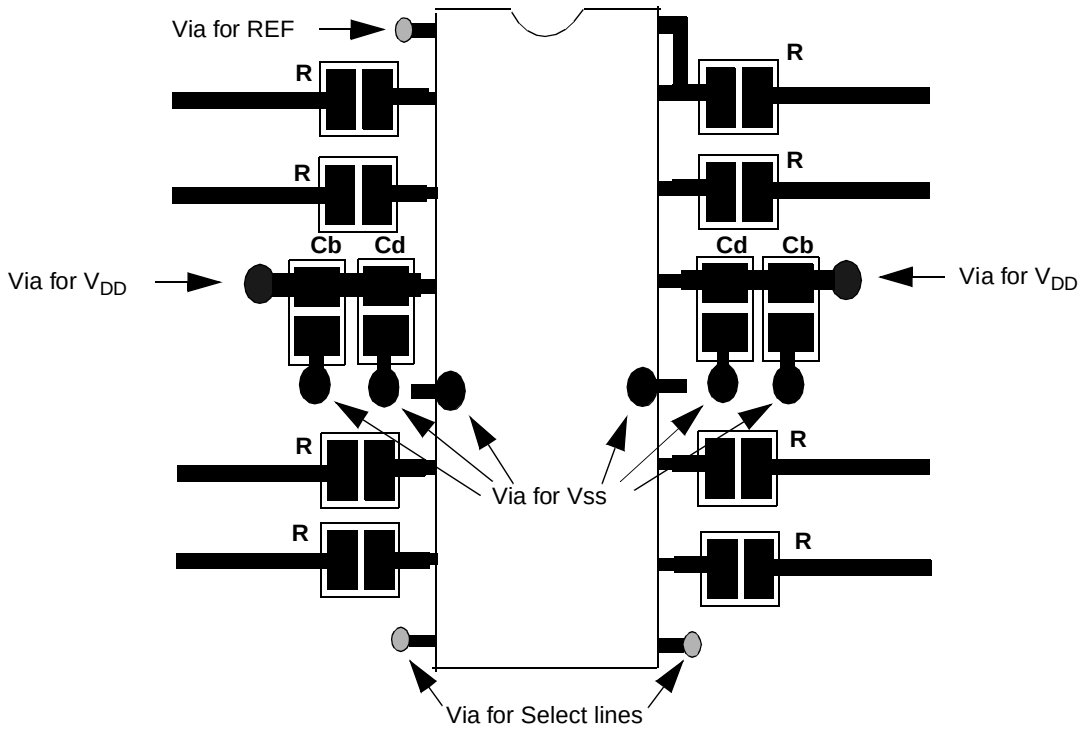

Figure 18. Layout Recommendations for the CY2308

Suggested Layout Recommendations for CY2308

1. It is also suggested that both a 100-pF and a 0.01-µF capacitor be placed between V_{DD} and V_{SS} on pins 4 and 12. The 0.01-µF Capacitor will be used as a Bypass Capacitor to prevent power supply droop when the clock buffer is switching all outputs simultaneously with maximum capacitive load. The 100-pF cap is used for decoupling noise from the power supply. Decoupling and bypass capacitors should be placed between the V_{DD} pin and the V_{DD} Via.
2. Use as many Vias as possible to ensure both solid V_{DD} and V_{SS} layers on the component level. It is recommended that larger Vias be used on V_{DD} and V_{SS} pins. It is also suggested to use individual Vias to V_{SS} on all decoupling capacitors, bypass capacitors and V_{SS} pins, as shown in *Figure 18*. Use of good quality surface mount capacitors is recommended.
3. A series damping resistor used to prevent wave reflection is suggested for each of the clocks being driven by the CY2308. This value can be between 10 and 75 ohms depending on the impedance of the circuit board traces. Series termination resistors should be placed as close to the output pins as possible

Suggested Routing of Clock Signals:

1. Route clock signals such that the traces do not intersect each other.
2. When driving multiple loads on a single output, either daisy chain the outputs (when distance < 2" at 50 MHz) or route individual traces to each load from as close to the source as possible. When individual traces are used from a single output, each trace should have a separate series termination resistance. See *Figure 19*.

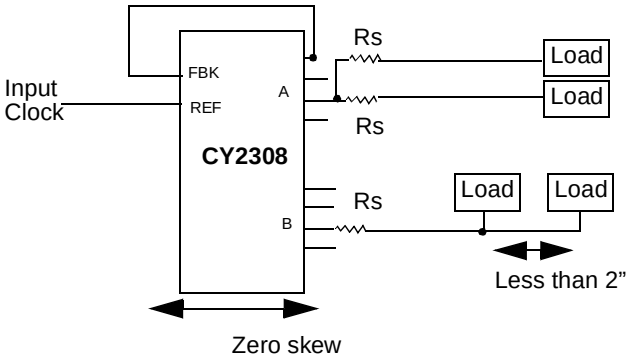

Figure 19. Multiple Outputs

3. Ensure that a minimum number of vias are used on clock signals. Try to route clocks on a single layer.
4. Do not use 90 degree angles when routing clocks. Use smooth curving traces as much as possible.
5. Ensure that a solid ground plane is on the layer adjacent to the clock trace routing layer.