

83C51KB

HIGH PERFORMANCE KEYBOARD MICROCONTROLLER

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| <ul style="list-style-type: none"> ■ Direct Drive LED Outputs <ul style="list-style-type: none"> — Four Pins (P3.7:4) — 13 mA Typical Current Sink Capability ■ 20 pF Cap On-chip for RC Resonator <ul style="list-style-type: none"> — Frequency Selectable (4-6 MHz) ■ 8 Dedicated Key Scan Input (KSI) Pins <ul style="list-style-type: none"> — Schmitt-trigger Inputs — External Interrupt — Level Detect Interrupt Mode for Automatic Power-down Exit ■ 16 Dedicated Key Scan Output (KSO) Pins with Quasi-bidirectional Port Drivers <ul style="list-style-type: none"> — No External Resistor Required — Located on P0.7:0 and P2.7:0 ■ 4-Kbyte On-chip ROM Memory | <ul style="list-style-type: none"> ■ 128-byte On-chip RAM Memory ■ Clock/Data Drivers to Motherboard <ul style="list-style-type: none"> — Strong Pullup Drivers for Keyboard Cable Communication — 8X42 Compatible Interface — Selectable external interrupt for Clock ■ ONCE mode (On-chip Emulation) ■ Power-on Reset Mode <ul style="list-style-type: none"> — Automatic Operation ■ 5 Volt D.C. Operation ■ Reduces Manufacturing Cost by Reducing Overall Component Count ■ Configurable Timer (16 bit or 2 by 8 Bit) ■ Uses Industry Standard Design Tools ■ Control Oriented Instruction Set ■ Industry Standard Architecture |
|--|--|

The 83C51KB is a highly integrated keyboard microcontroller for the standard and advanced desktop keyboard industry. The integration of external components into the microcontroller reduces overall keyboard control system manufacturing cost in terms of the number of components used, the amount of PCB space required, reduced inventory, and a reduction in required assembly activities. In addition, the integration reduces the number and amount of software routines needed for signal debounce and input status poll operation. There is a resultant reduction in CPU overhead as well as on-chip memory requirements. The 83C51KB product line is manufactured with Intel state of the art complimentary high-performance metallic oxide semiconductor (CHMOS) design rules.

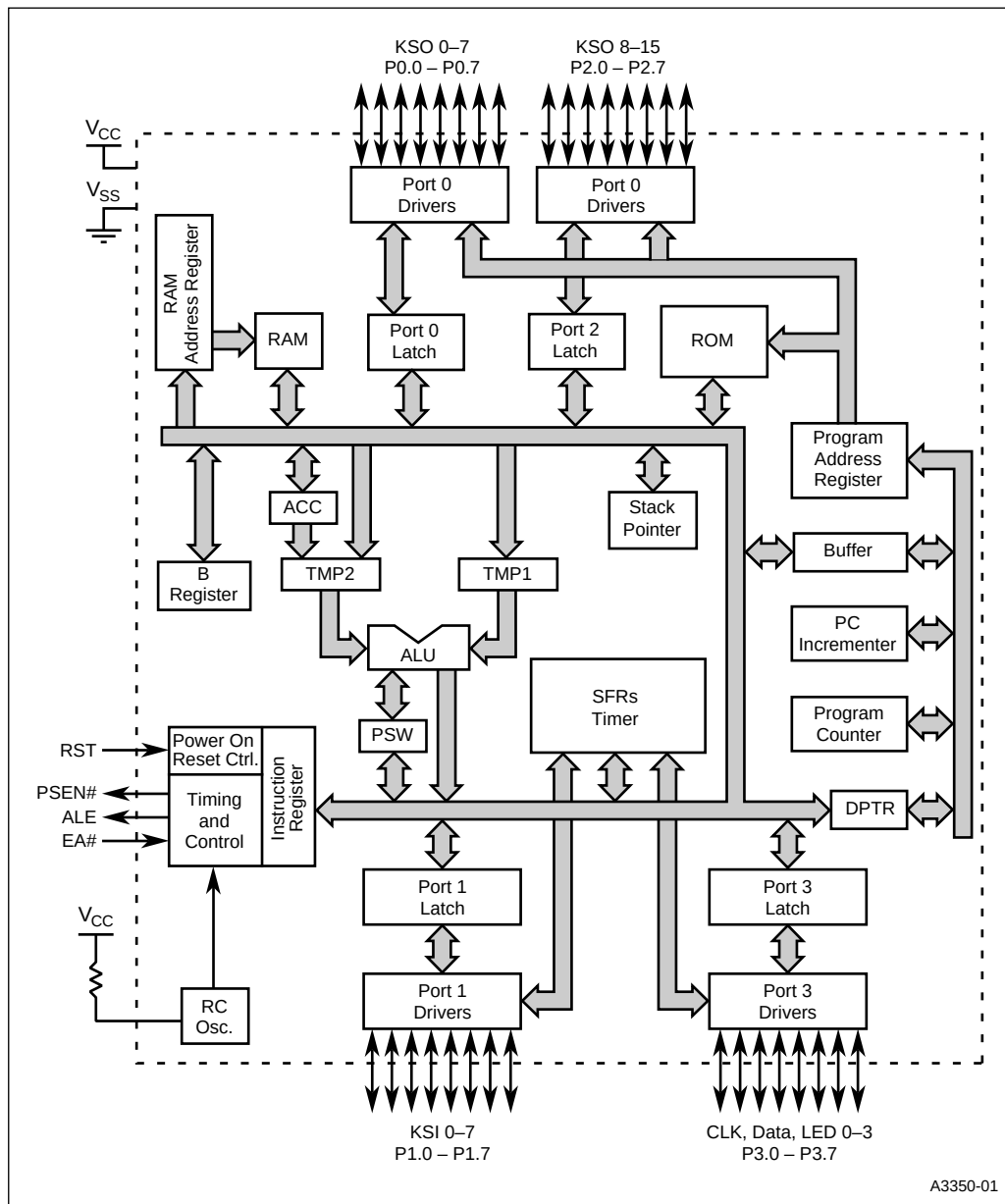


Figure 1. 83C51KB Block Diagram

1.0 TEMPERATURE RANGE

With the commercial (standard) temperature marking, this product line operates over the temperature range 0°C to +70°C.

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change depending on operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

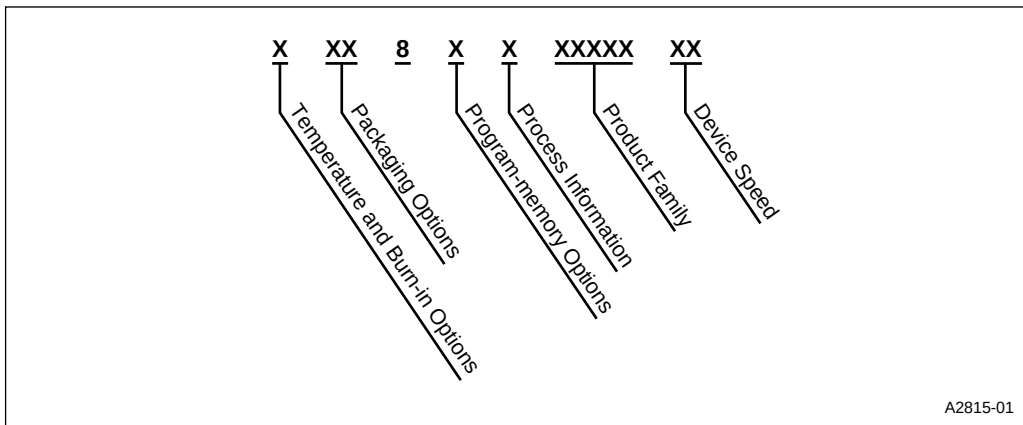
2.0 PROCESS INFORMATION

This device is manufactured on a complimentary high-performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

Table 1. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
40-lead PDIP	70°C/W	25°C/W

3.0 83C51KB PACKAGE INFORMATION



The 83C51KB Family Nomenclature

Table 2. 83C51KB Nomenclature Definitions

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	P	Plastic Dual-in-line Package (PDIP)
Program Memory Options	3	Factory programmed ROM
Process Information	C	CHMOS
Product Family	51	MCS 51 Compatible Product Family
Device Memory Options	KB	128 bytes RAM
		4 Kbytes ROM
Device Speed	no mark	4-6 MHz

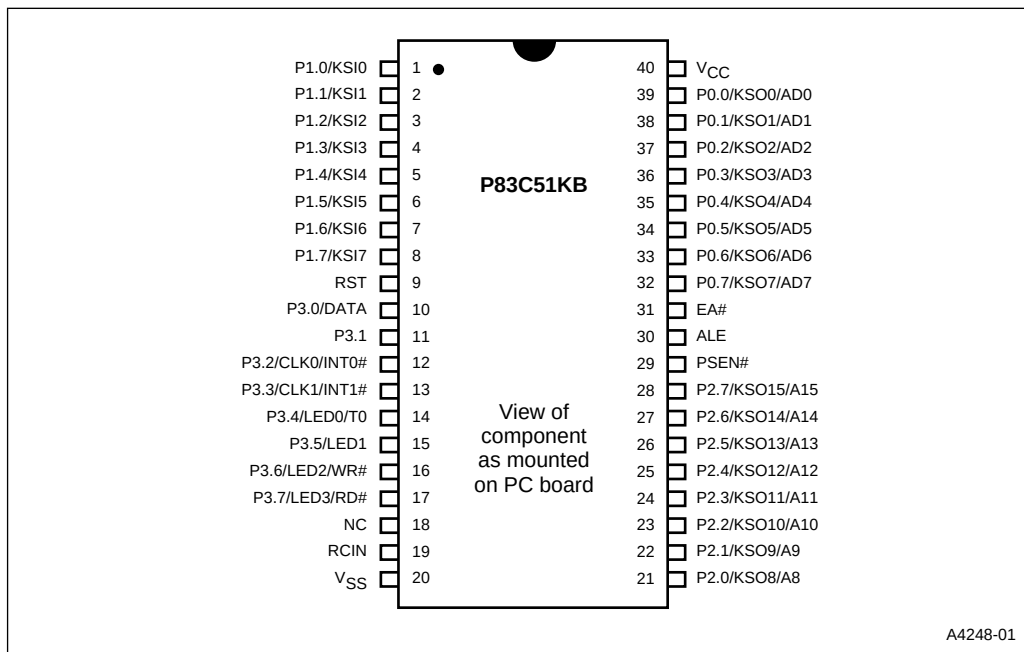


Figure 2. 83C51KB 40-pin DIP Diagram

4.0 83C51KB MEMORY

Table 3. 83C51KB Memory Map

Code Memory	Description	Notes
FFFFH 0000H	External code memory	4
0FFFH 0000H	4-Kbyte on-chip code memory array.	

Data Memory	Description	
FFFFH 0000H	External data memory	2, 3
00FFH 0080H	Special function registers	1
007FH 0020H	On-chip RAM	5
001FH 0000H	4 banks of general purpose registers, R0-R7	

NOTE:

1. The special function registers (SFRs) are accessible by direct addressing only.
2. Data in this area is accessible by indirect addressing only.
3. RD#/WR# active for these external data addresses.
4. PSEN# active for the external code addresses.
5. Addresses 20H through 2FH are bit addressable.

5.0 SIGNAL DESCRIPTION

Table 4. 40-pin DIP Signals Arranged by Name

Keyboard		Keyboard	
Name	Pin	Name	Pin
P0.7/KSO7/AD7	32	P 1.0/KSI0	1
P0.6/KSO6/AD6	33	P1.1/KSI1	2
P0.5/KSO5/AD5	34	P1.2/KSI2	3
P0.4/KSO4/AD4	35	P1.3/KSI3	4
P0.3/KSO3/AD3	36	P1.4/KSI4	5
P0.2/KSO2/AD2	37	P1.5/KSI5	6
P0.1/KSO1/AD1	38	P1.6/KSI6	7
P0.0/KSO0/AD0	39	P1.7/KSI7	8
P2.7/KSO15/A15	28	P3.0/DATA	10
P2.6/KSO14/A14	27	P3.1	11
P2.5/KSO13/A13	26	P3.2/CLK0/INT0#	12
P2.4/KSO12/A12	25	P3.3/CLK1/INT1#	13
P2.3/KSO11/A11	24	P3.4/LED0/T0	14
P2.2/KSO10/A10	23	P3.5/LED1	15
P2.1/KSO9/A9	22	P3.6/LED2/WR#	16
P2.0/KSO8/A8	21	P3.7/LED3/RD#	17

Chip Control	
Name	Pin
RCIN	19
RST	9
ALE	30
PSEN#	29
EA#	31

Power & Ground	
Name	Pin
V _{CC}	40
V _{SS}	20

Table 5. 40-pin DIP Signals Arranged by Pin Number

Pin	Name	Pin	Name
1	P 1.0/KSI0	21	P2.0/KSO8/A8
2	P1.1/KSI1	22	P2.1/KSO9/A9
3	P1.2/KSI2	23	P2.2/KSO10/A10
4	P1.3/KSI3	24	P2.3/KSO11/A11
5	P1.4/KSI4	25	P2.4/KSO12/A12
6	P1.5/KSI5	26	P2.5/KSO13/A13
7	P1.6/KSI6	27	P2.6/KSO14/A14
8	P1.7/KSI7	28	P2.7/KSO15/A15
9	RST	29	PSEN#
10	P3.0/DATA	30	ALE
11	P3.1	31	EA#
12	P3.2/CLK0/INT0#	32	P0.7/KSO7/AD7
13	P3.3/CLK1/INT1#	33	P0.6/KSO6/AD6
14	P3.4/LED0/T0	34	P0.5/KSO5/AD5
15	P3.5/LED1	35	P0.4/KSO4/AD4
16	P3.6/LED2/WR#	36	P0.3/KSO3/AD3
17	P3.7/LED3/RD#	37	P0.2/KSO2/AD2
18	NC	38	P0.1/KSO1/AD1
19	RCIN	39	P0.0/KSO0/AD0
20	V _{SS}	40	V _{CC}

Table 6. 83C51KB Signal Description

Signal Name	Type	Description	Alternate Function
A15:8 [†]	O	Address Signals . Upper address lines for the external bus. These signals are normally used for the KSO15:8 scan function and are not available for external memory access in a keyboard application. (See KSO signals).	KSO.15:8 P2.15:8
AD7:0 [†]	I/O	Address/Data Signals . Multiplexed lower address and data signals for external memory. These signals are normally used for the KSO7:0 scan function and are not available for external memory access in a keyboard application. (See KSO)	KSO.7:0 P0.7:0
ALE [†]	O	Address Latch Enable . ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. Since these external address signals are normally used for the KSO scan function, the ALE should not be used for external memory access in a keyboard application. ALE can be disabled when not used for external memory access by setting bit 0 of SFR AUXR at address 8EH.	
CLK1:0 P3.3:2	I/O	Clock signal . Either P3.2 or P3.3 is configurable with a 1.8K Ω pullup and with external interrupt INT0# or INT1# and used as keyboard CLK signal.	INT1:0#
DATA P3.0	I/O	DATA signal . P3.0 is configurable with a 1.8K Ω pullup and used as keyboard Data signal..	
EA#	I	External Access . Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. EA# should always be strapped to V _{CC} for keyboard applications using the 83C51KB.	
INT1:0# [†]	I	External Interrupts 0 and 1 . These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#. For keyboard applications, these signals are normally used for the CLK signals. (See KSIINT and CDPU bits in the PCON register)	CLK1:0 P3.3:2
KSI7:0 P1.7:0	I/O	Keyboard Scan Inputs . Application specific keyboard signals.	
KSO15:0 P2.15:8 P0.7:0	I/O	Keyboard Scan Outputs . The KSO signals are application specific to keyboard scan functions.	
LED3:0 P3.7:4	I/O	Light Emitting Diode Drivers . The LED signals are specifically designed to drive LEDs connected to V _{cc} directly (see D.C. Characteristics). The alternate functions are not available for keyboard applications.	RD#, WR#, T0
N/C	—	No Connection Signal . This signal is to be unconnected.	
P0.7:0 [†]	I/O	Port 0 . This is an 8-bit quasi-bidirectional I/O port (see KSO signals, see also AD7:0).	AD7:0
P1.7:0	I/O	Port 1 . This is an 8-bit quasi-bidirectional I/O port (see KSI signals).	
P2.7:0	I/O	Port 2 . This is an 8-bit quasi-bidirectional I/O port (see also A15:8).	A15:8

[†] The descriptions of RD#, WR#, ALE, P^{SEN}#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

Table 6. 83C51KB Signal Description

Signal Name	Type	Description	Alternate Function
P3.7:0	I/O	Port 3. This is an 8-bit quasi-bidirectional I/O port (see CLK1:0, DATA, LED3:0).	
PSEN# [†]	O	Program Store Enable. This output is asserted for external program memory fetch operations. It is not available for keyboard applications.	—
RCIN	I	Resonant Clock Input. RC resonator generated by connecting 1% precision resistor to V _{CC} or provide an external clock input from an external clock device.	
RD# [†]	O	Read . Read signal output for external data memory read operations. It is not available for keyboard applications.	LED3
RST	I	Reset. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation. This signal is input only. When power is applied to the chip, the internal reset signal remains high for approximately 80ms to 260ms (see the datasheet for current specifications). The reset circuit then deactivates and does not re-activate unless V _{CC} drops below the crossover at approximately 3VDC.	—
V _{CC}	PWR	Supply Voltage. Connect this pin to the +5V supply voltage.	—
V _{SS}	GND	Circuit Ground. Connect this pin to ground.	—
WR# [†]	O	Write. Write signal output for external data memory write operations. It is not available for keyboard applications.	LED2

[†] The descriptions of RD#, WR#, ALE, P'SEN#, A15:8/P2.7:0 and AD7:0/P0.7:0 are documented for the standard MCS 51 microcontrollers. They are not used for these functions in keyboard applications.

6.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[†]

Ambient Temperature under Bias:

Commercial	0°C to +70°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin to V _{SS}	-0.5 V to +6.5 V
I _{OL} per I/O Pin.....	15 mA
Power Dissipation	1.5 W

NOTE: Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS[†]

T_A (Ambient Temperature Under Bias):

Commercial	0°C to +70°C
V _{CC} (Digital Supply Voltage)	4.5 V to 5.5 V
V _{SS}	0 V

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

[†]**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

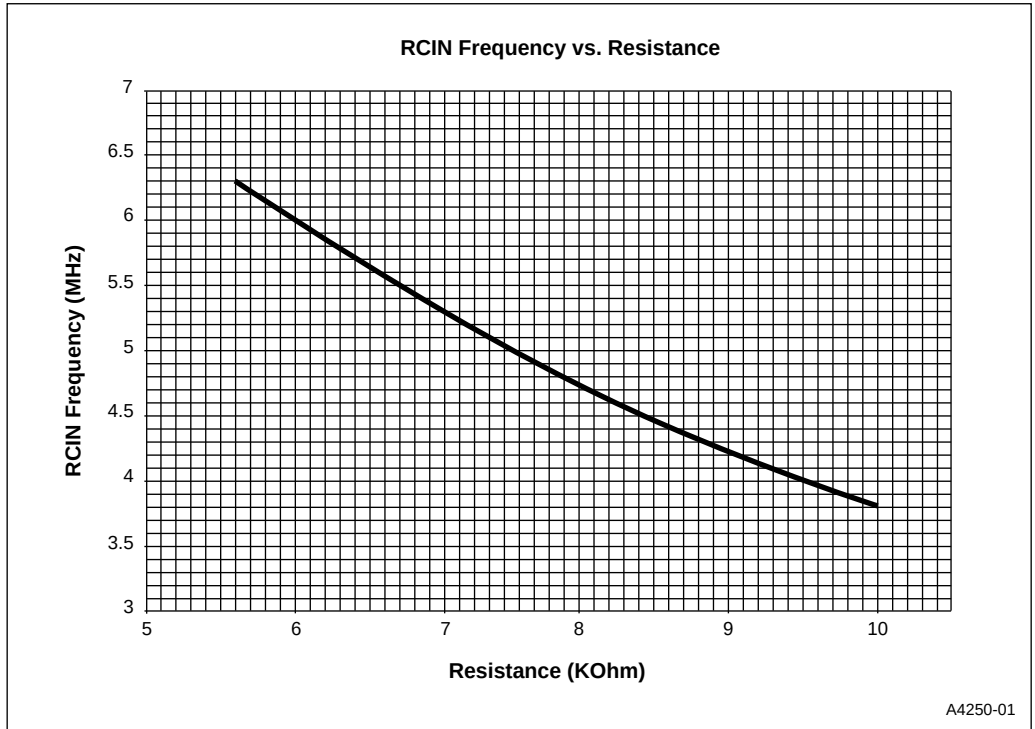


Figure 3. RCIN Frequency

NOTE: RC resonator accuracy is $\pm 5\%$ at fixed V_{CC} and temperature using a 1% external precision resistor.

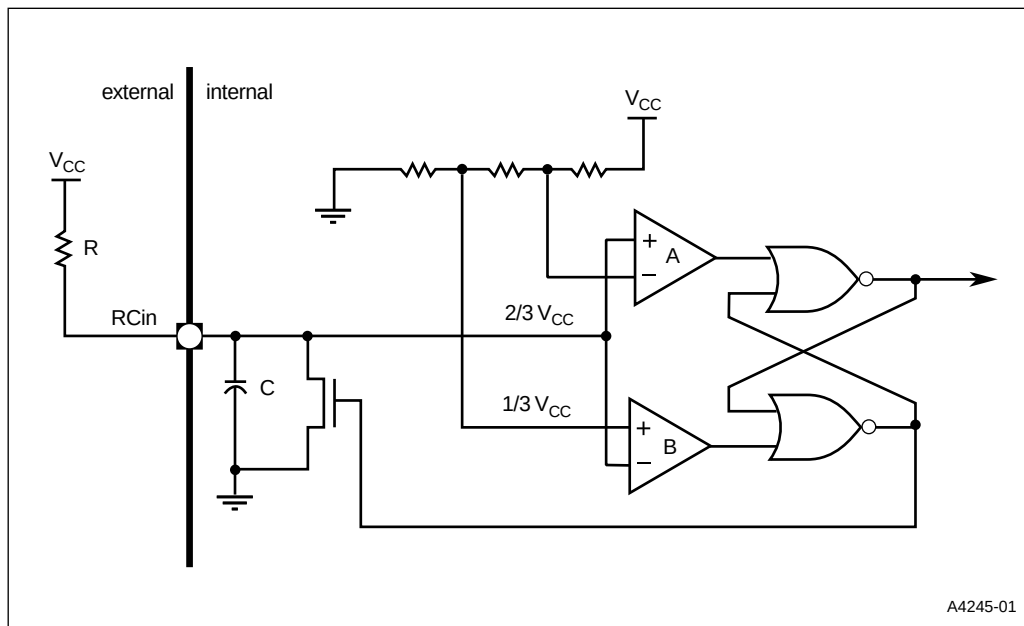


Figure 4. RC Oscillator

6.1 D.C. Characteristics

Table 7. D.C. Characteristics

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
V_{IL}	Input Low Voltage (except EA#, RCIN, RST)	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage RST	0		$0.2 V_{CC} - 0.3$	V	
V_{IL2}	Input Low Voltage EA#	-0.5		0.5	V	
V_{IL3}	Input Low Voltage RCIN			$V_{CC}/3$	V	
V_{IH}	Input High Voltage (except EA#, RCIN, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (EA#, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{IH2}	Input High Voltage RCIN	$2V_{CC}/3$				$I_{IH} = 8 \text{ mA}$ when external clock source is used on RCIN
V_{OL}	Output Low Voltage (Port 0, 1, 2, 3, ALE, PSEN# except P3.4/LED0, P3.5/LED1, P3.6/LED2, P3.7/LED3)			0.3 0.45 1.0	V	$I_{OL} = 200 \mu\text{A}$ $I_{OL} = 3.2 \text{ mA}$ $I_{OL} = 7.0 \text{ mA}$ (note 2,3)
I_{OL}	Output Low Current (P3.4/LED0, P3.5/LED1, P3.6/LED2, P3.7/LED3 only)	6	13	22	mA	$V_{OL} = 3.0 \text{ V}$
V_{OH}	Output High Voltage (Port 0, 1, 2, 3, ALE, PSEN#, except P3.0, P3.2, P3.3)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	$I_{OH} = -25 \mu\text{A}$ $I_{OH} = -65 \mu\text{A}$ $I_{OH} = -100 \mu\text{A}$ (note 4)

NOTE:

- Typical values are obtained using $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$ and are not guaranteed.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3: 10mA
Maximum I_{OL} per Port Pin—P3.4-P3.7: 22mA
Maximum I_{OL} per 8-bit port—Port 0-2: 15mA
Ports 3: 95mA
Maximum Total I_{OL} for All Output Pins: 110mA

If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.
- Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the $0.9 V_{CC}$ specification when the address lines are stabilizing.

Table 7. D.C. Characteristics (Continued)

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
V _{OH1}	Output High Voltage (P3.0, P3.2, P3.3 without 1.8K Ohm pullup)	V _{CC} -0.3 V _{CC} -0.7 V _{CC} -1.5			V	I _{OH} = -8 μA I _{OH} = -25 μA I _{OH} = -50 μA
V _{OH2}	Output High Voltage (P3.0, P3.2, P3.3 with 1.8K Ohm pullup)	V _{CC} -0.3 V _{CC} -0.7 V _{CC} -1.5			V	I _{OH} = -0.15 mA I _{OH} = -0.50 mA I _{OH} = -1.0 mA
R _{RST}	Reset Pulldown Resistor	40		225	K Ohm	
R _{CD}	Pull Up Resistance (P3.0, P3.2, P3.3 with 1.8K Ohm pullup)	1.2	1.8	2.9	K Ohm	
C _{IO}	Pin Capacitance		10		pF	@1MHz, 25°C
I _{IL}	Logical 0 Input Current (Port 0, 1, 2, 3, except P3.0, P3.2, P3.3)			-50	μA	V _{IN} =0.45V
I _{IL1}	Logical 0 Input Current (P3.0, P3.2, P3.3 without 1.8K Ohm pullup)			-250	μA	V _{IN} =0.45V
I _{IL2}	Logical 0 Input Current (P3.0, P3.2, P3.2 with 1.8K Ohm pullup)	-1.5		-4.5	mA	V _{IN} =0.45V
I _{TL}	Logical 1-to-0 Transiton Current (Port 0, 1, 2, 3)			-650	μA	V _{IN} =2.0V
I _{TL1}	Logical 1-to-0 Transition Current (P3.0, P3.2 or P3.3 with 1.8K Ohm pullups)			-4.5	mA	V _{IN} = 2.0V

NOTE:

1. Typical values are obtained using $V_{CC}=5.0V$, $T_A=25^{\circ}C$ and are not guaranteed.
2. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:

Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3:	10mA
Maximum I_{OL} per Port Pin—P3.4-P3.7:	22mA
Maximum I_{OL} per 8-bit port—Port 0-2:	15mA
Ports 3:	95mA
Maximum Total I_{OL} for AllOutput Pins:	110mA

If I_{OL} exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

3. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.
4. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

Table 7. D.C. Characteristics (Continued)

Symbol	Parameter	Min	Typical (note 1)	Max	Unit	Test Condition
I_{CC}	Power Supply Current: Active Mode at 6MHz Idle Mode at 6MHz Power Down Mode		7	12	mA	RST, EA# to V_{CC}
			2	5	mA	RST, EA# to V_{SS}
			10	50	μA	RST, EA# to V_{SS} (RCIN pin to external resistor, all other pins are no connect)
V_{POR}	Power on reset crossover	2.4	3	3.6	V	

NOTE:

- Typical values are obtained using $V_{CC}=5.0V$, $T_A=25^{\circ}C$ and are not guaranteed.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follow:
Maximum I_{OL} per Port Pin—Port 0, 1, 2, P3.1-P3.3: 10mA
Maximum I_{OL} per Port Pin—P3.4-P3.7: 22mA
Maximum I_{OL} per 8-bit port—Port 0-2: 15mA
Ports 3: 95mA
Maximum Total I_{OL} for AllOutput Pins: 110mA

If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4V to be superimposed on the low level outputs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify signals with a Schmitt Trigger, or CMOS-level input logic.
- Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

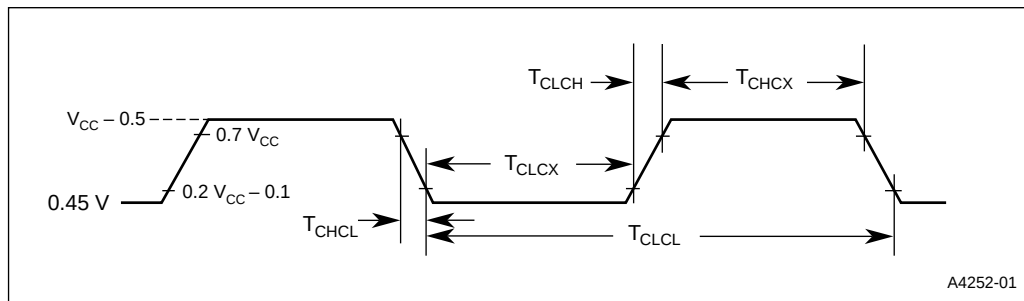


Figure 5. External Clock Drive

6.2 A.C. Characteristics

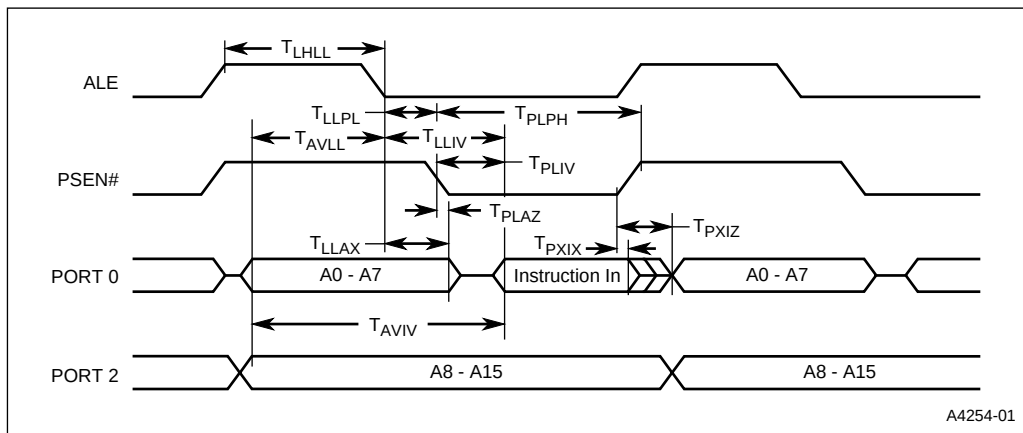
Table 8. A.C. Characteristics (Note 1, 2)

Symbol	Parameter	Min	Max	Unit
F _{OSC}	RCIN Frequency	4	6	MHz
T _{OSC}	1/Fosc	166.7	250	ns
T _{LHLL}	ALE Pulse Width	2Tosc - 50		·ns
T _{AVLL}	Address Valid to ALE Low	Tosc - 50		·ns
T _{LLAX}	Address Hold after ALE Low	Tosc - 40		·ns
T _{LLIV}	ALE Low to Valid Instruction In		4Tosc - 80	ns
T _{LLPL}	ALE Low to PSEN# Low	Tosc - 40		ns
T _{PLPH}	Psen# Pulse Width	3Tosc - 60		ns
T _{PLIV}	Psen# Low to Valid Instruction In		3Tosc - 90	ns
T _{PXIX}	Input Instruction Hold after PSEN#	0		ns
T _{PXIZ}	Input Instruction Float after PSEN#		Tosc - 20	ns
T _{AVIV}	Address Valid to Valid Instruction In		5Tosc - 90	ns
T _{PLAZ}	Psen# Low to Address Float		20	ns
T _{RLRH}	RD# Pulse Width	6Tosc - 120		ns
T _{WLWH}	Write# Pulse Width	6Tosc - 120		ns
T _{RLDV}	RD# Low to Valid Data In		5Tosc - 150	ns
T _{RHDX}	Input Data Hold after RD# High	0		ns
T _{RHDZ}	Input Data Float after RD# High		2Tosc - 45	ns
T _{LLDV}	ALE Low to Valid Data In		8Tosc - 130	ns
T _{AVDV}	Address Valid to Valid Data In		9Tosc - 145	ns
T _{LLWL}	ALE Low to RD# or WR# Low	3Tosc - 70	3Tosc + 70	ns
T _{AVWL}	Address Valid to WR# Low	4Tosc - 150		ns
T _{QVWX}	Output Data Valid before WR#	Tosc - 70		ns
T _{QVWH}	Output Data Valid to WR# High	7Tosc - 170		ns
T _{WHQX}	Output Data Hold after WR# High	Tosc - 60		ns
T _{RLAZ}	RD# Low to Address Float		0	ns
T _{WHLH}	RD# or WR# High to ALE High	Tosc - 55	Tosc + 40	ns
T _{POR}	Power on reset internal high time (note 3)	80	260	ms

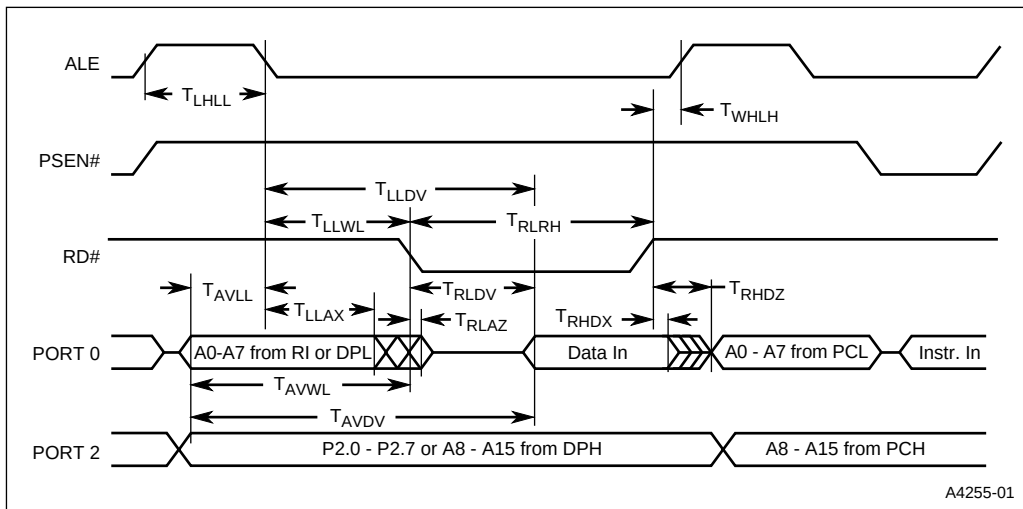
NOTE:

1. Capacitive loading=100pF
2. Rise time and fall time = 20ns for external clock drive
3. T_{POR} timing begins when the voltage exceeds the V_{POR} crossover voltage.

6.3 External Program Memory Read Cycle Waveform



6.4 External Program Memory Read Cycle External Data Memory Read Cycle Waveform



6.5 External Data Memory Read Cycle External Data Memory Write Cycle Waveform

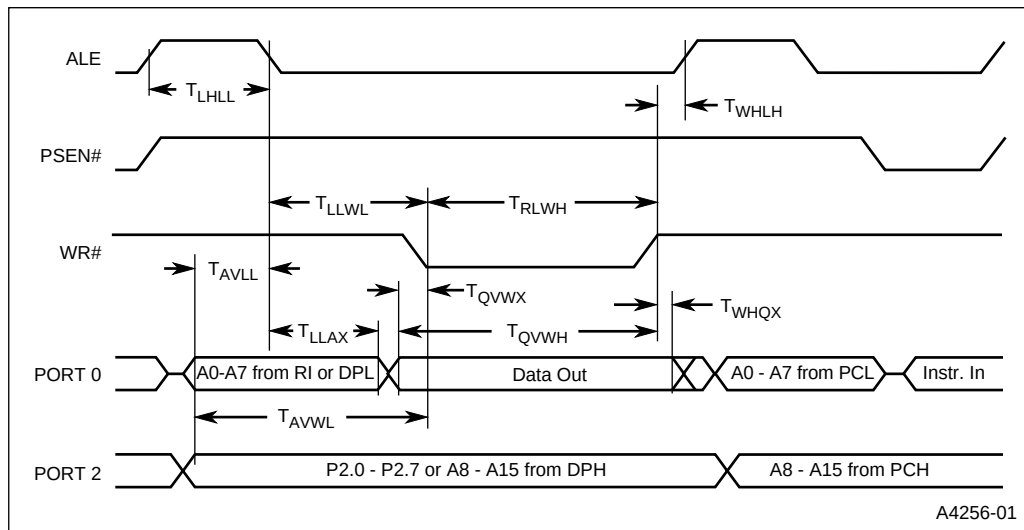


Figure 6. External Data Memory Write Cycle

6.6 Testing Characteristics

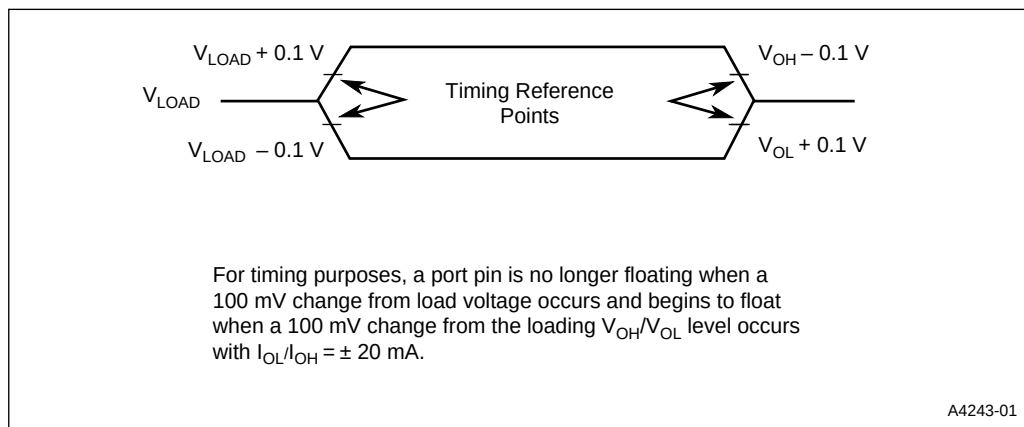
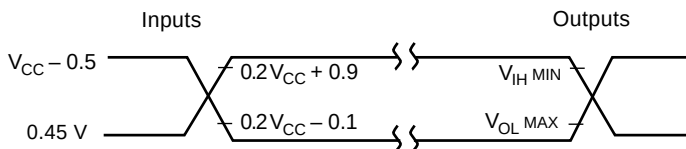


Figure 7. Float Waveforms



AC inputs during testing are driven at $V_{CC} - 0.5\text{V}$ for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at a min of V_{IH} for a logic 1 and V_{OL} for a logic 0.

A4244-01

6.7 A.C. Testing Input, Output Waveforms Signature Byte Information

Valid signature bytes for the 83C51KB are detailed in the following table:

Table 9. 83C51KB Signature Byte Values

TROM Address	Contents	Device Type
30H	89H	Intel Corp.
31H	58H	FX-core
60H	20H	83C51KB