2SJ130(L), 2SJ130(S)

Silicon P-Channel MOS FET

HITACHI

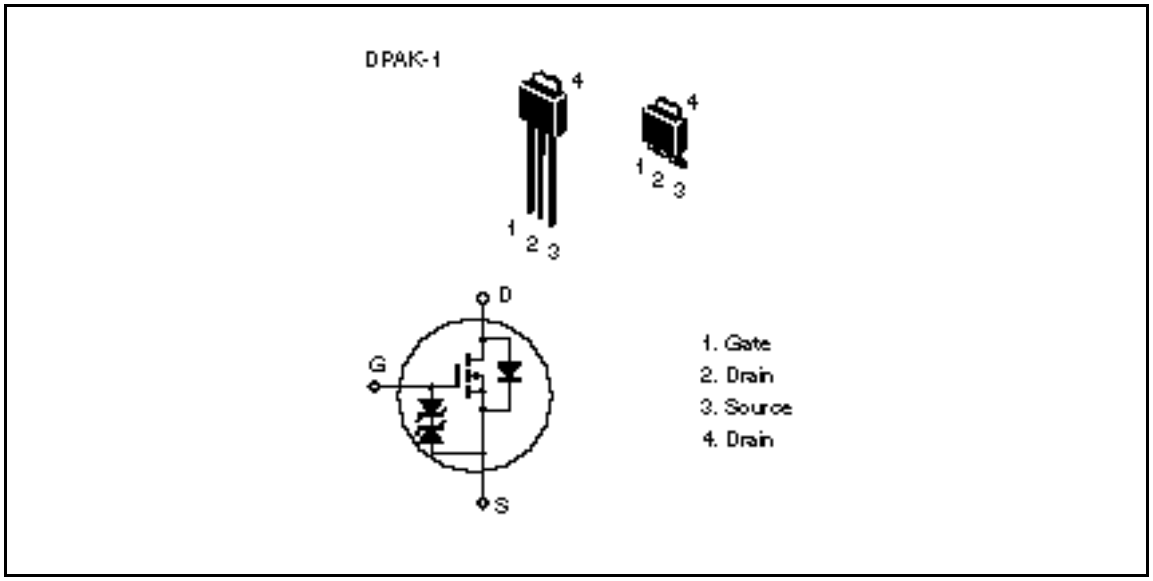
Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator, DC-DC converter and ultrasonic power oscillators

Outline



Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

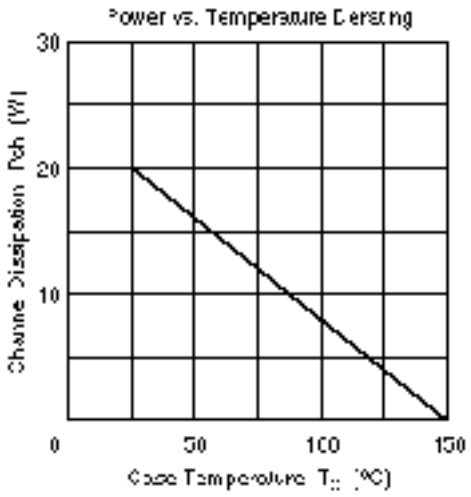
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–300	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–1	A
Drain peak current	$I_{D(pulse)}$	–2	A
Body to drain diode reverse drain current	I_{DR}	–1	A
Channel dissipation	Pch*[1]	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

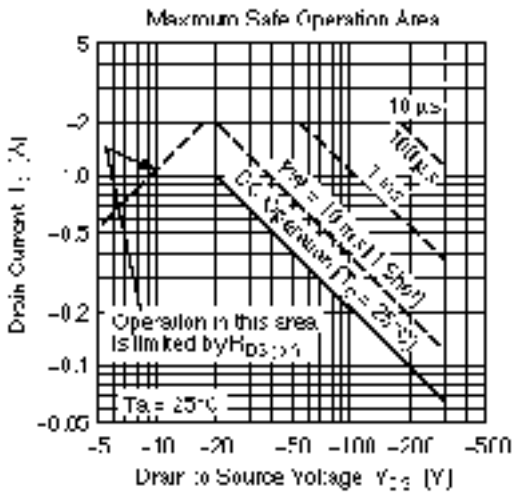
Note: 1. Value at T_C = 25°C

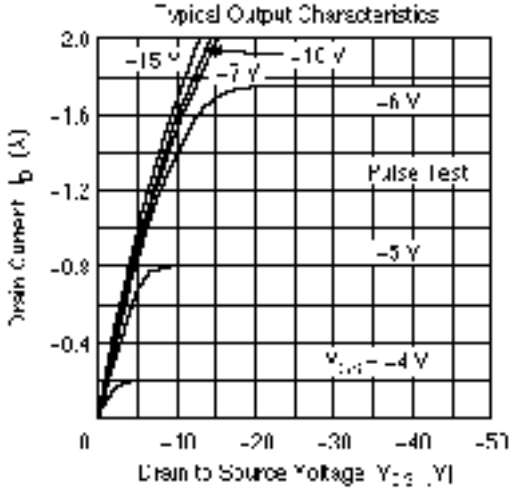
Electrical Characteristics (Ta = 25°C)

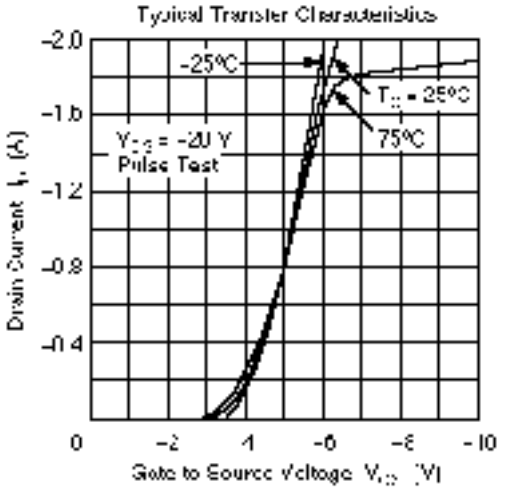
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–300	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–100	µA	V_{DS} = –240 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	8.5	Ω	I_D = –0.5 A, V_{GS} = –10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	0.25	0.4	—	S	I_D = –0.5 A, V_{DS} = –20 V*[1]
Input capacitance	Ciss	—	235	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	65	—	pF	
Reverse transfer capacitance	Crss	—	16	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	I_D = –0.5 A, V_{GS} = –10 V, R_L = 60 Ω
Rise time	t_r	—	25	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –1 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	200	—	ns	I_F = –1 A, V_{GS} = 0, di_F/dt = 50 A/µs

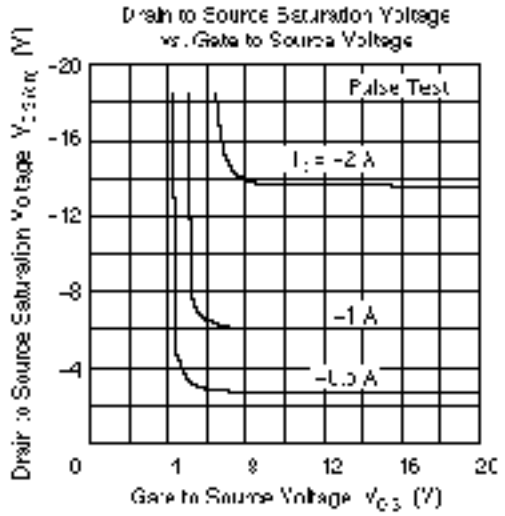
Note: 1. Pulse test

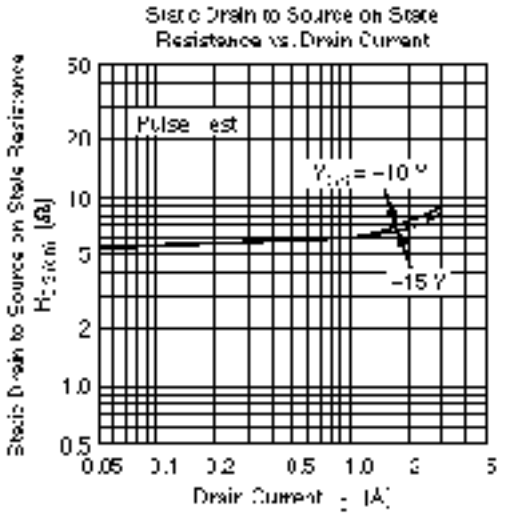

Power vs. Temperature Derating
Channel Dissipation Pch (W)
30
20
10
0
50
100
150
Case Temperature Tc (°C)

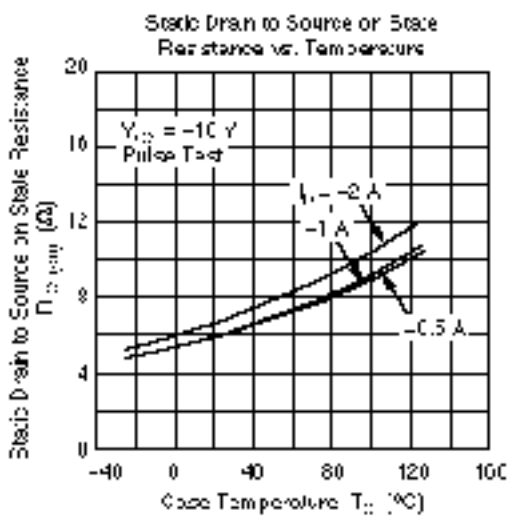

Maximum Safe Operation Area
Drain Current I_D (A)
10 µs
100 µs
1 ms
PW = 10 ms (1 Shot)
D.C. Operation (Tc = 25°C)
Operation in this area is limited by R_DS(on)
Ta = 25°C
-5
-10
-20
-50
-100
-200
-500
Drain to Source Voltage V_DS (V)

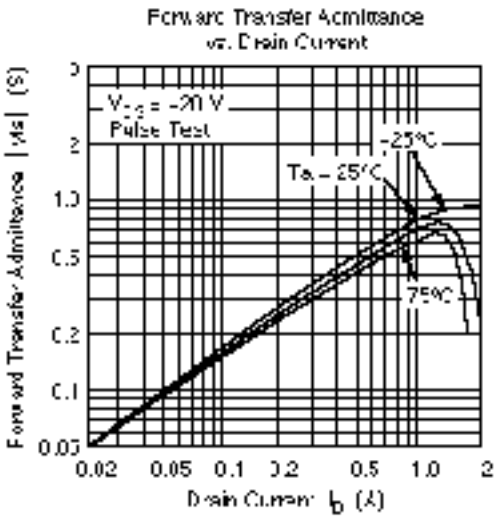

Typical Output Characteristics
Drain Current I_D (A)
-15 V
-10 V
-7 V
-6 V
Pulse Test
-5 V
V_GS = -4 V
2.0
1.6
1.2
0.8
0.4
0
-10
-20
-30
-40
-50
Drain to Source Voltage V_DS (V)

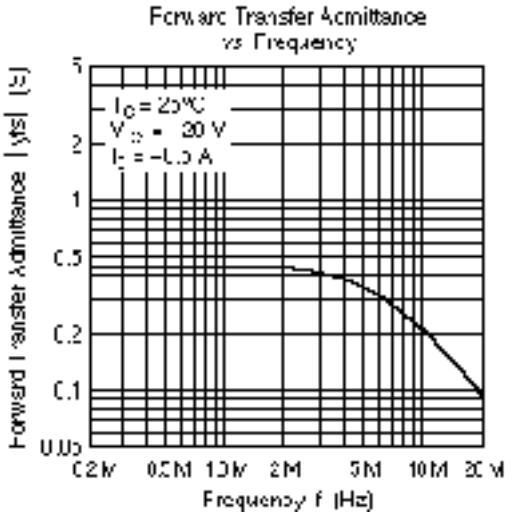

Typical Transfer Characteristics
Drain Current I_D (A)
-25°C
T_C = 25°C
75°C
V_DS = -20 V
Pulse Test
2.0
1.6
1.2
0.8
0.4
0
-2
-4
-6
-8
-10
Gate to Source Voltage V_GS (V)

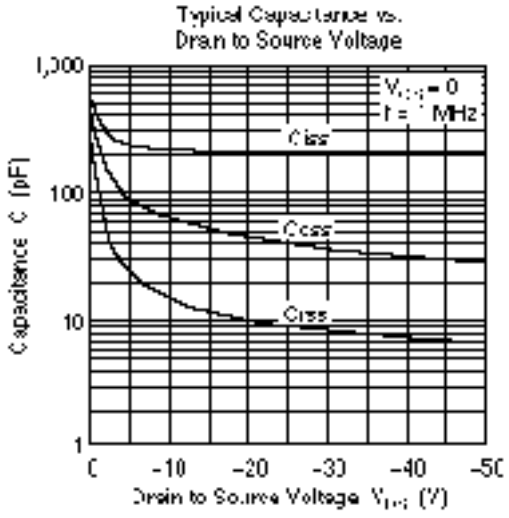

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Drain to Source Saturation Voltage V_DS(on) (V)
Pulse Test
I_D = -2 A
-1 A
-0.5 A
20
16
12
8
4
0
4
8
12
16
20
Gate to Source Voltage V_GS (V)

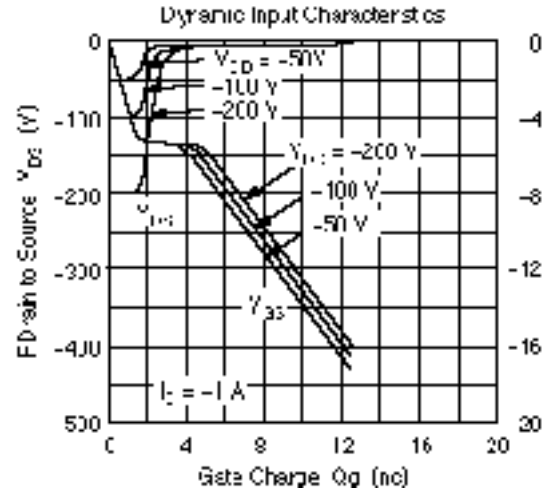

Static Drain to Source on State Resistance vs. Drain Current
Static Drain to Source on State Resistance R_DS(on) (Ω)
Pulse Test
V_GS = -10 V
-15 V
50
20
10
5
2
1.0
0.5
0.05
0.1
0.2
0.5
1.0
2
5
Drain Current I_D (A)

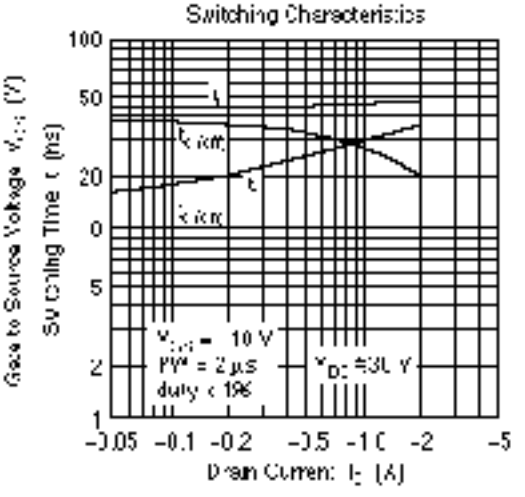

Static Drain to Source on State
Resistance vs. Temperature
Pulse Test
-2 A
-1 A
-0.5 A
Case Temperature

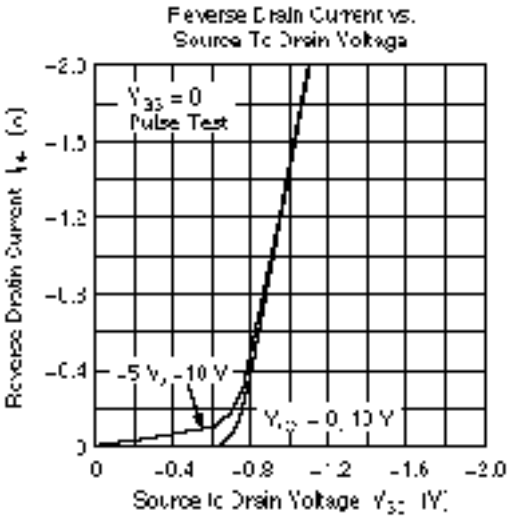

Forward Transfer Admittance
vs. Drain Current
Pulse Test
-25°C
75°C
Drain Current

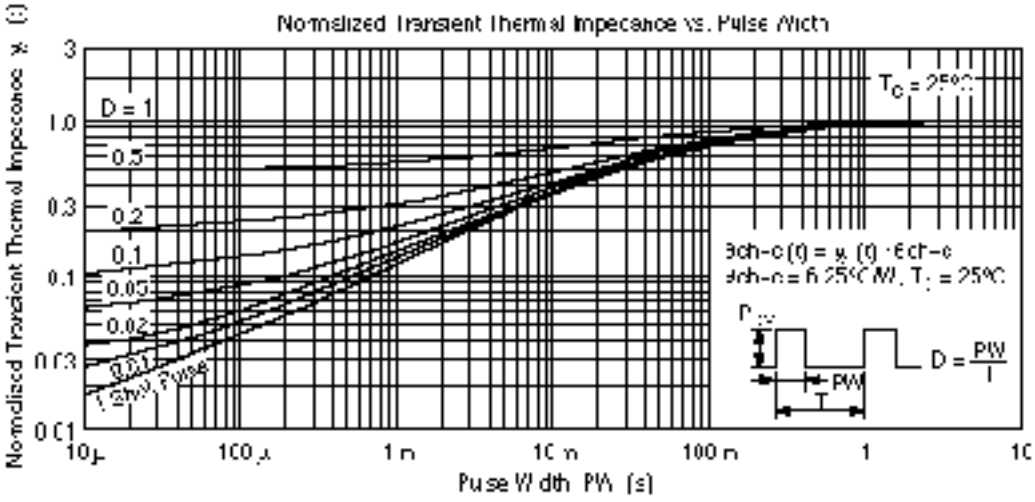

Forward Transfer Admittance
vs. Frequency
Frequency f (Hz)

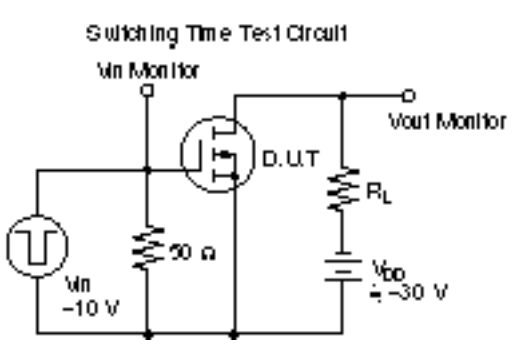

Typical Capacitance vs.
Drain to Source Voltage
Ciss
Coss
Crss
Drain to Source Voltage

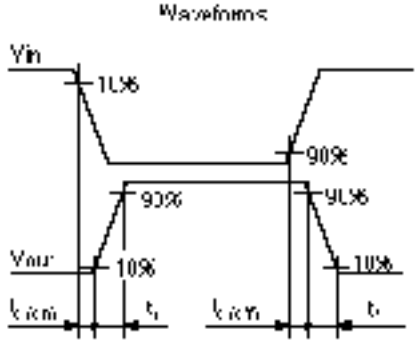

Dynamic Input Characteristics
-50 V
-100 V
-200 V
Gate Charge Qg (nc)


Switching Characteristics
Drain Current


Reverse Drain Current vs.
Source To Drain Voltage
Reverse Drain Current
Source to Drain Voltage
Pulse Test
-5 V, -10 V
0, 10 V
-2.0
-1.6
-1.2
-0.8
-0.4
0


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot Pulse
Pulse Width
3
1.0
0.3
0.1
0.03
0.01
100 µ
1 m
10 m
100 m
1
10


Switching Time Test Circuit
Vin Monitor
Vout Monitor
D.U.T
RL
50 Ω
Vin
-10 V
VDD
~ -30 V


Waveforms
Vin
10%
90%
90%
90%
Vout
10%
10%

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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U.S.A.
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071