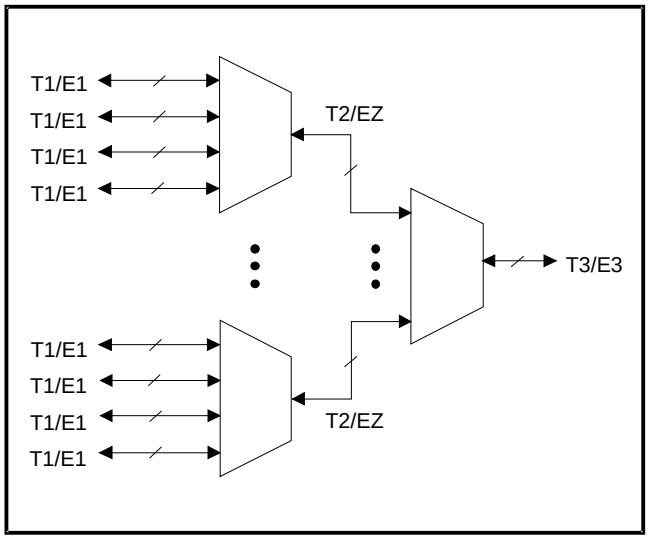
DALLAS SEMICONDUCTOR

DS3112
TEMPE T3 E3 Multiplexer
3.3V T3 / E3 Framer and M13/E13/G.747 MUX

FEATURES

- Operates as M13 or E13 multiplexer or as stand alone T3 or E3 framer
- Flexible multiplexer can be programmed for multiple configurations including:
  - M13 multiplexing (28 T1 lines into a T3 data stream)
  - E13 multiplexing (16 E1 lines into an E3 data stream)
  - E1 to T3 multiplexing (21 E1 lines into a T3 data stream)
- Two T1/E1 drop and insert ports
- T3 C-bit parity mode supported
- B3ZS/HDB3 encoder and decoder
- Generates and detects T3/E3 alarms
- Generates and detects T2/E2 alarms
- Integrated HDLC controller handles LAPD messages without host intervention
- Integrated FEAC controller
- Integrated BERT supports performance monitoring
- T3/E3 and T1/E1 diagnostic (Tx to Rx), line (Rx to Tx), and payload loopback supported
- Non-multiplexed or multiplexed 16-bit control port (with optional 8-bit mode)
- 3.3V supply with 5V tolerant I/O
- Available in 256–lead 1.27 mm pitch BGA package
- IEEE 1149.1 JTAG support

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

DS3112	(0°C to 70°C)
DS3112N	(-40°C to +85°C)

TABLE OF CONTENTS

SECTION 1: INTRODUCTION

The DS3112 TEMPE (**T**3 **E**3 **M**ulti**P**lex**E**r) device can be used either as a multiplexer or a T3/E3 framer. When the device is used as a multiplexer, it can be operated in one of three modes:

M13 – multiplex 28 T1 lines into a T3 data stream
E13 – multiplex 16 E1 lines into a E3 data stream
G747 – multiplex 21 E1 lines into a T3 data stream

See Figures 1A, 1B, and 1C for block diagrams of these three modes. In each of the block diagrams, the receive section is at the bottom and the transmit section is at the top. The receive path is defined as incoming T3/E3 data and the transmit path is defined as outgoing T3/E3 data. When the device is operated solely as a T3 or E3 framer, the multiplexer portion of the device is disabled and the raw T3/E3 payload will be output at the FRD output and input at the FTD input. See Figures 1A and 1B for details.

In the receive path, raw T3/E3 data is clocked into the device (either in a bipolar or unipolar fashion) with the HRCLK at the HRPOS and HRNEG inputs. The data is then framed by the T3/E3 framer and passed through the two step demultiplexing process to yield the resultant T1 and E1 data streams which are output at the LRCLK and LRDAT outputs. In the transmit path, the reverse occurs. The T1 and E1 datastreams are input to the device at the LTCLK and LTDAT inputs. The device will sample these inputs and then multiplex the T1 and E1 datastreams through a two step multiplexing process to yield the resultant T3 or E3 datastream. Then this datastream is passed through the T3/E3 formatter to have the framing overhead added, and the final datastream to be transmitted is output at the HTPOS and HTNEG outputs using the HTCLK output.

The DS3112 has been designed to meet all of the latest telecommunications standards. Table 1A is list of all of the applicable standards for the device.

The TEMPE device has a number of advanced features such as:

- the ability to drop and insert up to two T1 or E1 ports
- an onboard HDLC controller with 256 byte buffers
- an onboard Bit Error Rate Tester (BERT)
- advanced diagnostics to create and detect many different types of errors

See Table 1B for a complete list of main features within the device.

Applicable Standards Table 1A

1. American National Standard for Telecommunications - **ANSI T1.107 – 1995** “Digital Hierarchy - Formats Specification”
2. American National Standard for Telecommunications - **ANSI T1.231 - 199X** – Draft “Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring”
3. American National Standard for Telecommunications - **ANSI T1.231 – 1993** “Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring”
4. American National Standard for Telecommunications - **ANSI T1.404 – 1994** “Network-to-Customer Installation - DS3 Metallic Interface Specification”
5. American National Standard for Telecommunications - **ANSI T1.403 – 1999** “Network and Customer Installation Interfaces – DS1 Electrical Interface”
6. American National Standard for Telecommunications - **ANSI T1.102 – 1993** “Digital Hierarchy – Electrical Interfaces”
7. Bell Communications Research - **TR-TSY-000009**, Issue 1, May 1986 “Asynchronous Digital Multiplexes Requirements and Objectives”
8. Bell Communications Research - **TR-TSY-000191**, Issue 1, May 1986 “Alarm Indication Signal Requirements and Objectives”
9. Bellcore - **GR-499-CORE**, Issue 1, December 1995 “Transport Systems Generic Requirements (TSGR): Common Requirements”
10. Bellcore - **GR-820-CORE**, Issue 1, November 1994 “Generic Digital Transmission Surveillance”
11. Network Working Group Request for Comments - RFC1407, January, 1993 “Definition of Managed Objects for the DS3/E3 Interface Type”
12. International Telecommunication Union (ITU) **G.703**, 1991 “Physical/Electrical Characteristics of Hierarchical Digital Interfaces
13. International Telecommunication Union (ITU) **G.823**, March 1993 “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy”
14. International Telecommunication Union (ITU) **G.742**, 1993 “Second Order Digital Multiplex Equipment Operating at 8448 kbit/s and Using Positive Justification”
15. International Telecommunication Union (ITU) **G.747**, 1993 “Second Order Digital Multiplex Equipment Operating at 6312 kbit/s and Multiplexing Three Tributaries at 2048 kbit/s”
16. International Telecommunication Union (ITU) **G.751**, 1993 “Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34368 kbit/s and Using Positive Justification”
17. International Telecommunication Union (ITU) **G.775**, November 1994 “Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria”
18. International Telecommunication Union (ITU) **O.151**, October 1992 “Error Performance Measuring Equipment Operating at the Primary Rate And Above”
19. International Telecommunication Union (ITU) **O.153**, October 1992 “Basic Parameters for the Measurement of Error Performance at Bit Rates Below the Primary Rate”
20. International Telecommunication Union (ITU) **O.161**, 1984 “In-Service Code Violation Monitors for Digital Systems”

List of Main DS3112 TEMPE Features Table 1B

General Features

- Can be Operated as a Stand Alone T3 or E3 Framer without any M13 or E13 Multiplexing
- T1/E1 FIFOs in the receive direction provide T1/E1 demultiplexed clocks with very little jitter
- Two T1/E1 drop and insert ports
- B3ZS/HDB3 encoder and decoder
- T3 C-Bit Parity mode
- All the receive T1/E1 ports can be clocked out on a common clock
- All the transmit T1/E1 ports can be clocked in on a common clock
- Generates gapped clocks that can be used as demand clocks in unchannelized T3/E3 applications
- T1/E1 ports can be configured into a “loop timed” mode
- T3/E3 port interfaces can be either bipolar or unipolar
- The clock, data and control signals can be inverted to allow a glueless interface to other device
- Loss of transmit and receive clock detect

T3/E3 Framer

- Generates T3/E3 Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI) alarms
- Transmit framer pass through mode
- Generates T3 idle signal
- Detects the following T3/E3 alarms and events: Loss Of Signal (LOS), Loss Of Frame (LOF), Alarm Indication Signal (AIS), Remote Alarm Indication (RAI), T3 idle signal, Change Of Frame Alignment (COFA), B3ZS and HDB3 codewords being received, Severely Errored Framing Event (SEFE), and T3 Application ID status indication

T2/E2 Framer

- Generates T2/E2 Alarm Indication Signal (AIS) and Remote Alarm Indication (RAI) alarms
- Generates Alarm Indication Signal (AIS) for T1/E1 datastreams in both the transmit and receive directions
- Detects the following T2/E2 alarms and events: Loss Of Frame (LOF), Alarm Indication Signal (AIS), and Remote Alarm Indication (RAI)
- Detects T1 line loopback commands (C3 bit is the inverse of C1 and C2)
- Generates T1 line loopback commands

HDLC Controller

- Designed to handle multiple LAPD messages without Host intervention
- 256 byte receive and transmit buffers are large enough to handle the three T3 messages (Path ID, Idle Signal ID, and Test Signal ID) that are sent and received once a second which means the Host only needs to access the HDLC Controller once a second
- Handles all of the normal Layer 2 tasks such as zero stuffing/destuffing, CRC generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low water marks for the FIFO
- HDLC Controller can be used in either the T3 C-Bit Parity Mode or in the Sn Bits in the E3 Mode

FEAC Controller

- Designed to handle multiple FEAC Codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-byte FIFO
- Transmit FEAC can be configured to send either one codeword, or constant codewords, or two different codewords back-to-back to create T3 Line Loopback commands
- FEAC Controller can be used in either the T3 C-Bit Parity Mode or in the Sn Bits in the E3 Mode

BERT

- Can generate and detect the pseudorandom patterns of 2^7 – 1, 2^11 – 1, 2^15 – 1 and QRSS as well as repetitive patterns from 1 to 32 bits in length
- BERT is a global chip resource that can be used either in the T3/E3 data path or in any one of the T1 or E1 data paths
- Large error counter (24 bits) allows testing to proceed for long periods without Host intervention
- Errors can be inserted into the generated BERT patterns for diagnostic purposes

Diagnostics

- T3/E3 and T1/E1 diagnostic loopbacks (transmit to receive)
- T3/E3 and T1/E1 line loopbacks (receive to transmit)
- T3/E3 payload loopback
- T3/E3 errors counters for: BiPolar Violations (BPV), Code Violations (CV), Loss Of Frame (LOF), framing bit errors (F, M or FAS), EXcessive Zeros (EXZ), T3 Parity bits, T3 C-Bit Parity, and Far End Block Errors (FEBE)
- Error counters can be either updated automatically on one second boundaries as timed by the DS3112 or via software control or via an external hardware pulse
- Can insert the following T3/E3 errors: BiPolar Violations (BPV), EXcessive Zeros (EXZ), T3 Parity bits, T3 C-Bit Parity, framing bit errors (F, M or FAS)
- Inserted errors can be either controlled via software or via an external hardware pulse
- Generates T2/E2 Loss Of Frame (LOF)

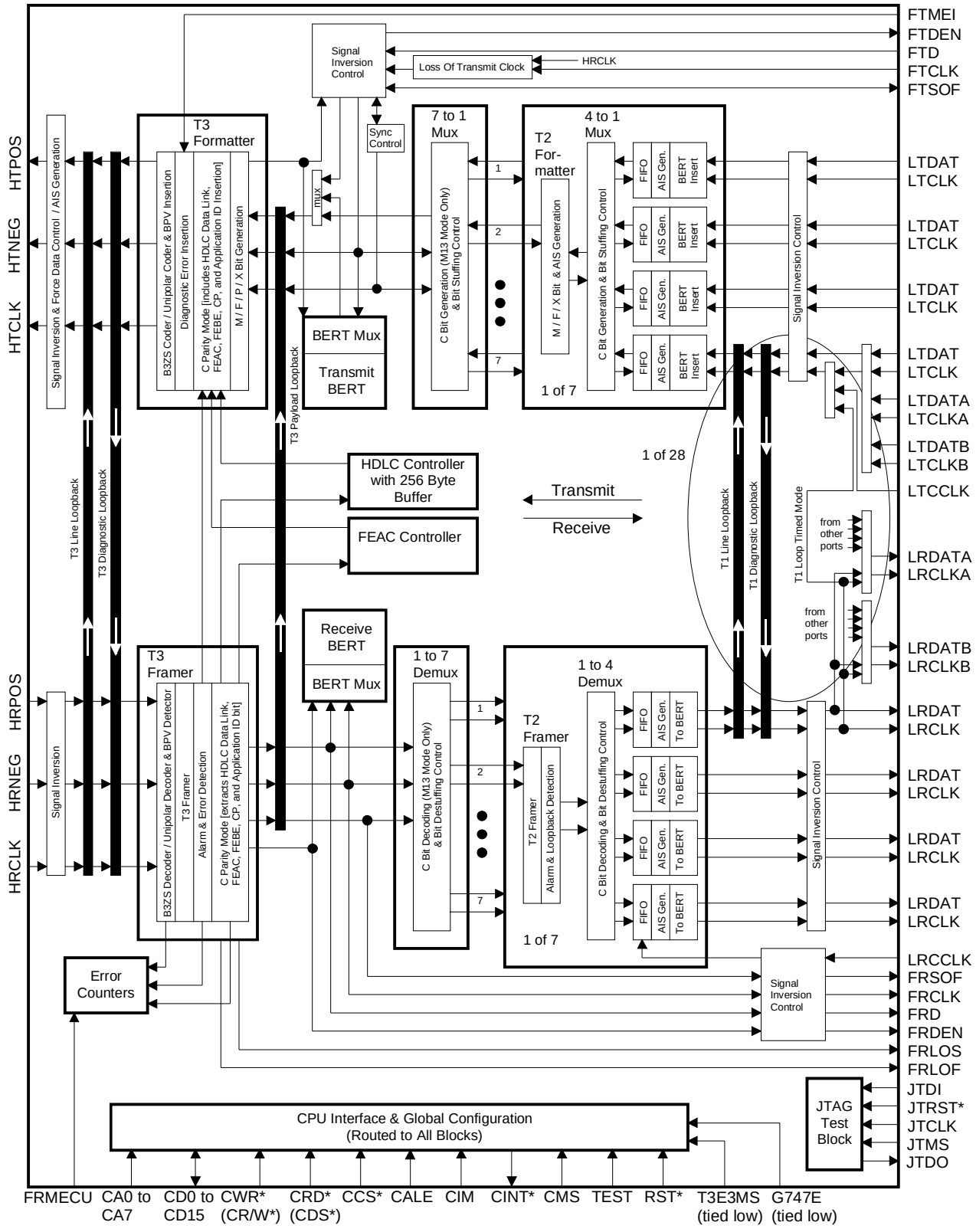
Control Port

- Non-Multiplexed or Multiplexed 16 Bit Control Port (with an optional 8 bit mode)
- Intel and Motorola Bus Compatible

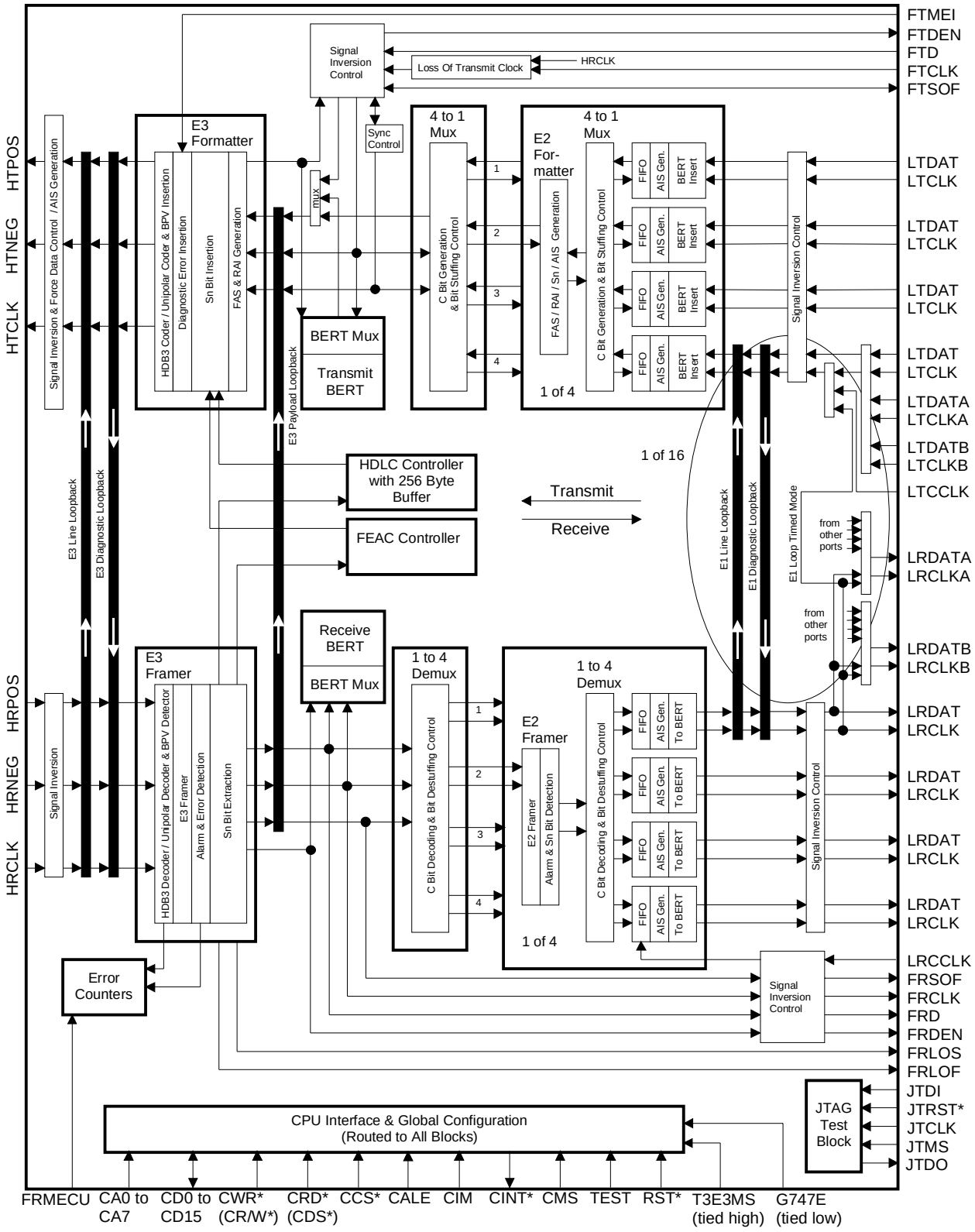
Packaging and Power

- 3.3V low power CMOS with 5V tolerant inputs and outputs
- 256 lead plastic BGA package (27 mm x 27 mm)
- IEEE 1149.1 JTAG test port

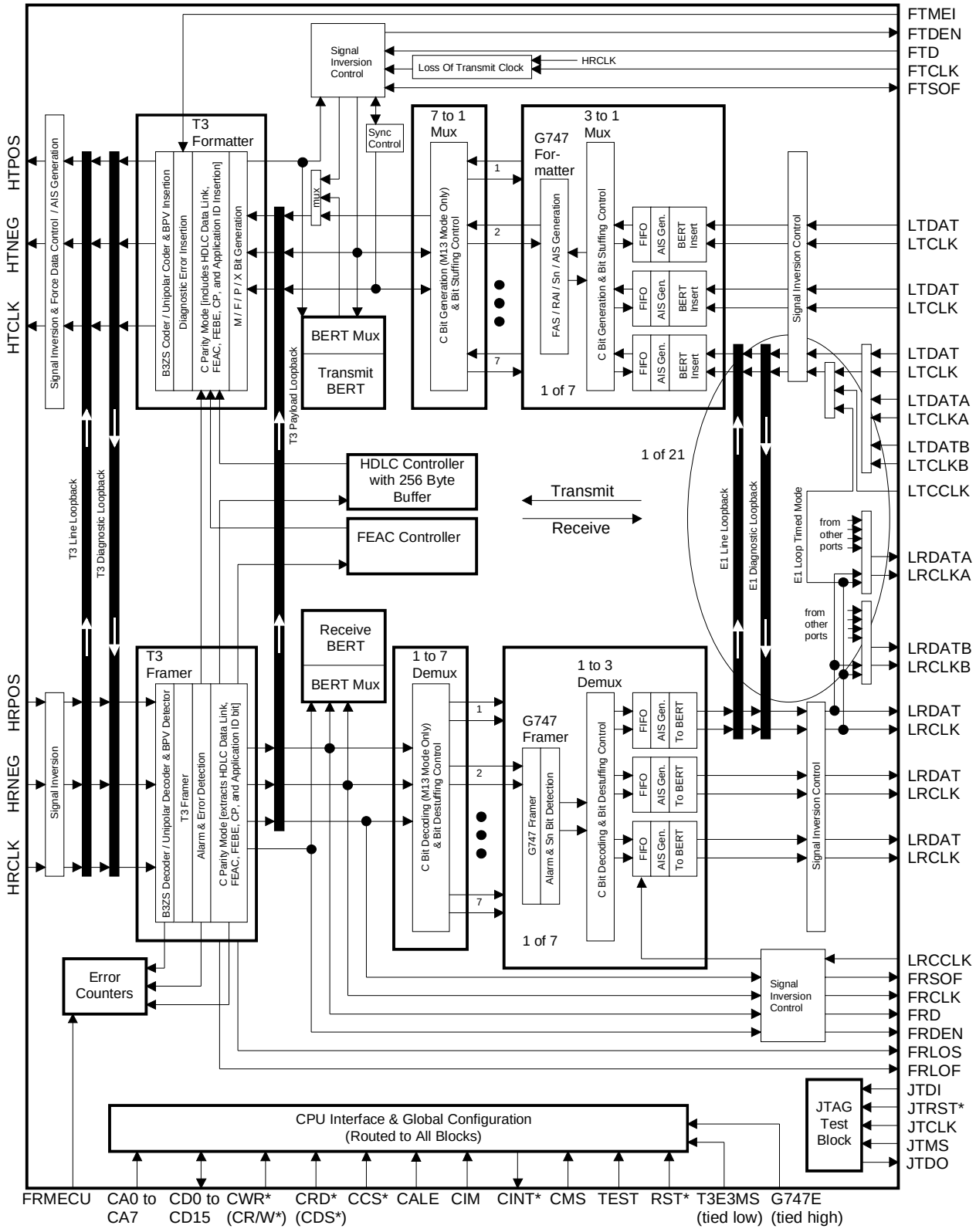
DS3112 Framer and Multiplexer Block Diagram (T3 Mode) Figure 1A



DS3112 Framer and Multiplexer Block Diagram (E3 Mode) Figure 1B



DS3112 Framer and Multiplexer Block Diagram (G747 Mode) Figure 1C



SECTION 2: SIGNAL DESCRIPTION

2.1 OVERVIEW / SIGNAL LEAD LIST

This section describes the input and output signals on the DS3112. Signal names follow a convention that is shown in Table 2.1A. Table 2.1B lists all of the signals, their signal type, description, and lead location. Symbols appended with an asterisks (*) are active low signals. The absence of an asterisks implies an active high signal.

SIGNAL NAMING CONVENTION Table 2.1A

First Letters	Signal Category	Section
C	CPU / Host Control Access Port	2.2
FR	T3 / E3 Receive Framer	2.3
FT	T3 / E3 Transmit Formatter	2.4
LR	Low Speed (T1 or E1) Receive Port	2.5
LT	Low Speed (T1 or E1) Transmit Port	2.6
HR	High Speed (T3 or E3) Receive Port	2.7
HT	High Speed (T3 or E3) Transmit Port	2.8
J	JTAG Test Port	2.9

SIGNAL DESCRIPTION / LEAD LIST (preliminary lead assignment) Table 2.1B

Lead	Symbol	Type	Signal Description
C7	CALE	I	CPU Bus Address Latch Enable.
H3	CA0	I	CPU Bus Address Bit 0. LSB.
H2	CA1	I	CPU Bus Address Bit 1.
H1	CA2	I	CPU Bus Address Bit 2.
J4	CA3	I	CPU Bus Address Bit 3.
J3	CA4	I	CPU Bus Address Bit 4.
J2	CA5	I	CPU Bus Address Bit 5.
J1	CA6	I	CPU Bus Address Bit 6.
K2	CA7	I	CPU Bus Address Bit 7. MSB.
C4	CCS*	I	CPU Bus Chip Select.
C2	CD0	I/O	CPU Bus Data Bit 0. LSB.
D2	CD1	I/O	CPU Bus Data Bit 1.
D3	CD2	I/O	CPU Bus Data Bit 2.
E4	CD3	I/O	CPU Bus Data Bit 3.
C1	CD4	I/O	CPU Bus Data Bit 4.
D1	CD5	I/O	CPU Bus Data Bit 5.
E3	CD6	I/O	CPU Bus Data Bit 6.
E2	CD7	I/O	CPU Bus Data Bit 7.
E1	CD8	I/O	CPU Bus Data Bit 8.
F3	CD9	I/O	CPU Bus Data Bit 9.
G4	CD10	I/O	CPU Bus Data Bit 10.
F2	CD11	I/O	CPU Bus Data Bit 11.

Lead	Symbol	Type	Signal Description
F1	CD12	I/O	CPU Bus Data Bit 12.
G3	CD13	I/O	CPU Bus Data Bit 13.
G2	CD14	I/O	CPU Bus Data Bit 14.
G1	CD15	I/O	CPU Bus Data Bit 15. MSB.
B3	CIM	I	CPU Bus Intel/Motorola Bus Select. 0 = INTEL, 1 = MOT.
A2	CINT*	O	CPU Bus Interrupt.
B2	CMS	I	CPU Bus Mode Select. 0 = 16 Bit, 1 = 8 Bit Mode.
D5	CRD*(CDS*)	I	CPU Bus Read Enable (CPU Bus Data Strobe).
A3	CWR*(CR/W*)	I	CPU Bus Write Enable (CPU Bus Read/Write Select).
A9	FRCLK	O	Receive Framer (T3 or E3) Clock Output.
B9	FRD	O	Receive Framer (T3 or E3) Data Output.
C9	FRDEN	O	Receive Framer (T3 or E3) Data Enable Output.
C8	FRLOF	O	Receive Framer (T3 or E3) Loss Of Frame Output.
B8	FRLOS	O	Receive Framer (T3 or E3) Loss Of Signal Output.
A7	FRMECU	I	Receive Framer (T3 or E3) Manual Error Counter Update.
A8	FRSOF	O	Receive Framer (T3 or E3) Start Of Frame Pulse.
A10	FTCLK	I	Transmit Framer (T3 or E3) Clock Input.
B10	FTD	I	Transmit Framer (T3 or E3) Data Input.
C10	FTDEN	O	Transmit Framer (T3 or E3) Data Enable Output.
C11	FTMEI	I	Transmit Framer (T3 or E3) Manual Error Insert Pulse.
A11	FTSOF	I/O	Transmit Framer (T3 or E3) Start Of Frame Pulse.
B6	G747E	I	G747 Mode Enable. 0 = Normal T3 Mode, 1 = G747 Mode.
A13	HRCLK	I	High Speed (T3 or E3) Port Receive Clock Input.
C12	HRNEG	I	High Speed (T3 or E3) Port Receive Negative Data Input.
B13	HRPOS	I	High Speed (T3 or E3) Port Receive Positive or NRZ Data Input.
B14	HTCLK	O	High Speed (T3 or E3) Port Transmit Clock Output.
A14	HTNEG	O	High Speed (T3 or E3) Port Transmit Negative Data Output.
C14	HTPOS	O	High Speed (T3 or E3) Port Transmit Positive or NRZ Data Output.
D7	JTCLK	I	JTAG IEEE 1149.1 Test Serial Clock.
B5	JTDI	I	JTAG IEEE 1149.1 Test Serial Data Input.
A4	JTDO	O	JTAG IEEE 1149.1 Test Serial Data Output.
A5	JTMS	I	JTAG IEEE 1149.1 Test Mode Select.
C6	JTRST*	I	JTAG IEEE 1149.1 Test Reset.
G20	LRCCLK	I	Low Speed (T1 or E1) Port Common Receive Clock Input.
N2	LRCLK1	O	Low Speed (T1 or E1) Receive Clock from Port 1.
R1	LRCLK2	O	Low Speed (T1 or E1) Receive Clock from Port 2.
R3	LRCLK3	O	Low Speed (T1 or E1) Receive Clock from Port 3.
U2	LRCLK4	O	Low Speed (T1 or E1) Receive Clock from Port 4.
V2	LRCLK5	O	Low Speed (T1 or E1) Receive Clock from Port 5.
Y2	LRCLK6	O	Low Speed (T1 or E1) Receive Clock from Port 6.

Lead	Symbol	Type	Signal Description
Y3	LRCLK7	O	Low Speed (T1 or E1) Receive Clock from Port 7.
Y5	LRCLK8	O	Low Speed (T1 or E1) Receive Clock from Port 8.
Y6	LRCLK9	O	Low Speed (T1 or E1) Receive Clock from Port 9.
V8	LRCLK10	O	Low Speed (T1 or E1) Receive Clock from Port 10.
V9	LRCLK11	O	Low Speed (T1 or E1) Receive Clock from Port 11.
V10	LRCLK12	O	Low Speed (T1 or E1) Receive Clock from Port 12.
V11	LRCLK13	O	Low Speed (T1 or E1) Receive Clock from Port 13.
Y13	LRCLK14	O	Low Speed (T1 or E1) Receive Clock from Port 14.
W14	LRCLK15	O	Low Speed (T1 or E1) Receive Clock from Port 15.
Y16	LRCLK16	O	Low Speed (T1 or E1) Receive Clock from Port 16.
Y17	LRCLK17	O	Low Speed (T1 or E1) Receive Clock from Port 17.
U16	LRCLK18	O	Low Speed (T1 or E1) Receive Clock from Port 18.
V18	LRCLK19	O	Low Speed (T1 or E1) Receive Clock from Port 19.
V19	LRCLK20	O	Low Speed (T1 or E1) Receive Clock from Port 20.
V20	LRCLK21	O	Low Speed (T1 or E1) Receive Clock from Port 21.
T20	LRCLK22	O	Low Speed (T1 or E1) Receive Clock from Port 22.
R20	LRCLK23	O	Low Speed (T1 or E1) Receive Clock from Port 23.
N18	LRCLK24	O	Low Speed (T1 or E1) Receive Clock from Port 24.
M18	LRCLK25	O	Low Speed (T1 or E1) Receive Clock from Port 25.
L18	LRCLK26	O	Low Speed (T1 or E1) Receive Clock from Port 26.
K18	LRCLK27	O	Low Speed (T1 or E1) Receive Clock from Port 27.
H20	LRCLK28	O	Low Speed (T1 or E1) Receive Clock from Port 28.
K1	LRCLKA	O	Low Speed (T1 or E1) Receive Clock from Drop Port A.
M1	LRCLKB	O	Low Speed (T1 or E1) Receive Clock from Drop Port B.
N1	LRDAT1	O	Low Speed (T1 or E1) Receive Data from Port 1.
P2	LRDAT2	O	Low Speed (T1 or E1) Receive Data from Port 2.
P4	LRDAT3	O	Low Speed (T1 or E1) Receive Data from Port 3.
T3	LRDAT4	O	Low Speed (T1 or E1) Receive Data from Port 4.
U3	LRDAT5	O	Low Speed (T1 or E1) Receive Data from Port 5.
W3	LRDAT6	O	Low Speed (T1 or E1) Receive Data from Port 6.
U5	LRDAT7	O	Low Speed (T1 or E1) Receive Data from Port 7.
W5	LRDAT8	O	Low Speed (T1 or E1) Receive Data from Port 8.
W6	LRDAT9	O	Low Speed (T1 or E1) Receive Data from Port 9.
Y7	LRDAT10	O	Low Speed (T1 or E1) Receive Data from Port 10.
U9	LRDAT11	O	Low Speed (T1 or E1) Receive Data from Port 11.
W10	LRDAT12	O	Low Speed (T1 or E1) Receive Data from Port 12.
W11	LRDAT13	O	Low Speed (T1 or E1) Receive Data from Port 13.
V12	LRDAT14	O	Low Speed (T1 or E1) Receive Data from Port 14.
Y14	LRDAT15	O	Low Speed (T1 or E1) Receive Data from Port 15.
W15	LRDAT16	O	Low Speed (T1 or E1) Receive Data from Port 16.
W16	LRDAT17	O	Low Speed (T1 or E1) Receive Data from Port 17.
Y18	LRDAT18	O	Low Speed (T1 or E1) Receive Data from Port 18.
Y19	LRDAT19	O	Low Speed (T1 or E1) Receive Data from Port 19.
W20	LRDAT20	O	Low Speed (T1 or E1) Receive Data from Port 20.

Lead	Symbol	Type	Signal Description
T17	LRDAT21	O	Low Speed (T1 or E1) Receive Data from Port 21.
T19	LRDAT22	O	Low Speed (T1 or E1) Receive Data from Port 22.
R19	LRDAT23	O	Low Speed (T1 or E1) Receive Data from Port 23.
P20	LRDAT24	O	Low Speed (T1 or E1) Receive Data from Port 24.
M17	LRDAT25	O	Low Speed (T1 or E1) Receive Data from Port 25.
L19	LRDAT26	O	Low Speed (T1 or E1) Receive Data from Port 26.
K19	LRDAT27	O	Low Speed (T1 or E1) Receive Data from Port 27.
J18	LRDAT28	O	Low Speed (T1 or E1) Receive Data from Port 28.
K3	LRDATA	O	Low Speed (T1 or E1) Receive Data from Drop Port A.
L3	LRDATB	O	Low Speed (T1 or E1) Receive Data from Drop Port B.
G19	LTCCLK	I	Low Speed (T1 or E1) Port Common Transmit Clock Input.
P1	LTCLK1	I	Low Speed (T1 or E1) Transmit Clock for Port 1.
R2	LTCLK2	I	Low Speed (T1 or E1) Transmit Clock for Port 2.
U1	LTCLK3	I	Low Speed (T1 or E1) Transmit Clock for Port 3.
T4	LTCLK4	I	Low Speed (T1 or E1) Transmit Clock for Port 4.
V3	LTCLK5	I	Low Speed (T1 or E1) Transmit Clock for Port 5.
V4	LTCLK6	I	Low Speed (T1 or E1) Transmit Clock for Port 6.
V5	LTCLK7	I	Low Speed (T1 or E1) Transmit Clock for Port 7.
U7	LTCLK8	I	Low Speed (T1 or E1) Transmit Clock for Port 8.
W7	LTCLK9	I	Low Speed (T1 or E1) Transmit Clock for Port 9.
Y8	LTCLK10	I	Low Speed (T1 or E1) Transmit Clock for Port 10.
Y9	LTCLK11	I	Low Speed (T1 or E1) Transmit Clock for Port 11.
Y11	LTCLK12	I	Low Speed (T1 or E1) Transmit Clock for Port 12.
W12	LTCLK13	I	Low Speed (T1 or E1) Transmit Clock for Port 13.
V13	LTCLK14	I	Low Speed (T1 or E1) Transmit Clock for Port 14.
V14	LTCLK15	I	Low Speed (T1 or E1) Transmit Clock for Port 15.
V15	LTCLK16	I	Low Speed (T1 or E1) Transmit Clock for Port 16.
W17	LTCLK17	I	Low Speed (T1 or E1) Transmit Clock for Port 17.
W18	LTCLK18	I	Low Speed (T1 or E1) Transmit Clock for Port 18.
Y20	LTCLK19	I	Low Speed (T1 or E1) Transmit Clock for Port 19.
U18	LTCLK20	I	Low Speed (T1 or E1) Transmit Clock for Port 20.
T18	LTCLK21	I	Low Speed (T1 or E1) Transmit Clock for Port 21.
P17	LTCLK22	I	Low Speed (T1 or E1) Transmit Clock for Port 22.
P19	LTCLK23	I	Low Speed (T1 or E1) Transmit Clock for Port 23.
N20	LTCLK24	I	Low Speed (T1 or E1) Transmit Clock for Port 24.
M20	LTCLK25	I	Low Speed (T1 or E1) Transmit Clock for Port 25.
K20	LTCLK26	I	Low Speed (T1 or E1) Transmit Clock for Port 26.
J19	LTCLK27	I	Low Speed (T1 or E1) Transmit Clock for Port 27.
H18	LTCLK28	I	Low Speed (T1 or E1) Transmit Clock for Port 28.
L2	LTCLKA	I	Low Speed (T1 or E1) Transmit Clock for Insert Port A.
M3	LTCLKB	I	Low Speed (T1 or E1) Transmit Clock for Insert Port B.
N3	LTDAT1	I	Low Speed (T1 or E1) Transmit Data for Port 1.
P3	LTDAT2	I	Low Speed (T1 or E1) Transmit Data for Port 2.

Lead	Symbol	Type	Signal Description
T2	LTDAT3	I	Low Speed (T1 or E1) Transmit Data for Port 3.
V1	LTDAT4	I	Low Speed (T1 or E1) Transmit Data for Port 4.
W1	LTDAT5	I	Low Speed (T1 or E1) Transmit Data for Port 5.
W4	LTDAT6	I	Low Speed (T1 or E1) Transmit Data for Port 6.
Y4	LTDAT7	I	Low Speed (T1 or E1) Transmit Data for Port 7.
V6	LTDAT8	I	Low Speed (T1 or E1) Transmit Data for Port 8.
V7	LTDAT9	I	Low Speed (T1 or E1) Transmit Data for Port 9.
W8	LTDAT10	I	Low Speed (T1 or E1) Transmit Data for Port 10.
W9	LTDAT11	I	Low Speed (T1 or E1) Transmit Data for Port 11.
Y10	LTDAT12	I	Low Speed (T1 or E1) Transmit Data for Port 12.
Y12	LTDAT13	I	Low Speed (T1 or E1) Transmit Data for Port 13.
W13	LTDAT14	I	Low Speed (T1 or E1) Transmit Data for Port 14.
Y15	LTDAT15	I	Low Speed (T1 or E1) Transmit Data for Port 15.
U14	LTDAT16	I	Low Speed (T1 or E1) Transmit Data for Port 16.
V16	LTDAT17	I	Low Speed (T1 or E1) Transmit Data for Port 17.
V17	LTDAT18	I	Low Speed (T1 or E1) Transmit Data for Port 18.
W19	LTDAT19	I	Low Speed (T1 or E1) Transmit Data for Port 19.
U19	LTDAT20	I	Low Speed (T1 or E1) Transmit Data for Port 20.
U20	LTDAT21	I	Low Speed (T1 or E1) Transmit Data for Port 21.
R18	LTDAT22	I	Low Speed (T1 or E1) Transmit Data for Port 22.
P18	LTDAT23	I	Low Speed (T1 or E1) Transmit Data for Port 23.
N19	LTDAT24	I	Low Speed (T1 or E1) Transmit Data for Port 24.
M19	LTDAT25	I	Low Speed (T1 or E1) Transmit Data for Port 25.
L20	LTDAT26	I	Low Speed (T1 or E1) Transmit Data for Port 26.
J20	LTDAT27	I	Low Speed (T1 or E1) Transmit Data for Port 27.
H19	LTDAT28	I	Low Speed (T1 or E1) Transmit Data for Port 28.
L1	LTDATA	I	Low Speed (T1 or E1) Transmit Data for Insert Port A.
M2	LTDATB	I	Low Speed (T1 or E1) Transmit Data for Insert Port B.
A12	NC	-	No Connect. Do not connect any signal to this lead.
A15	NC	-	No Connect. Do not connect any signal to this lead.
A16	NC	-	No Connect. Do not connect any signal to this lead.
A17	NC	-	No Connect. Do not connect any signal to this lead.
A18	NC	-	No Connect. Do not connect any signal to this lead.
A19	NC	-	No Connect. Do not connect any signal to this lead.
A20	NC	-	No Connect. Do not connect any signal to this lead.
A6	NC	-	No Connect. Do not connect any signal to this lead.
B1	NC	-	No Connect. Do not connect any signal to this lead.
B11	NC	-	No Connect. Do not connect any signal to this lead.
B12	NC	-	No Connect. Do not connect any signal to this lead.
B15	NC	-	No Connect. Do not connect any signal to this lead.
B16	NC	-	No Connect. Do not connect any signal to this lead.
B17	NC	-	No Connect. Do not connect any signal to this lead.
B18	NC	-	No Connect. Do not connect any signal to this lead.
B19	NC	-	No Connect. Do not connect any signal to this lead.

Lead	Symbol	Type	Signal Description
B20	NC	-	No Connect. Do not connect any signal to this lead.
B7	NC	-	No Connect. Do not connect any signal to this lead.
C13	NC	-	No Connect. Do not connect any signal to this lead.
C15	NC	-	No Connect. Do not connect any signal to this lead.
C16	NC	-	No Connect. Do not connect any signal to this lead.
C17	NC	-	No Connect. Do not connect any signal to this lead.
C18	NC	-	No Connect. Do not connect any signal to this lead.
C19	NC	-	No Connect. Do not connect any signal to this lead.
C20	NC	-	No Connect. Do not connect any signal to this lead.
D12	NC	-	No Connect. Do not connect any signal to this lead.
D14	NC	-	No Connect. Do not connect any signal to this lead.
D16	NC	-	No Connect. Do not connect any signal to this lead.
D18	NC	-	No Connect. Do not connect any signal to this lead.
D19	NC	-	No Connect. Do not connect any signal to this lead.
D20	NC	-	No Connect. Do not connect any signal to this lead.
E17	NC	-	No Connect. Do not connect any signal to this lead.
E18	NC	-	No Connect. Do not connect any signal to this lead.
E19	NC	-	No Connect. Do not connect any signal to this lead.
E20	NC	-	No Connect. Do not connect any signal to this lead.
F18	NC	-	No Connect. Do not connect any signal to this lead.
F19	NC	-	No Connect. Do not connect any signal to this lead.
F20	NC	-	No Connect. Do not connect any signal to this lead.
G17	NC	-	No Connect. Do not connect any signal to this lead.
G18	NC	-	No Connect. Do not connect any signal to this lead.
T1	NC	-	No Connect. Do not connect any signal to this lead.
W2	NC	-	No Connect. Do not connect any signal to this lead.
Y1	NC	-	No Connect. Do not connect any signal to this lead.
C5	RST*	I	Reset.
B4	T3E3MS	I	T3 / E3 Mode Select. 0 = T3, 1 = E3.
C3	TEST*	I	Factory Test Input.
D10	VDD	-	Positive Supply. 3.3V (+/- 5%).
D11	VDD	-	Positive Supply. 3.3V (+/- 5%).
D15	VDD	-	Positive Supply. 3.3V (+/- 5%).
D6	VDD	-	Positive Supply. 3.3V (+/- 5%).
F17	VDD	-	Positive Supply. 3.3V (+/- 5%).
F4	VDD	-	Positive Supply. 3.3V (+/- 5%).
K17	VDD	-	Positive Supply. 3.3V (+/- 5%).
K4	VDD	-	Positive Supply. 3.3V (+/- 5%).
L17	VDD	-	Positive Supply. 3.3V (+/- 5%).
L4	VDD	-	Positive Supply. 3.3V (+/- 5%).
R17	VDD	-	Positive Supply. 3.3V (+/- 5%).
R4	VDD	-	Positive Supply. 3.3V (+/- 5%).
U10	VDD	-	Positive Supply. 3.3V (+/- 5%).
U11	VDD	-	Positive Supply. 3.3V (+/- 5%).

Lead	Symbol	Type	Signal Description
U15	VDD	-	Positive Supply. 3.3V (+/- 5%).
U6	VDD	-	Positive Supply. 3.3V (+/- 5%).
A1	VSS	-	Ground Reference.
D13	VSS	-	Ground Reference.
D17	VSS	-	Ground Reference.
D4	VSS	-	Ground Reference.
D8	VSS	-	Ground Reference.
D9	VSS	-	Ground Reference.
H17	VSS	-	Ground Reference.
H4	VSS	-	Ground Reference.
J17	VSS	-	Ground Reference.
M4	VSS	-	Ground Reference.
N17	VSS	-	Ground Reference.
N4	VSS	-	Ground Reference.
U12	VSS	-	Ground Reference.
U13	VSS	-	Ground Reference.
U17	VSS	-	Ground Reference.
U4	VSS	-	Ground Reference.
U8	VSS	-	Ground Reference.

2.2 CPU BUS SIGNAL DESCRIPTION

Signal Name: **CMS**
Signal Description: **CPU Bus Mode Select**
Signal Type: **Input**
This signal should be tied low when the device is to be operated as a 16-bit bus. This signal should be tied high when the device is to be operated as an 8-bit bus.

0 = CPU Bus is in the 16-Bit Mode
1 = CPU Bus is in the 8-Bit Mode

Signal Name: **CIM**
Signal Description: **CPU Bus Intel/Motorola Bus Select**
Signal Type: **Input**
The signal determines whether the CPU Bus will operate in the Intel Mode (CIM = 0) or the Motorola Mode (CIM = 1). The signal names in parenthesis are operational when the device is in the Motorola Mode.

0 = CPU Bus is in the Intel Mode
1 = CPU Bus is in the Motorola Mode

Signal Name: **CD0 to CD15**
Signal Description: **CPU Bus Data Bus**
Signal Type: **Input / Output (tri-state capable)**
The external Host will configure the device and obtain real time status information about the device via these signals. When reading data from the CPU Bus, these signals will be outputs. When writing data to the CPU Bus, these signals will become inputs. When the CPU bus is operated in the 8-bit mode (CMS = 1), CD8 to CD15 are inactive and should be tied low.

Signal Name: **CA0 to CA7**
Signal Description: **CPU Bus Address Bus**
Signal Type: **Input**
These input signals determine which internal device configuration register that the external Host wishes to access. When the CPU bus is operated in the 16-bit mode (CMS = 0), CA0 is inactive and should be tied low. When the CPU bus is operated in the 8-bit mode (CMS = 1), CA0 is the least significant address bit.

Signal Name: **CWR* (CR/W*)**
Signal Description: **CPU Bus Write Enable (CPU Bus Read/Write Select)**
Signal Type: **Input**
In Intel Mode (CIM = 0) this signal will determine when data is to be written to the device. In Motorola Mode (CIM = 1), this signal will be used to determine whether a read or write is to occur.

Signal Name: **CRD* (CDS*)**
Signal Description: **CPU Bus Read Enable (CPU Bus Data Strobe)**
Signal Type: **Input**
In Intel Mode (CIM = 0) this signal will determine when data is to be read from the device. In Motorola Mode (CIM = 1), a rising edge will be used to write data into the device.

Signal Name: **CINT***
Signal Description: **CPU Bus Interrupt**
Signal Type: **Output (open drain)**
This signal is an open drain output which will be forced low if one or more unmasked interrupt sources within the device is active. The signal will remain low until either the interrupt is serviced or masked.

Signal Name: **CCS***
Signal Description: **CPU Bus Chip Select**
Signal Type: **Input**
This active low signal must be asserted for the device to accept a read or write command from an external Host.

Signal Name: **CALE**
Signal Description: **CPU Bus Address Latch Enable**
Signal Type: **Input**
This input signal controls a latch that exists on the CA0 to CA7 inputs. When CALE is high, the latch is transparent. The falling edge of CALE causes the latch to sample and hold the CA0 to CA7 inputs. In non-multiplexed bus applications, CALE should be tied high. In multiplexed bus applications, CA[7:0] should be tied to CD[7:0] and the falling edge of CALE will latch the address.

2.3 T3 / E3 RECEIVE FRAMER SIGNAL DESCRIPTION

Signal Name: **FRSOF**
Signal Description: **T3/E3 Receive Framer Start Of Frame Sync Signal**
Signal Type: **Output**
This signal pulses for one FRCLK period to indicate the T3 or E3 frame boundary. See Figure 2.3A for an example. This signal can be configured via the FRSOFI control bit in Master Control Register 3 (see Section 4.2) to be either active high (normal mode) or active low (inverted mode).

Signal Name: **FRCLK**
Signal Description: **T3/E3 Receive Framer Clock**
Signal Type: **Output**
This signal outputs the clock that is used to pass data through the receive T3/E3 framer. It can be sourced from either the HRCLK or FTCLK inputs (see Figures 1A and 1B for details). This signal is used to clock the receive data out of the device at the FRD output. Data can be either updated on a rising edge (normal mode) or a falling edge (inverted mode). This option is controlled via the FRCLKI control bit in Master Control Register 3 (see Section 4.2).

Signal Name: **FRD**
Signal Description: **T3/E3 Receive Framer Serial Data**
Signal Type: **Output**
This signal outputs data from the receive T3/E3 framer. This signal is updated either on the rising edge of FRCLK (normal mode) or the falling edge of FRCLK (inverted mode). This option is controlled via the FRCLKI control bit in Master Control Register 3 (see Section 4.2). Also, this signal can be internally inverted if enabled via the FRDI control bit in Master Control Register 3 (see Section 4.2).

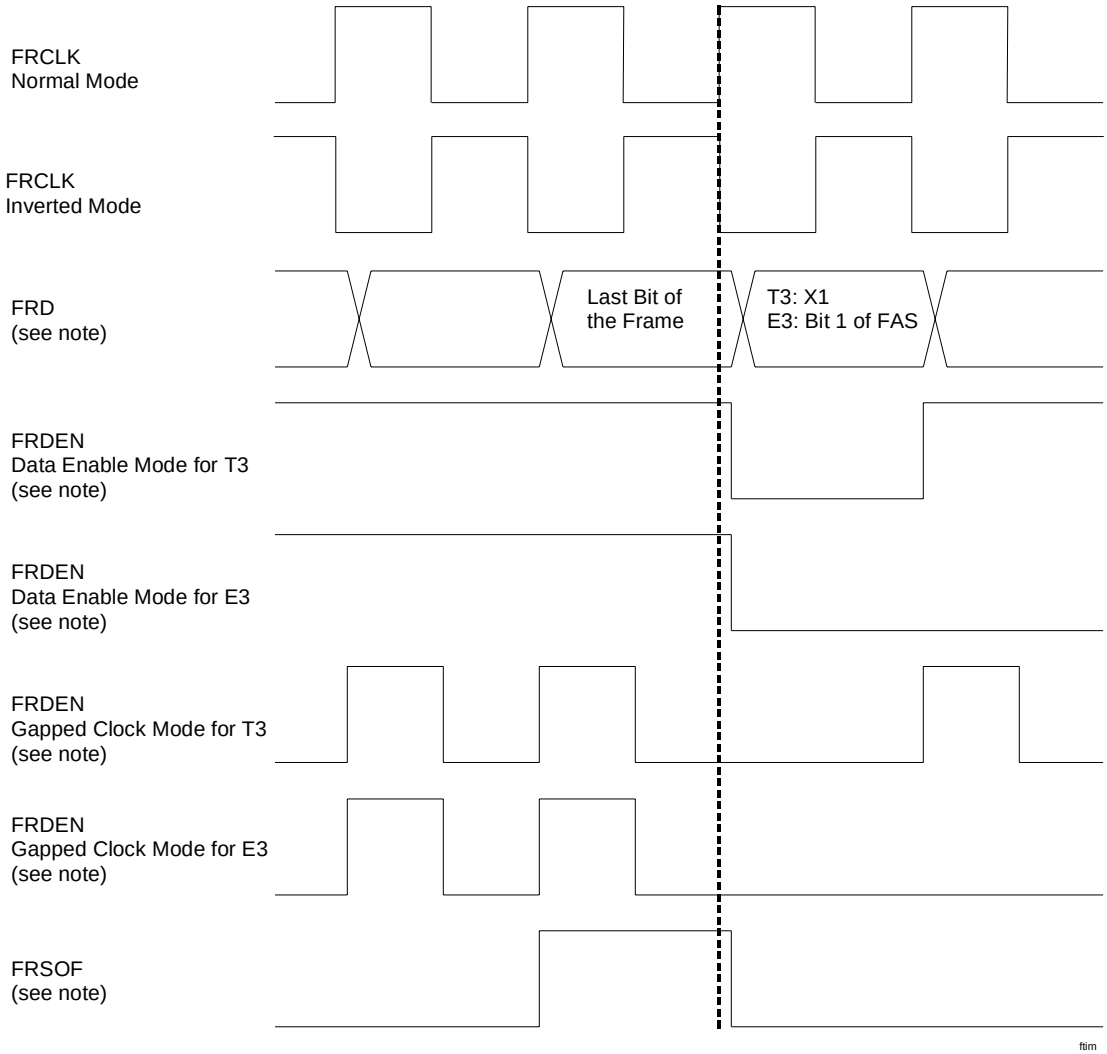
Signal Name: **FRDEN**
Signal Description: **T3/E3 Receive Framer Serial Data Enable or Gapped Clock Output**
Signal Type: **Output**
Via the DENMS control bit in Master Control Register 1, this signal can be configured to either output a data enable or a gapped clock. In the data enable mode, this signal will go active when payload data is available at the FRD output and it will go inactive when overhead data is being output at the FRD output. In the gapped clock mode, this signal will transition for each bit of payload data and will be suppressed for each bit of overhead data. In the T3 Mode, overhead data is defined as the M Bits, F Bits, C Bits, X Bits, and P Bits. In the E3 Mode, overhead data is defined as the FAS word, RAI Bit and Sn Bit (i.e. bits 1 to 12). See Figure 2.3A for an example. This signal can be internally inverted if enabled via the FRDENI control bit in Master Control Register 3 (see Section 4.2).

Signal Name: **FRMECU**
Signal Description: **T3/E3 Receive Framer Manual Error Counter Update Strobe**
Signal Type: **Input**
Via the AECU control bit in Master Control Register 1 (see Section 4.2), the DS3112 can be configured to use this asynchronous input to initiate an updating of the internal error counters. A 0 to 1 transition on this input causes the device to begin loading the internal error counters with the latest error counts. This signal must be returned low before a subsequent updating of the error counters can occur. The Host must wait at least 100 ns before reading the error counters to allow the device time to update the error counters. This signal is logically OR'ed with the MECU control bit in Master Control Register 1. If this signal is not used, then it should be tied low.

Signal Name: **FRLOS**
Signal Description: **T3/E3 Receive Framer Loss Of Signal**
Signal Type: **Output**
This signal will be forced high when the receive T3/E3 framer is in a Loss Of Signal (LOS) state. It will remain high as long as the LOS state persists and will return low when the framer exits the LOS state. See Section 5.3 for details on the set and clear criteria for this signal. LOS status is also available via a software bit in the T3/E3 Status Register (see Section 5.3).

Signal Name: **FRLOF**
Signal Description: **T3/E3 Receive Framer Loss Of Frame**
Signal Type: **Output**
This signal will be forced high when the receive T3/E3 framer is in a Loss Of Frame (LOF) state. It will remain high as long as the LOF state persists and will return low when the framer synchronizes. See Section 5.3 for details on the set and clear criteria for this signal. LOF status is also available via a software bit in the T3/E3 Status Register (see Section 5.3).

T3/E3 Receive Framer Timing Figure 2.3A



Note: FRD, FRDEN, and FRSOF can be inverted via Master Control Register 3.

2.4 T3 / E3 TRANSMIT FORMATTER SIGNAL DESCRIPTION

Signal Name: **FTSOF**
Signal Description: **T3/E3 Transmit Formatter Start Of Frame Sync Signal**
Signal Type: **Output / Input**
This signal can be configured via the FTSOFC control bit in Master Control Register 1 to be either an output or an input. When this signal is an output, it pulses for one FTCLK period to indicate a T3 or E3 frame boundary. See Figure 2.4A for an example. When this signal is an input, it is sampled to set the transmit T3 or E3 frame boundary. See Figure 2.4A for an example. This signal can be configured via the FTSOFI control bit in Master Control Register 3 (see Section 4.2) to be either active high (normal mode) or active low (inverted mode).

Signal Name: **FTCLK**
Signal Description: **T3/E3 Transmit Formatter Clock**
Signal Type: **Input**
An accurate T3 (44.736 MHz +/- 20 ppm) or E3 (34.368 MHz +/- 20 ppm) clock should be applied at this signal. This signal is used to clock data into the transmit T3/E3 formatter. Transmit data can be clocked into the device either on a rising edge (normal mode) or a falling edge (inverted mode). This option is controlled via the FTCLKI control bit in Master Control Register 3 (see Section 4.2).

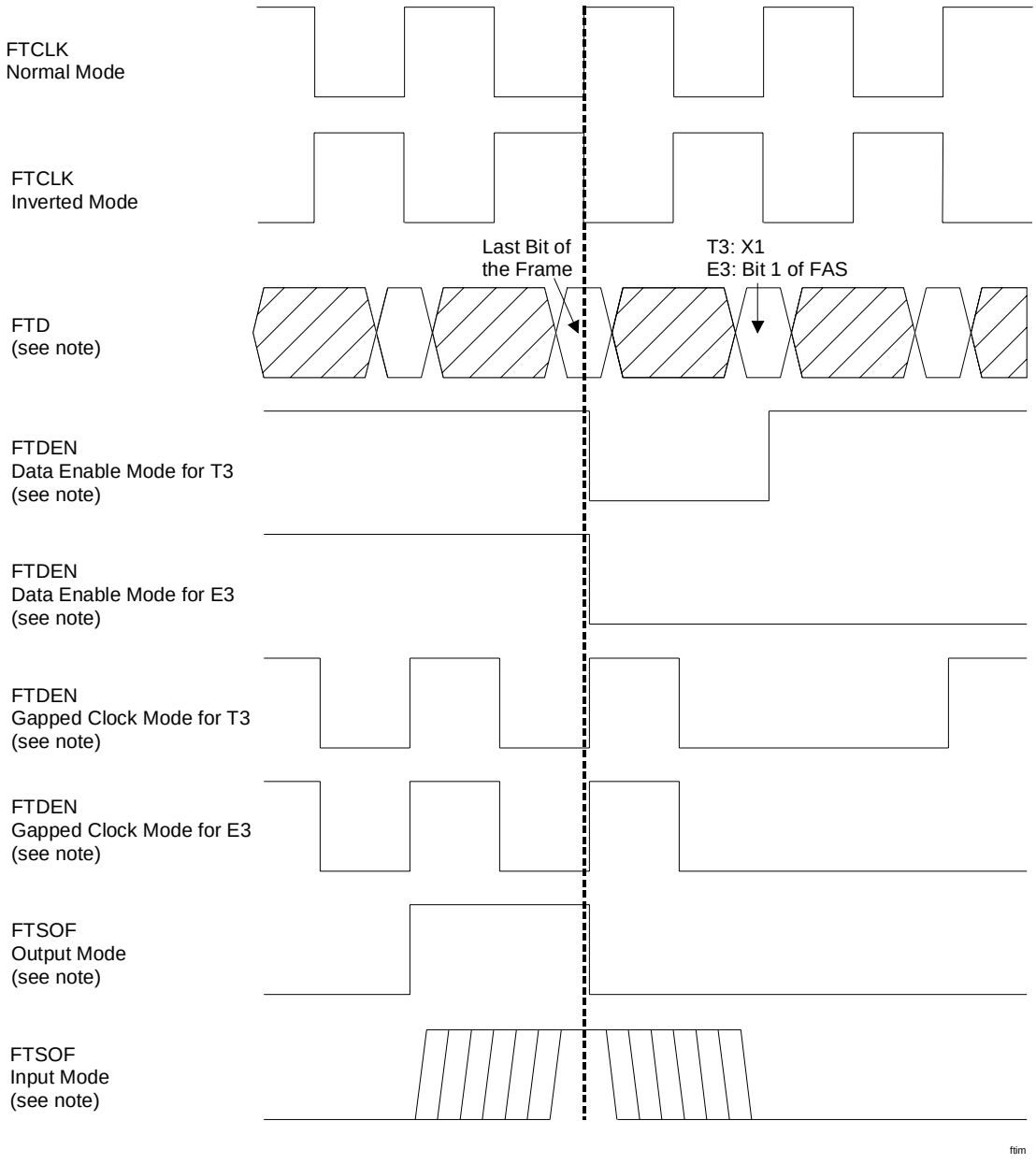
Signal Name: **FTD**
Signal Description: **T3/E3 Transmit Formatter Serial Data**
Signal Type: **Input**
This signal inputs data into the transmit T3/E3 formatter. This signal can be sampled either on the rising edge of FTCLK (normal mode) or the falling edge of FTCLK (inverted mode). This option is controlled via the FTCLKI control bit in Master Control Register 3 (see Section 4.2). Also, the data input to this signal can be internally inverted if enabled via the FTDI control bit in Master Control Register 3 (see Section 4.2). When T3 C-Bit Parity Mode is disabled, C Bits are sampled at this input. This signal is ignored when the M13/E13 multiplexer is enabled (see the UNCHEN control bit in Master Control Register 1). If not used, this signal should be tied low.

Signal Name: **FTDEN**
Signal Description: **T3/E3 Transmit Formatter Serial Data Enable or Gapped Clock Output**
Signal Type: **Output**
Via the DENMS control bit in Master Control Register 1, this signal can be configured to either output a data enable or a gapped clock. In the data enable mode, this signal will go active when payload data should be made available at the FTD input. In the gapped clock mode, this signal will act as a demand clock for the FTD input and it will transition for each bit of payload data needed at the FTD input and it will be suppressed when the transmit formatter inserts overhead data and hence no data is needed at the FTD input. In the T3 Mode, overhead data is defined as the M Bits, F Bits, C Bits, X Bits, and P Bits. In the E3 Mode, overhead data is defined as the FAS word, RAI Bit and Sn Bit (i.e. bits 1 to 12). See Figure 2.4A for an example. This signal can be internally inverted if enabled via the FTDENI control bit in Master Control Register 3 (see Section 4.2). This signal operates in the same manner even when the device is configured in the Transmit Pass Through mode (see the TPT control bit in the T3/E3 Control Register).

Signal Name: **FTMEI**
Signal Description: **T3/E3 Transmit Formatter Manual Error Insert Strobe**
Signal Type: **Input**

Via the EIC control bit in the T3/E3 Error insert Control Register (see Section 5.2), the DS3112 can be configured to use this asynchronous input to cause errors to be inserted into the transmitted data stream. A 0 to 1 transition on this input causes the device to begin the process of causing errors to be inserted. This signal must be returned low before any subsequent errors can be generated. If this signal is not used, then it should be tied low.

T3/E3 Transmit Formatter Timing Figure 2.4A



Note: FTD, FTDEN, and FTSOF can be inverted via Master Control Register 3.

2.5 LOW SPEED (T1 OR E1) RECEIVE PORT SIGNAL DESCRIPTION

Signal Name: **LRDAT1 to LRDAT28**
Signal Description: **Low Speed (T1 or E1) Receive Serial Data Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial data for the 28 T1 data streams or the 16/21 E1 data streams. Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of the associated LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (see Section 4.2). Also, the data can be internally inverted before being output if enabled via the LRDATI control bit in Master Control Register 2 (see Section 4.2). When the device is in the E3 Mode, LRDAT17 to LRDAT28 are meaningless and should be ignored. When the device is in the G747 Mode, LRDAT4, LRDAT8, LRDAT12, LRDAT16, LRDAT20, LRDAT24, and LRDAT28 are meaningless and should be ignored. When the M13 / E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRCLK1 to LRCLK28**
Signal Description: **Low Speed (T1 or E1) Receive Serial Clock Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial clocks for the 28 T1 data streams or the 16/21 E1 data streams. The T1 or E1 serial data streams at the associated LRDAT signals can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (see Section 4.2). When the device is in the E3 Mode, LRCLK17 to LRCLK28 are meaningless and should be ignored. When the device is in the G747 Mode, LRCLK4, LRCLK8, LRCLK12, LRCLK16, LRCLK20, LRCLK24, and LRCLK28 are meaningless and should be ignored. When the M13 / E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRDATA / LRDATB**
Signal Description: **Low Speed (T1 or E1) Receive Drop Port Serial Data Outputs**
Signal Type: **Output**
These two output signals present the demultiplexed serial data from one of the 28 T1 data streams or from one of the 16/21 E1 data streams (see Section 7.4). Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of the associated LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (see Section 4.2). Also, the data can be internally inverted before being output if enabled via the LRDATI control bit in Master Control Register 2 (see Section 4.2). When the M13 / E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRCLKA / LRCLKB**
Signal Description: **Low Speed (T1 or E1) Receive Drop Port Serial Clock Outputs**
Signal Type: **Output**
These output signals present the demultiplexed serial clocks from one of the 28 T1 data streams or from one of the 16/21 E1 data streams (see Section 7.4). The T1 or E1 serial data streams at the associated LRDAT signals can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of LRCLK. This option is controlled via the LRCLKI control bit in Master Control Register 2 (see Section 4.2). When the M13 / E13 multiplexer is disabled, then these outputs are meaningless and should be ignored.

Signal Name: **LRCCLK**
Signal Description: **Low Speed (T1 or E1) Receive Common Clock Input**
Signal Type: **Input**
If enabled via the LRCCEN control bit in Master Control Register 1 (see Section 4.2), all 28 LRCLK or 16/21 LRCLK can be slaved to this common clock input. In T3 mode, LRCCLK would be a 1.544 MHz clock and in E3 mode, LRCCLK would be 2.048 MHz. Use of this configuration is only possible in applications where it can be guaranteed that all of the multiplexed T1 or E1 signals at the far end are based on a common clock. If this signal is not used, then it should be tied low. This signal can be internally inverted. This option is controlled via the LRCLKI control bit in Master Control Register 2 (see Section 4.2).

2.6 LOW SPEED (T1 OR E1) TRANSMIT PORT SIGNAL DESCRIPTION

Signal Name: **LTDAT1 to LTDAT28**
Signal Description: **Low Speed (T1 or E1) Transmit Serial Data Inputs**
Signal Type: **Input**
These input signals sample the serial data from the 28 T1 data streams or the 16/21 E1 data streams that will be multiplexed into a single T3 or E3 data stream. Data can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of the associated LTCLK. This option is controlled via the LTCLKI control bit in Master Control Register 2 (see Section 4.2). Also, the data can be internally inverted before being multiplexed if enabled via the LTDATI control bit in Master Control Register 2 (see Section 4.2). When the device is in the E3 Mode, LTDAT17 to LTDAT28 are ignored and should be tied low. When the device is in the G747 Mode, LTDAT4, LTDAT8, LTDAT12, LTDAT16, LTDAT20, LTDAT24, and LTDAT28 are ignored and should be tied low. When the M13 / E13 multiplexer is disabled, then these inputs are ignored and should be tied low.

Signal Name: **LTCLK1 to LTCLK28**
Signal Description: **Low Speed (T1 or E1) Transmit Serial Clock Inputs**
Signal Type: **Input**
These input signals clock data in from the 28 T1 data streams or from the 16/21 E1 data streams. The T1 or E1 serial data streams at the associated LTDAT signals can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of LTCLK. This option is controlled via the LTCLKI control bit in Master Control Register 2 (see Section 4.2). When the device is in the E3 Mode, LTCLK17 to LTCLK28 are meaningless and should be tied low. When the device is in the G747 Mode, LTCLK4, LTCLK8, LTCLK12, LTCLK16, LTCLK20, LTCLK24, and LTCLK28 are meaningless and should be tied low. When the M13 / E13 multiplexer is disabled, then these inputs are ignored and should be tied low.

Signal Name: **LTDATA / LTDATB**
Signal Description: **Low Speed (T1 or E1) Transmit Insert Port Serial Data Inputs**
Signal Type: **Input**
These two input signals allow data to be inserted in place of any of the 28 T1 data streams or into any of the 16/21 E1 data streams (see Section 7.4). Data can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of the associated LTCLK. This option is controlled via the LTCLKI control bit in Master Control Register 2 (see Section 4.2). Also, the data can be internally inverted before being multiplexed if enabled via the LTDATI control bit in Master Control Register 2 (see Section 4.2). When the M13 / E13 multiplexer is disabled, then these inputs are ignored and should be tied low.

Signal Name: **LTCLKA / LTCLKB**
Signal Description: **Low Speed (T1 or E1) Transmit Insert Port Serial Clock Inputs**
Signal Type: **Input**
These two input signals are used to clock data into the device that will be inserted into one of the 28 T1 data streams or into one of the 16/21 E1 data streams (see Section 7.4). The T1 or E1 serial data streams at the associated LTDAT signals can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of LTCLKA/LTCLKB. This option is controlled via the LTCLKI control bit in Master Control Register 2 (see Section 4.2). When the M13 / E13 multiplexer is disabled, then these inputs are ignored and should be tied low.

Signal Name: **LTCCLK**
Signal Description: **Low Speed (T1 or E1) Transmit Common Clock Input**
Signal Type: **Input**
If enabled via the LTCCEN in Master Control Register 1 (see Section 4.2), all 28 LTCLK or 16 LTCLK signals are disabled and all the data at the 28 LTDAT or 16 LTDAT inputs (as well as the LTDATA and LTDATB inputs) will be clocked into the device using the LTCCLK signal. In T3 mode, LTCCLK would be a 1.544 MHz clock and in E3 mode, LTCCLK would be 2.048 MHz. If not used, this signal should be tied low. If this signal is used, then all of the LTCLK signals should be tied low. This signal can be internally inverted. This option is controlled via the LTCLKI control bit in Master Control Register 2 (see Section 4.2).

2.7 HIGH SPEED (T3 OR E3) RECEIVE PORT SIGNAL DESCRIPTION

Signal Name: **HRPOS / HRNEG**
Signal Description: **High Speed (T3 or E3) Receive Serial Data Inputs**
Signal Type: **Input**
These input signals sample the serial data from the incoming T3 data streams or E3 data streams. Data can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of the associated HRCLK. This option is controlled via the HRCLKI control bit in Master Control Register 2 (see Section 4.2).

Signal Name: **HRCLK**
Signal Description: **High Speed (T3 or E3) Receive Serial Clock Input**
Signal Type: **Input**
This signal is used to clock data in from the incoming T3 or E3 data streams. The T3 or E3 serial data streams at the HRPOS and HRNEG signals can be clocked into the device either on falling edges (normal clock mode) or rising edges (inverted clock mode) of HRCLK. This option is controlled via the HRCLKI control bit in Master Control Register 2 (see Section 4.2).

Note: The HRCLK must be present for the Host to be able to obtain status information (except the LOTC and LORC status bits – see Section 4.3) from the device.

2.8 HIGH SPEED (T3 OR E3) TRANSMIT PORT SIGNAL DESCRIPTION

Signal Name: **HTPOS / HTNEG**
Signal Description: **High Speed (T3 or E3) Transmit Serial Data Outputs**
Signal Type: **Output**
These output signals present the outgoing T3 data streams or E3 data streams. Data can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of HTCLK. This option is controlled via the HTCLKI control bit in Master Control Register 2 (see Section 4.2). Also, these outputs can be forced high or low via the HTDATH and HTDATL control bits respectively in Master Control Register 2 (see Section 4.2).

Signal Name: **HTCLK**
Signal Description: **High Speed (T3 or E3) Receive Serial Clock Output**
Signal Type: **Output**
This output signal is used to clock T3 or E3 data out of the device. The T3 or E3 serial data streams at the HTPOS and HTNEG signals can be clocked out of the device either on rising edges (normal clock mode) or falling edges (inverted clock mode) of HTCLK. This option is controlled via the HTCLKI control bit in Master Control Register 2 (see Section 4.2).

2.9 JTAG SIGNAL DESCRIPTION

Signal Name: **JTCLK**
Signal Description: **JTAG IEEE 1149.1 Test Serial Clock**
Signal Type: **Input**
This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, this signal should be pulled high.

Signal Name: **JTDI**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Input**
Signal Type: **Input (with internal 10K pull up)**
Test instructions and data are clocked into this signal on the rising edge of JTCLK. If not used, this signal should be pulled high. This signal has an internal pull-up.

Signal Name: **JTDO**
Signal Description: **JTAG IEEE 1149.1 Test Serial Data Output**
Signal Type: **Output**
Test instructions are clocked out of this signal on the falling edge of JTCLK. If not used, this signal should be left open circuited.

Signal Name: **JTRST***
Signal Description: **JTAG IEEE 1149.1 Test Reset**
Signal Type: **Input (with internal 10K pull up)**
This signal is used to asynchronously reset the test access port controller. At power up, JTRST must be set low and then high. This action will set the device into the boundary scan bypass mode allowing normal device operation. If boundary scan is not used, this signal should be held low. This signal has an internal pull-up.

Signal Name: **JTMS**
Signal Description: **JTAG IEEE 1149.1 Test Mode Select**
Signal Type: **Input (with internal 10K pull up)**
This signal is sampled on the rising edge of JTCLK and is used to place the test port into the various defined IEEE 1149.1 states. If not used, this signal should be pulled high. This signal has an internal pull-up.

2.10 SUPPLY, TEST, RESET AND MODE SIGNAL DESCRIPTION

Signal Name: **RST***
Signal Description: **Global Hardware Reset**
Signal Type: **Input (with internal 10K pull up)**
This active low asynchronous signal causes the device to be reset. When this signal is forced low, it causes all of the internal registers to be forced to 00h and the high speed T3/E3 ports as well as the low speed T1/E1 ports to source an unframed all ones data pattern. The device will be held in a reset state as long as this signal is low. This signal should be activated after the hardware configuration signals (LIEN and T3E3MS) and the clocks (FTCLK, LTCLK, HRCLK, and LITCLK) are stable and must be returned high before the device can be configured for operation.

Signal Name: **T3E3MS**
Signal Description: **T3 / E3 Mode Select Input**
Signal Type: **Input**
This signal determines whether the DS3112 will operate in either the T3 Mode or the E3 Mode. It acts as a global control bit for the entire DS3112. This signal should be set into the proper state before a hardware reset is issued via the RST* signal. This input is coupled with the G747E input to create a special test mode whereby all of the outputs are 3-stated. See Table 2.10A.

0 = T3 Mode
1 = E3 Mode

Signal Name: **G747E**
Signal Description: **G747 Mode Enable Input**
Signal Type: **Input**
This signal determines whether the DS3112 will operate in either the T3 Mode or the G747 Mode. It acts as a global control bit for the entire DS3112. This signal should be set into the proper state before a hardware reset is issued via the RST* signal. This input is coupled with the T3E3MS input to create a special test mode whereby all of the outputs are 3-stated. See Table 2.10A.

0 = T3 Mode
1 = G747 Mode

Mode Select Decode Table 2.10A

T3E3MS	G747E	Mode Selected
0	0	T3 or M13 operation
0	1	G747 operation
1	0	E3 or E13 operation
1	1	special test mode that 3-states all outputs

Signal Name: **TEST***
Signal Description: **Factory Test Input**
Signal Type: **Input (with internal 10K pull up)**
This input should be left open circuited by the user.

Signal Name: **VSS**
Signal Description: **Digital Ground Reference**
Signal Type: **n/a**
All VSS signals should be tied together.

Signal Name: **VDD**
Signal Description: **Digital Positive Supply**
Signal Type: **n/a**
3.3V (± 5%). All VDD signals should be tied together.

SECTION 3: MEMORY MAP

Address	Acronym	R/W	Register Name	Section
00	MRID	R/W	Master Reset and ID Register.	4.1
02	MC1	R/W	Master Configuration Register 1.	4.2
04	MC2	R/W	Master Configuration Register 2.	4.2
06	MC3	R/W	Master Configuration Register 3.	4.2
08	MSR	R	Master Status Register.	4.3
0A	IMSR	R/W	Interrupt Mask Register for MSR.	4.3
0C	TEST	R/W	Test Register.	4.4
0E			not assigned	
10	T3E3CR	R/W	T3 / E3 Control Register.	5.2
12	T3E3SR	R	T3 / E3 Status Register.	5.3
14	IT3E3SR	R/W	Interrupt Mask for T3E3SR.	5.3
16	T3E3INFO	R	T3 / E3 Information Register.	5.3
18	T3E3EIC	R/W	T3 /E3 Error Insert Control Register.	5.3
1A			not assigned	
1C			not assigned	
1E			not assigned	
20	BPVCR	R	T3 / E3 BiPolar Violation (BPV) Count Register.	5.4
22	EXZCR	R	T3 / E3 EXcessive Zero (EXZ) Count Register.	5.4
24	FECR	R	T3 / E3 Frame Error Count Register.	5.4
26	PCR	R	T3 Parity Bit Error Count Register.	5.4
28	CPCR	R	T3 C-Bit Parity Error Count Register.	5.4
2A	FEBECR	R	T3 Far End Block Error or E3 RAI Count Register.	5.4
2C			not assigned	
2E			not assigned	
30	T2E2CR1	R/W	T2 / E2 Control Register 1.	6.2
32	T2E2CR2	R/W	T2 / E2 Control Register 2.	6.2
34	T2E2SR1	R/W	T2 / E2 Status Register 1.	6.3
36	T2E2SR2	R/W	T2 / E2 Status Register 2.	6.3
38			not assigned	
3A			not assigned	
3C			not assigned	
3E			not assigned	
40	T1E1RAIS1	R/W	T1 / E1 Receive Path AIS Generation Control Register 1.	6.4
42	T1E1RAIS2	R/W	T1 / E1 Receive Path AIS Generation Control Register 2.	6.4
44	T1E1TAIS1	R/W	T1 / E1 Transmit Path AIS Generation Control Register 1.	6.4
46	T1E1TAIS2	R/W	T1 / E1 Transmit Path AIS Generation Control Register 2.	6.4
48			not assigned	
4A			not assigned	
4C			not assigned	
4E			not assigned	
50	T1E1LLB1	R/W	T1 / E1 Line Loopback Control Register 1.	7.2
52	T1E1LLB2	R/W	T1 / E1 Line Loopback Control Register 2.	7.2
54	T1E1DLB1	R/W	T1 / E1 Diagnostic Loopback Control Register 1.	7.2
56	T1E1DLB2	R/W	T1 / E1 Diagnostic Loopback Control Register 2.	7.2
58	T1LBCR1	R/W	T1 Line Loopback Command Register 1.	7.2
5A	T1LBCR2	R/W	T1 Line Loopback Command Register 2.	7.2

Address	Acronym	R/W	Register Name	Section
5C	T1LBSR1	R	T1 Line Loopback Status Register 1.	7.3
5E	T1LBSR2	R	T1 Line Loopback Status Register 2.	7.3
60	T1E1SDP	R/W	T1 / E1 Select Register for Receive Drop Ports A and B.	7.4
62	T1E1SIP	R/W	T1 / E1 Select Register for Transmit Drop Ports A and B.	7.4
64			not assigned	
66			not assigned	
68			not assigned	
6A			not assigned	
6C			not assigned	
6E	BERTMC	R/W	BERT Mux Control Register.	8.2
70	BERTC0	R/W	BERT Control 0.	8.2
72	BERTC1	R/W	BERT Control 1.	8.2
74	BERTRP0	R/W	BERT Repetitive Pattern Set 0 (lower word).	8.2
76	BERTRP1	R/W	BERT Repetitive Pattern Set 1 (upper word).	8.2
78	BERTBC0	R	BERT Bit Counter 0 (lower word).	8.2
7A	BERTBC1	R	BERT Bit Counter 1 (upper word).	8.2
7C	BERTEC0	R	BERT Error Counter 0 (lower word).	8.2
7E	BERTEC1	R	BERT Error Counter 1 (upper word).	8.2
80	HCR	R/W	HDLC Control Register.	9.2
82	RHDLC	R	Receive HDLC FIFO Register.	9.2
84	THDLC	W	Transmit HDLC FIFO Register.	9.2
86	HSR	R	HDLC Status Register.	9.3
88	IHSR	R/W	Interrupt Mask Register for HSR.	9.3
8A			not assigned	
8C			not assigned	
8E			not assigned	
90	FCR	R/W	FEAC Control Register.	10.2
92	FSR	R	FEAC Status Register.	10.3
94			not assigned	
96			not assigned	
98			not assigned	
9A			not assigned	
9C			not assigned	
9E			not assigned	

Note: Addresses A0 to FF are not assigned.

SECTION 4: MASTER DEVICE CONFIGURATION AND STATUS/INTERRUPT

4.1 MASTER RESET AND ID REGISTER DESCRIPTION

The Master Reset and ID (MRID) register can be used to globally reset the device. When the RST bit is set to one, all of the internal registers will be placed into their default state which is 0000h. A reset can also be invoked by the RST* hardware signal.

The upper byte of the MRID register is read only and it can be read by the Host to determine the chip revision. Contact the factory for specifics on the meaning of the value read from the ID0 to ID7 bits.

Register Name: **MRID**
Register Description: **Master Reset and ID Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	n/a	n/a	T3E3RSY	T2E2RSY	RFIFOR	RST
Default	-	-	-	-	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Default	1	0	1	0	0	0	0	1

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Master Software Reset (RST). When this bit is set to a one by the Host, it will force all of the internal registers to their default state which is 0000h and forces the T3/E3 and T1/E1 outputs to send an all ones pattern. This bit must be set high for a minimum of 100ns. This software bit is logically OR'ed with the hardware signal RST*.

0 = normal operation
1 = force all internal registers to their default value of 0000h

Bit 1 / Low Speed (T1/E1) Receive FIFO Reset (RFIFOR). A 0 to 1 transition on this bit will cause the receive T1/E1 demux FIFOs to be reset which will causes them to be flushed. See the DS3112 Block Diagrams in Figures 1A and 1B for details on the placement of the FIFOs within the chip. This bit must be cleared and set again for a subsequent reset to occur.

Bit 2 / T2/E2/G747 Force Receive Framer Resynchronization (T2E2RSY). A 0 to 1 transition on this bit will cause all seven of the T2 receive framers or all four of the E2 receive framers or all seven of the G747 framers to resynchronize. This bit must be cleared and set again for a subsequent resynchronization to occur.

Bit 3 / T3/E3 Force Receive Framer Resynchronization (T3E3RSY). A 0 to 1 transition on this bit will cause the T3 receive framer or the E3 receive framer to resynchronize. This bit must be cleared and set again for a subsequent resynchronization to occur.

Bits 8 to 15 / Chip Revision ID Bit 0 to 7 (ID0 to ID7). Read only. Contact the factory for details on the meaning of the ID bits.

4.2 MASTER CONFIGURATION REGISTERS DESCRIPTION

Register Name: **MC1**
Register Description: **Master Configuration Register 1**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	FTSOFC	LOTCMC	UNI	MECU	AECU	CBEN	UNCHEN	ZCSD
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LLTM	DENMS	LRCCEN	LTCCEN
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Zero Code Suppression Disable (ZCSD).
0 = enable the B3ZS and HDB3 encoders/decoders
1 = disable the B3ZS and HDB3 encoders/decoders

Bit 1 / T3/E3 Unchannelized Mode Enable (UNCHEN). When this bit is set low, the M13 / E13 / G747 multiplexer is enabled and data at the FTD input is ignored. When this bit is set high, the M13 / E13 / G747 multiplexer is disabled and the LTDAT inputs are ignored. The table below displays which bits are not sampled at the FTD input when UNCHEN = 1.

DS3112 Mode	**Bits Positions Not Sampled At FTD**
T3 M23 (C-Bit Parity disabled)	F / P / M / C / X
T3 C-Bit Parity	F / P / M / X
E3	FAS / Sn / RAI

0 = enable the M13 / E13 / G747 multiplexers and disable the FTD Input
1 = disable the M13 / E13 / G747 multiplexers and enable the FTD Input

Bit 2 / T3 C-Bit Parity Mode Enable (CBEN). This bit is only active when the device is T3 Mode. When this bit is set low, C-Bit Parity is defeated and the C Bits are sourced from the M23 Multiplexer Block (see Figure 1A). This bit should not be set low in the T3 Unchannelized Mode (UNCHEN = 1). When this bit is set high, C-Bit Parity mode is enabled and the C Bits are sourced from the T3 Framer Block (see Figures 1A and 1C).

0 = disable C-Bit Parity mode (also known as the M23 Mode)
1 = enable C-Bit Parity mode

Bit 3 / Automatic One Second Error Counters Update Defeat (AECU). When this bit is set low, the device will automatically update the T3/E3 performance error counters on an internally created one second boundary. The Host will be notified of the update via the setting of the OST status bit in the Master Status Register. In this mode, the Host has a full one second period to retrieve the error information before if will be overwritten with the next update. When this bit is set high, the device will defeat the automatic one second update and enable a manual update mode. In the manual update mode, the device relies on either the Framer Manual Error Counter Update (FRMECU) hardware input signal or the MECU control bit to update the error counters. The FRMECU hardware input signal and MECU control bit are logically OR'ed and hence a zero to one transition on either will initiate an error counter update to occur. After either the FRMECU signal or MECU bit has toggled, the Host must wait at least 100 ns before reading the error counters to allow the device time to complete the update.

0 = enable the automatic update mode and disable the manual update mode
1 = disable the automatic update mode and enable the manual update mode

Bit 4 / Manual Error Counter Update (MECU). A zero to one transition on this bit will cause the device to update the performance error counters. This bit is ignored if the AECU control bit is set low. This bit must be cleared and set again for a subsequent update. This bit is logically OR'ed with the external FRMECU hardware input signal. After this bit has toggled, the Host must wait at least 100 ns before reading the error counters to allow the device time to complete the update.

Bit 5 / High Speed (T3/E3) Port Unipolar Enable (UNI). When this bit is set low, the device will output a bipolar coded signal at HTPOS and HTNEG and expect a bipolar coded signal at HRPOS and HRNEG. When this bit is set high, the device will output a NRZ coded signal at HTPOS and expect a NRZ coded signal at HRPOS. In the unipolar mode, the device will force the HTNEG output low and the HRNEG input is ignored and should be tied low. In the unipolar mode, the B3ZS and HDB3 coder/decoders should be disabled by setting the ZCSD bit to one (ZCSD = 1).

0 = bipolar mode
1 = unipolar mode

Bit 6 / Loss Of Transmit Clock Mux Control (LOTCMC). The DS3112 can detect if the FTCLK fails to transition. If this bit is set low, the device will take no action (other than setting the LOTC status bit) when the FTCLK fails to transition. When this bit is set high, the device will automatically switch to the input receive clock (HRCLK) when the FTCLK fails and transmit AIS.

0 = do not switch to the HRCLK signal if FTCLK fails to transition
1 = automatically switch to the HRCLK signal if the FTCLK fails to transition and send AIS

Bit 7 / T3/E3 Transmit Frame Sync I/O Control (FTSOFC). When this bit is set low, the FTSOF signal will be an output and will pulse for one FTCLK cycle at the beginning of each frame. When this bit is high, the FTSOF signal is an input and the device uses it to determine the frame boundaries.

0 = FTSOF is an output
1 = FTSOF is an input

Bit 8 / Low Speed (T1/E1) Transmit Port Common Clock Enable (LTCCEN). When this bit is set high, the LTCLK1 to LTCLK28 and LTCLKA and LTCLKB inputs are ignored and a common clock sourced via the LTCCLK input is used in their place.

0 = disable LTCCLK
1 = enable LTCCLK

Bit 9 / Low Speed (T1/E1) Receive Port Common Clock Enable (LRCCEN). When this bit is set high, the LRCLK1 to LRCLK28 and LRCLKA and LRCLKB outputs will all be sourced from the LRCCLK input. This configuration can only be used in applications where it can be insured that all of the T1 or E1 channels from the far end are being sourced from a common clock.

0 = disable LRCCLK
1 = enable LRCCLK

Bit 10 / High Speed (T3/E3) Data Enable Mode Select (DENMS). When this bit is set low, the FRDEN and FTDEN outputs will be asserted during payload data and deasserted during overhead data. When this bit is high, FRDEN and FTDEN are gapped clocks that pulse during payload data and are suppressed during overhead data.

0 = FRDEN and FTDEN are Data Enables
1 = FRDEN and FTDEN are Gapped Clocks

Bit 11 / Low Speed (T1/E1) Port Loop Timed Mode (LLTM). When this bit is set low, the low speed T1 and E1 receive clocks (LRCLK) are not routed to the transmit side. When this bit is high, the LRCLKs are routed to the transmit side to be used as the transmit T1 and E1 clocks. When enabled, all the low speed ports are looped timed. This control bit affects all the low speed ports. The device is not capable of setting individual low speed ports into and out of looped timed mode. See the Block Diagram in Figures 1A and 1B for more details.

0 = disable loop timed mode (LRCLK is not used to replace the associated LTCLK)
1 = enable loop timed mode (LRCLK replaces the associated LTCLK)

Register Name: **MC2**
Register Description: **Master Configuration Register 2**
Register Address: **04h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	HTDATL	HTDATH	HRDATI	HRCLKI	HTDATI	HTCLKI
Default	-	-	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LRDATI	LRCLKI	LTDATI	LTCLKI
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / HTCLK Invert Enable (HTCLKI).
0 = do not invert the HTCLK signal (normal mode)
1 = invert the HTCLK signal (inverted mode)

Bit 1 / HTPOS/HTNEG Invert Enable (HTDATI).
0 = do not invert the HTPOS and HTNEG signals (normal mode)
1 = invert the HTPOS and HTNEG signals (inverted mode)

Bit 2 / HRCLK Invert Enable (HRCLKI).
0 = do not invert the HRCLK signal (normal mode)
1 = invert the HRCLK signal (inverted mode)

Bit 3 / HRPOS/HRNEG Invert Enable (HTDATI).
0 = do not invert the HRPOS and HRNEG signals (normal mode)
1 = invert the HRPOS and HRNEG signals (inverted mode)

Bit 4 / HTPOS/HTNEG Force High Disable (HTDATH).
Please note that this bit must be set by the Host in order for T3/E3 traffic to be output from the device.
0 = force the HTPOS and HTNEG signals high (force high mode)
1 = allow normal transmit data to appear at the HTPOS and HTNEG signals (normal mode)

Bit 5 / HTPOS/HTNEG Force Low Enable (HTDATL).
0 = allow normal transmit data to appear at the HTPOS and HTNEG signals (normal mode)
1 = force the HTPOS and HTNEG signals low (force low mode)

Bit 8 / LTCLK Invert Enable (LTCLKI).
0 = do not invert the LTCLK[n], LTCLKA, LTCLKB, and LTCCLK signals (normal mode)
1 = invert the LTCLK[n], LTCLKA, LTCLKB, and LTCCLK signals (inverted mode)

Bit 9 / LTDAT Invert Enable (LTDATI).
0 = do not invert the LTDAT[n], LTDATA and LTDATB signals (normal mode)
1 = invert the LTDAT[n], LTDATA and LTDATB signals (inverted mode)

Bit 10 / LRCLK Invert Enable (LRCLKI).
0 = do not invert the LRCLK[n], LRCLKA, LRCLKB, and LRCCLK signals (normal mode)
1 = invert the LRCLK[n], LRCLKA, LRCLKB, and LRCCLK signals (inverted mode)

Bit 11 / LRDAT Invert Enable (LRDATI).
0 = do not invert the LRDAT[n], LRDATA and LRDATB signals (normal mode)
1 = invert the LRDAT[n], LRDATA and LRDATB signals (inverted mode)

Register Name: **MC3**
Register Description: **Master Configuration Register 3**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	FRSOFI	FRCLKI	FRDI	FRDENI	FTSOFI	FTCLKI	FTDI	FTDENI
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / FTDEN Invert Enable (FTDENI).
0 = do not invert the FTDEN signal (normal mode)
1 = invert the FTDEN signal (inverted mode)

Bit 1 / FTD Invert Enable (FTDI).
0 = do not invert the FTD signal (normal mode)
1 = invert the FTD signal (inverted mode)

Bit 2 / FTCLK Invert Enable (FTCLKI).
0 = do not invert the FTCLK signal (normal mode)
1 = invert the FTCLK signal (inverted mode)

Bit 3 / FTSOF Invert Enable (FTSOFI).
0 = do not invert the FTSOF signal (normal mode)
1 = invert the FTSOF signal (inverted mode)

Bit 4 / FRDEN Invert Enable (FRDENI).
0 = do not invert the FRDEN signal (normal mode)
1 = invert the FRDEN signal (inverted mode)

Bit 5 / FRD Invert Enable (FRDI).
0 = do not invert the FRD signal (normal mode)
1 = invert the FRD signal (inverted mode)

Bit 6 / FRCLK Invert Enable (FRCLKI).
0 = do not invert the FRCLK signal (normal mode)
1 = invert the FRCLK signal (inverted mode)

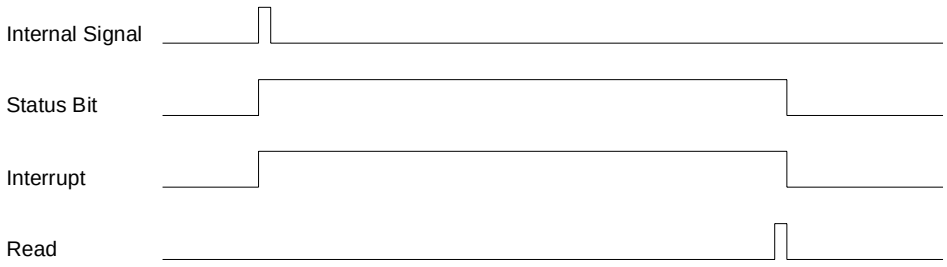
Bit 7 / FRSOF Invert Enable (FRSOFI).
0 = do not invert the FRSOF signal (normal mode)
1 = invert the FRSOF signal (inverted mode)

4.3 MASTER STATUS AND INTERRUPT REGISTER DESCRIPTION

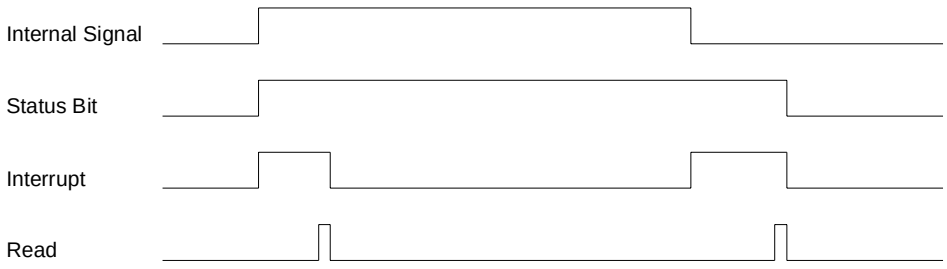
A Note About The Status Registers in the DS3112

The status registers in the DS3112 allow the Host to monitor the real time condition of the device. Most of the status bits in the device can cause a hardware interrupt to occur. Also, most of the status bits within the device are latched to insure that the Host can detect changes in state and the true status of the device. There are three types of status bits in the DS3112. The first type is called an **event** status bit and it is derived from a momentary condition or state that occurs within the device. The event status bits are always cleared when read and can generate an interrupt when they are asserted. An example of an event status bit is the One Second Timer Boundary Occurrence (OST). The second type of status bit is called an **alarm** status bit and it is derived from conditions that can occur for longer than an instance. The alarm status bits will be cleared when read unless the alarm is still present. The alarm status bits generate interrupts on a change in state in the alarm (i.e. when it is asserted or deasserted). An example of an alarm status bit is the Loss Of Frame (LOF). The third type of status bit is called a **real time** status bit. The real time status bit remains active as long as the condition exists and will generate an interrupt as long as the condition exists. An example of a real time status bit is the Loss Of Transmit Clock (LOTC).

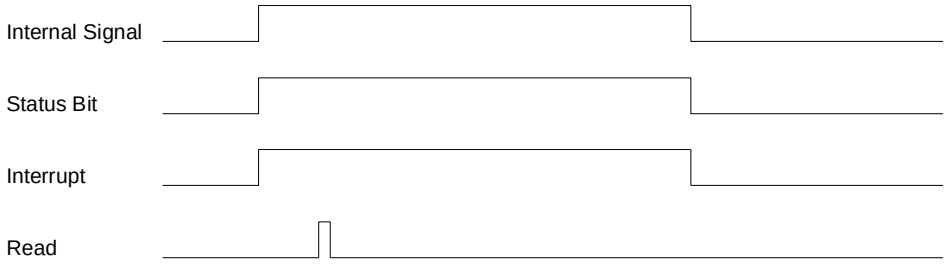
Event Status Bit Figure 4.3A



Alarm Status Bit Figure 4.3B



Real Time Status Bit Figure 4.3C



A Note About the MSR

The Master Status Register (MSR) is a special status register that can be used to help the Host quickly locate changes in device status. There is a status bit in the MSR for each of the major blocks within the DS3112. When an alarm or event occurs in one of these blocks, the device can be configured to set a bit in the MSR. Status bits in the MSR can also cause a hardware interrupt to occur. In either polled or interrupt driven software routines, the Host can first read the MSR to locate which status registers need to be serviced.

Register Name: **MSR**
Register Description: **Master Status Register**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	T2E2SR2	T2E2SR1	FEAC	HDLC	BERT	COVF	OST
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	G747	T3E3MS	LORC	LOTC	T3E3SR	T1LB
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / One Second Timer Boundary Occurrence (OST). This latched read only event status bit will be set to a one on each one second boundary as timed by the DS3112. The device chooses an arbitrary one second boundary that is timed from the HRCLK signal. This bit will be cleared when read and will not be set again until another one second boundary has occurred. The setting of this status bit can cause a hardware interrupt to occur if the OST bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 1 / Counter Overflow Event (COVF). This latched read only event status bit will be set to a one if any of the error counters saturates (the error counters saturate when full). This bit will be cleared when read even if one or more of the error counters is still saturated. The setting of this status bit can cause a hardware interrupt to occur if the COVF bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 2 / Change in BERT Status (BERT). This read only real time status bit will be set to a one if there is a major change of status in the BERT receiver. A major change of status is defined as either a change in the receive synchronization (i.e. the BERT has gone into or out of receive synchronization), a bit error has been detected, or an overflow has occurred in either the Bit Counter or the Error Counter. The Host must read the status bits of the BERT in the BERT Status Register (BERTEC0) to determine the change of state. This bit will be cleared when the BERTEC0 is read and will not be set again until the BERT has experienced another change of state. The setting of this status bit can cause a hardware interrupt to occur if the BERT bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the BERTEC0 register is read. See Figure 4.3D.

Bit 3 / Change in HDLC Status (HDLC). This read only real time status bit will be set to a one if there is a change of status in the HDLC controller. The Host must read the status bits of the HDLC in the HDLC Status Register (HSR) to determine the change of state. This bit will be cleared when the HSR is read and will not be set again until the HDLC has experienced another change of state. The setting of this status bit can cause a hardware interrupt to occur if the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the HSR register is read. See Figure 4.3E.

Bit 4 / Change in FEAC Status (FEAC). This read only real time status bit will be set to a one when the FEAC controller has detected and verified a new Far End Alarm and Control (FEAC) 16-bit codeword. This bit will be cleared when the FEAC Status Register (FSR) is read and will not be set again until the FEAC controller has detected and verified another new codeword. The setting of this status bit can cause a hardware interrupt to occur if the FEAC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the FSR register is read.

Bit 5 / Change in T2/E2 LOF or AIS Status (T2E2SR1). This read only real time status bit will be set to a one when one or more of the T2/E2/G747 framers have detected a change in either Loss Of Frame (LOF) or Alarm Indication Signal (AIS). See the T2E2SR1 register description in Section 6.3 for more details. This bit will be cleared when the T2E2SR1 register is read. The setting of this status bit can cause a hardware interrupt to occur if the T2E2SR1 bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the T2E2SR1 register is read. See Figure 4.3F.

Bit 6 / Change in T2/E2 RAI Status (T2E2SR2). This read only real time status bit will be set to a one when one or more of the T2/E2/G747 framers have detected a change in the detection of the Remote Alarm Indication (RAI) signal. See the T2E2SR2 register description in Section 6.3 for more details. This bit will be cleared when the T2E2SR2 register is read. The setting of this status bit can cause a hardware interrupt to occur if the T2E2SR2 bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the T2E2SR2 register is read. See Figure 4.3G.

Bit 8 / T1 Loopback Detected (T1LB). This read only real time status bit will be set to a one when one or more of the T2 framers have detects an active T1 loopback command. See the T1LBSR1 and T1LBSR2 register descriptions in Section 7.3 for more details. This bit will be cleared when the T1 loopback command is no longer active on any of the lines. The setting of this status bit can cause a hardware interrupt to occur if the T1LB bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the none of the T2 framers detects an active T1 loopback command. See Figure 4.3H.

Bit 9 / Change in T3/E3 Framer Status (T3E3SR). This read only real time status bit will be set to a one when the T3/E3 framer has detected a change in RAI, AIS, LOF, LOS, or T3 Idle signal or has detected the start of a Transmit or Receive Frame. See the T3E3SR register description in Section 5.3 for more details. This bit will be cleared when the T3E3SR register is read. The setting of this status bit can cause a hardware interrupt to occur if the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the T3E3SR register is read. See Figure 4.3I.

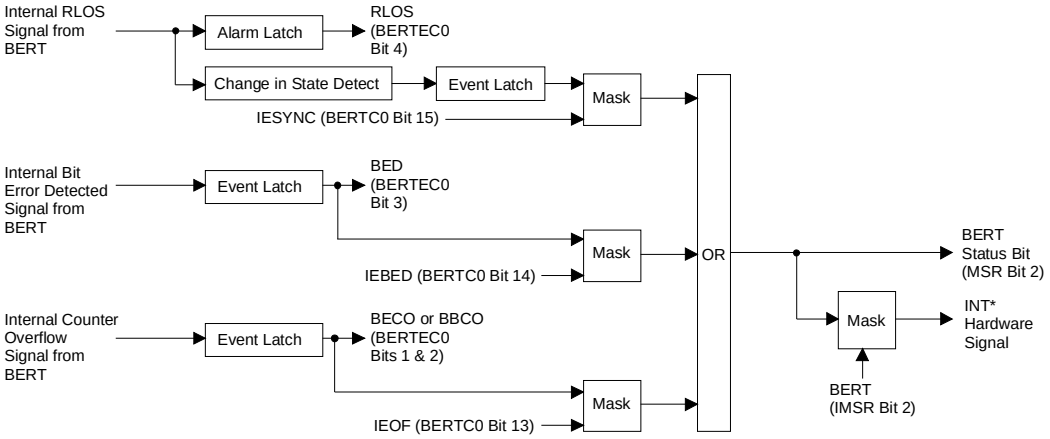
Bit 10 / Loss Of Transmit Clock Detected (LOTC). This read only real time status bit will be set to a one when the device detects that the FTCLK clock has not toggled for 200 ns (+/- 100 ns). This bit will be cleared when a clock is detected at the FTCLK input. The setting of this status bit can cause a hardware interrupt to occur if the LOTC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the device detects a clock at FTCLK. The HRCLK checks for the presence of the FTCLK. On reset, both the LOTC and LORC status bits will be set and then immediately cleared if the clock is present.

Bit 11 / Loss Of Receive Clock Detected (LORC). This read only real time status bit will be set to a one when the device detects that the HRCLK clock has not toggled for 200 ns (+/- 100 ns). This bit will be cleared when a clock is detected at the HRCLK input. The setting of this status bit can cause a hardware interrupt to occur if the LORC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when the device detects a clock at HRCLK. The FTCLK checks for the presence of the HRCLK. On reset, both the LOTC and LORC status bits will be set and then immediately cleared if the clock is present.

Bit 12 / State of the T3E3MS Input Signal (T3E3MS). This read only real time status bit reflects the current state of the external T3E3MS input signal. This status bit cannot generate an interrupt.

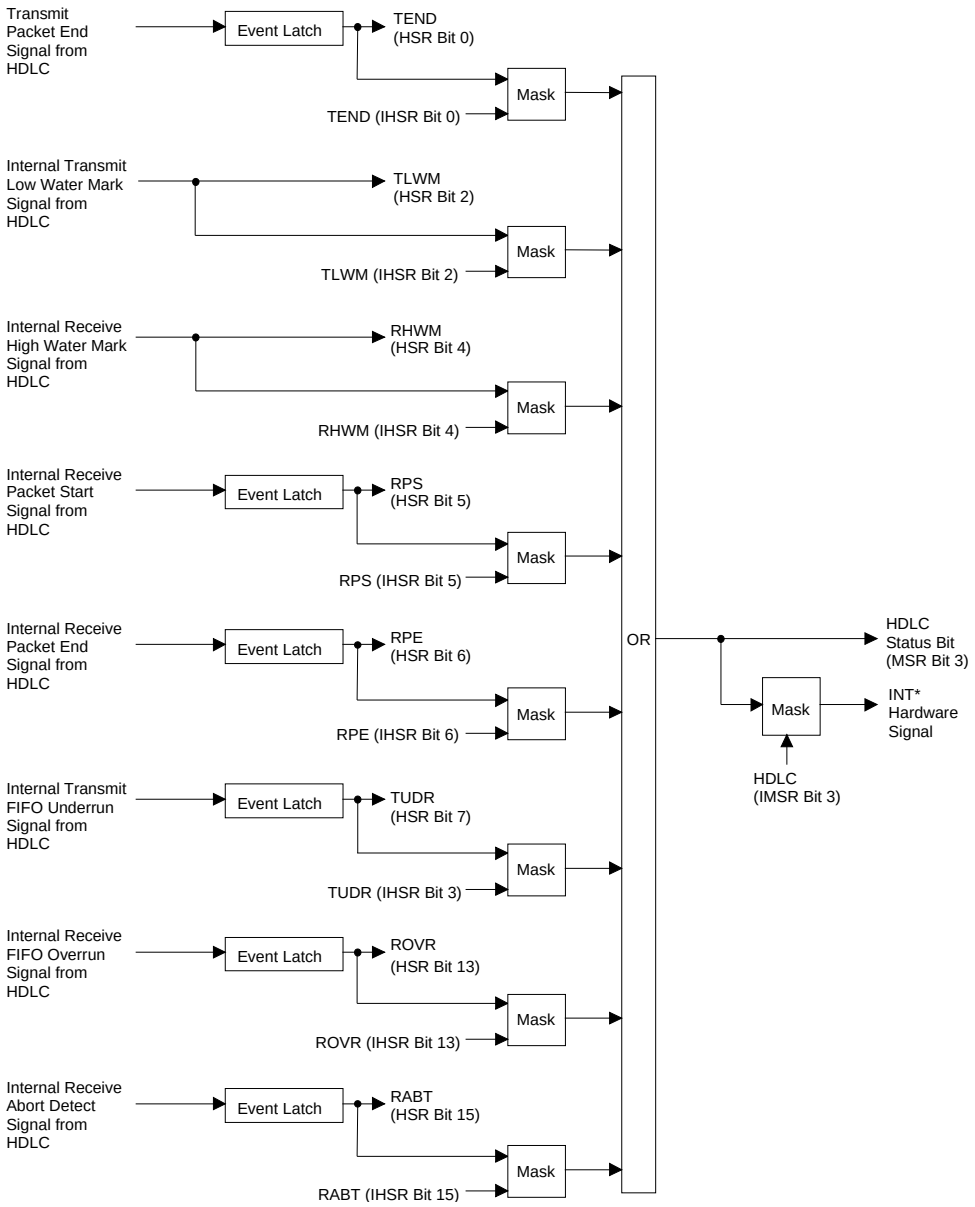
Bit 13 / State of the Input Signal (G747E). This read only real time status bit reflects the current state of the external G747E input signal. This status bit cannot generate an interrupt.

BERT Status Bit Flow Figure 4.3D



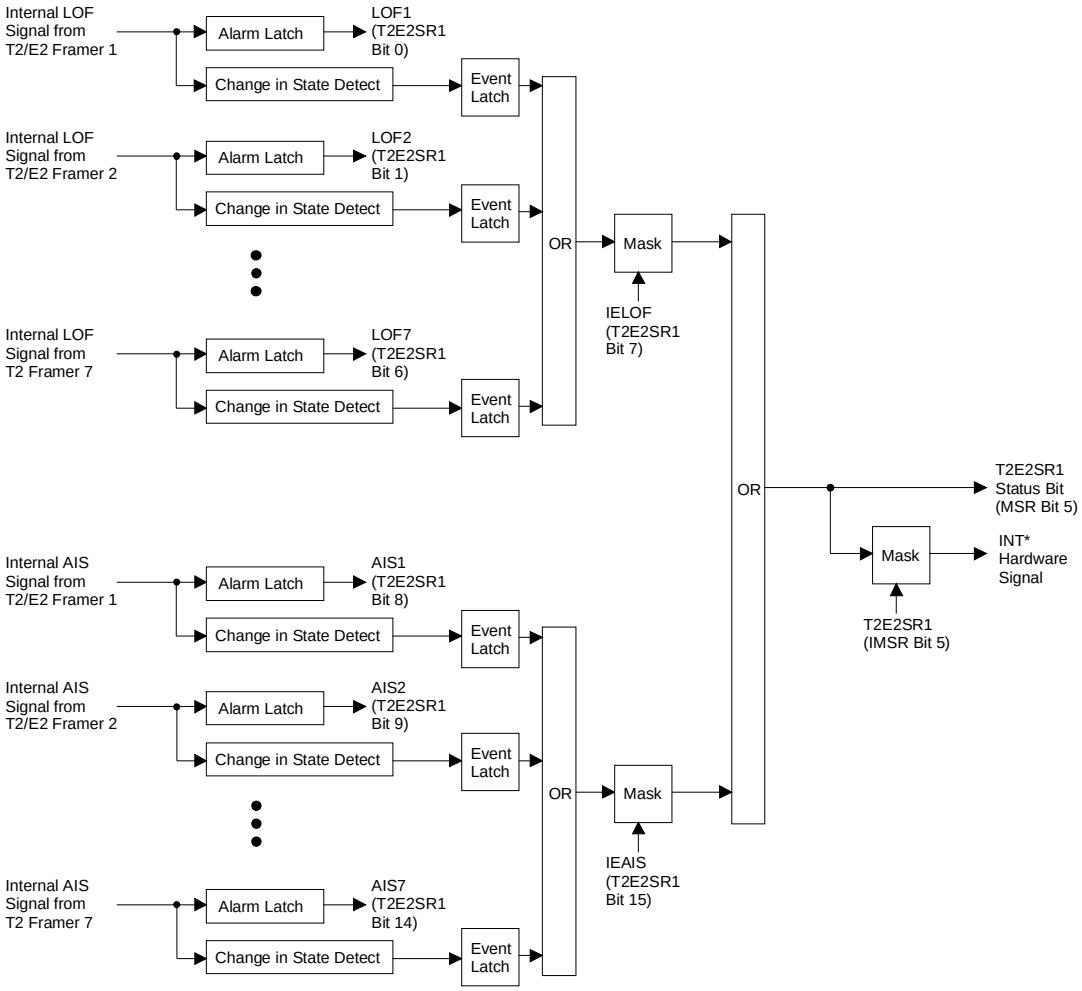
Note: All event and alarm latches above are cleared when the BERTEC0 register is read.

HDLC Status Bit Flow Figure 4.3E



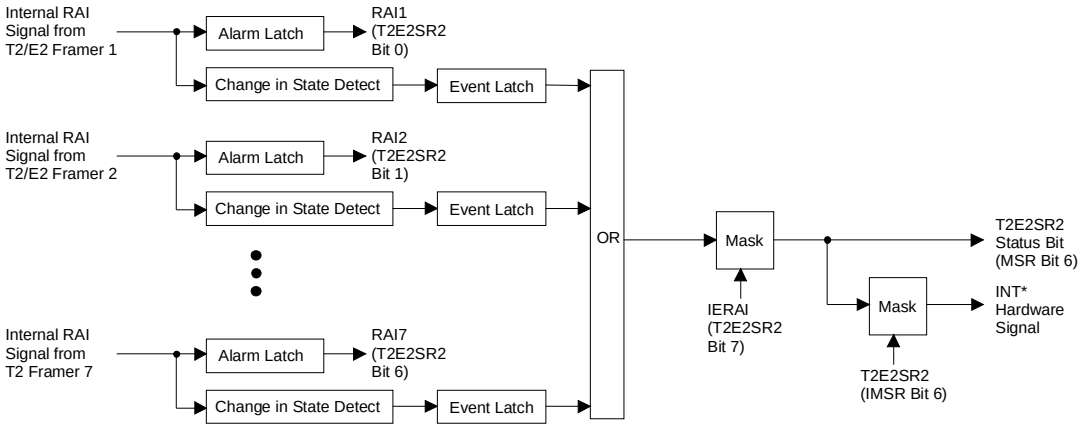
Note: All event latches above are cleared when the HSR register is read.

T2E2SR1 Status Bit Flow Figure 4.3F



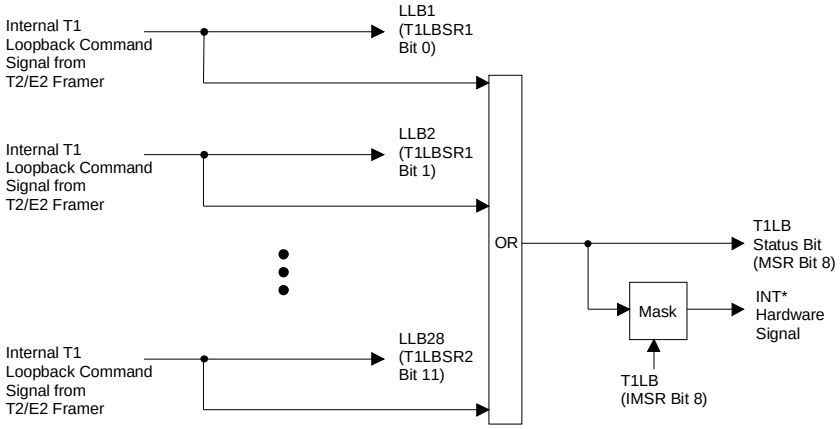
Note: All event and alarm latches above are cleared when the T2E2SR1 register is read.

T2E2SR2 Status Bit Flow Figure 4.3G

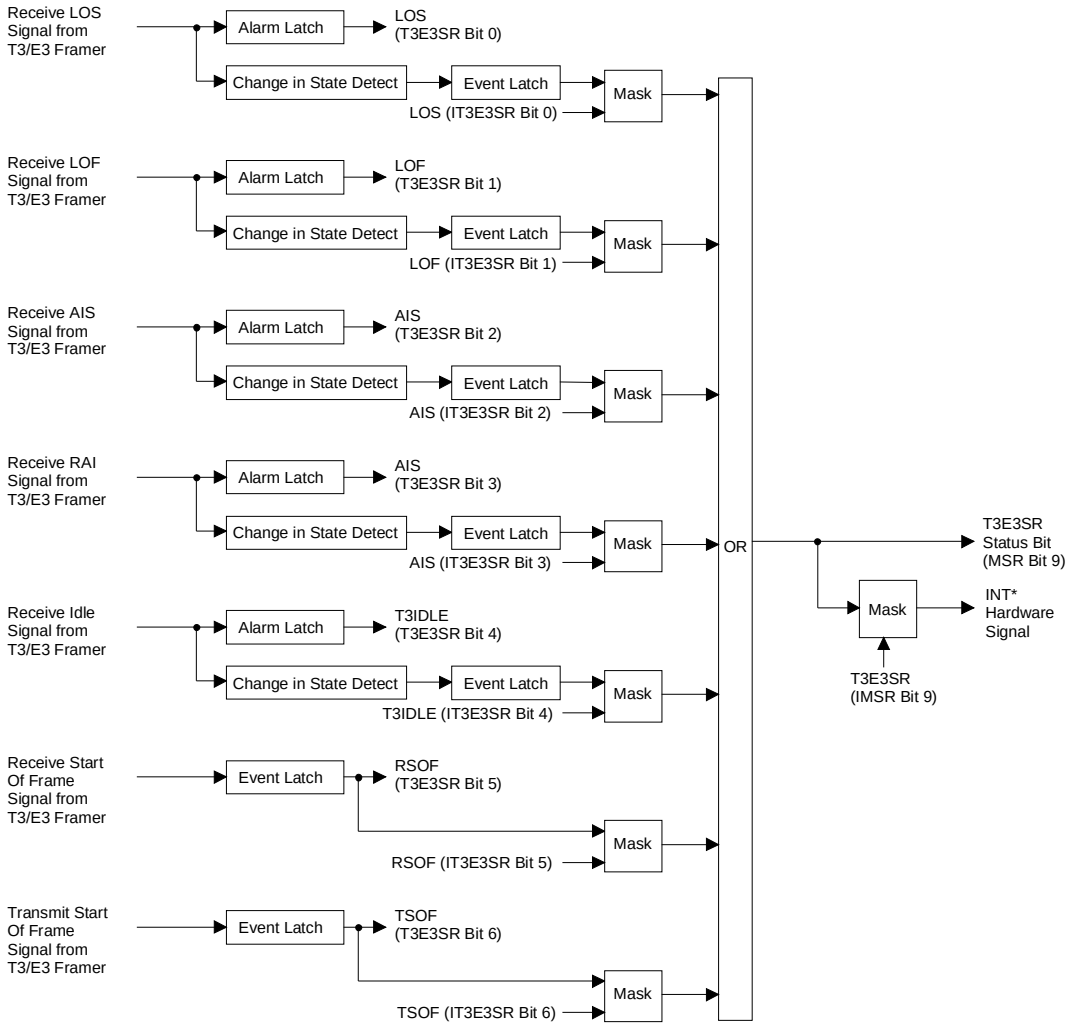


Note: All event and alarm latches above are cleared when the T2E2SR2 register is read.

T1LB Status Bit Flow Figure 4.3H



T3E3SR Status Bit Flow Figure 4.3I



Note: All event and alarm latches above are cleared when the T3E3SR register is read.

Register Name: **IMSR**
Register Description: **Interrupt Mask for Master Status Register**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	T2E2SR2	T2E2SR1	FEAC	HDLC	BERT	COVF	OST
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LORC	LOTC	T3E3SR	T1LB
Default	-	-	-	-	0	0	0	0

Bit 0 / One Second Timer Boundary Occurrence (OST).
0 = interrupt masked
1 = interrupt unmasked

Bit 1 / Counter Overflow Event (COVF).
0 = interrupt masked
1 = interrupt unmasked

Bit 2 / Change in BERT Status (BERT).
0 = interrupt masked
1 = interrupt unmasked

Bit 3 / Change in HDLC Status (HDLC).
0 = interrupt masked
1 = interrupt unmasked

Bit 4 / Change in FEAC Status (FEAC).
0 = interrupt masked
1 = interrupt unmasked

Bit 5 / Change in T2/E2 LOF or AIS Status (T2E2SR1).
0 = interrupt masked
1 = interrupt unmasked

Bit 6 / Change in T2/E2 RAI Status (T2E2SR2).
0 = interrupt masked
1 = interrupt unmasked

Bit 8 / T1 Loopback Detected (T1LB).
0 = interrupt masked
1 = interrupt unmasked

Bit 9 / Change in T3/E3 Framer Status (T3E3SR).
0 = interrupt masked
1 = interrupt unmasked

Bit 10 / Loss Of Transmit Clock (LOTC).
0 = interrupt masked
1 = interrupt unmasked

Bit 11 / Loss Of Receive Clock (LORC).
0 = interrupt masked
1 = interrupt unmasked

4.4 TEST REGISTER DESCRIPTION

Register Name: **TEST**
Register Description: **Test Register**
Register Address: **0Ch**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	FT5	FT4	FT3	FT2	FT1	FT0
Default	-	-	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 5 / Factory Test Bits (FT0 to FT5). These bits are used by the factory to place the DS3112 into the test mode. For normal device operation, these bits should be set to zero whenever this register is written to.

SECTION 5: T3 / E3 FRAMER

5.1 GENERAL DESCRIPTION

On the receive side, the T3/E3 framer locates the frame boundaries of the incoming T3 or E3 datastream and monitors the datastream for alarms and errors. Alarms are detected and reported in T3/E3 Status Register (T3E3SR) and the T3/E3 Information Register (T3E3INFO) which are described in Section 5.3. Errors are accumulated in a set of error counters (see Section 5.4). The Host can force the T3/E3 framer to resynchronize via the T3E3RSY control bit in the MRID register (see Section 4.1). On the transmit side, the device formats the outgoing datastream with the proper framing pattern and overhead and can generate alarms. It can also inject errors for diagnostic testing purposes (see the T3E3EIC register). The transmit side of the framer is called the "formatter".

The T3/E3 framer and formatter can be used in conjunction with the multiplexer or as a stand alone framer. This selection is made in the Master Configuration 1 (MC1) register (see Section 4.2).

T3/E3 Line Loopback

The Line Loopback loops the incoming T3/E3 data (the HRCLK, HRPOS, and HRNEG inputs) directly back to the transmit side (the HTCLK, HTPOS, and HTNEG outputs). When this loopback is enabled, the incoming receive data continues to pass through the device but the data output from the T3/E3 formatter is replaced with the data being input to the device. See the Block Diagrams in Section 1 for a visual description of this loopback.

T3/E3 Diagnostic Loopback

The Diagnostic Loopback loops the outgoing T3/E3 data from the T3/E3 formatter back to receive side framer. When this loopback is enabled, the incoming receive data at HRCLK, HRPOS, and HRNEG is ignored. See the Block Diagrams in Section 1 for a visual description of this loopback. Please note that the device can still generate AIS at the HTCLK, HTPOS, and HTNEG outputs when this loopback is invoked. This is important to keep the data that is being looped back from disturbing downstream equipment.

T3/E3 Payload Loopback

The Payload Loopback loops the framed T3/E3 data from the receive side framer back to the transmit side formatter. When this loopback is enabled, the incoming receive data continues to pass through the device but the data normally being input to the T3/E3 formatter is ignored. See the Block Diagrams in Section 1 for a visual description of this loopback.

5.2 T3 / E3 FRAMER CONTROL REGISTER DESCRIPTION

Register Name: **T3E3CR**
Register Description: **T3/E3 Control Register**
Register Address: **10h**

Bit #	7	6	5	4	3	2	1	0
Name	DLB	LLB	T3IDLE	E3SnC1	E3SnC0	TPT	TRAI	TAIS
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	PLB	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
Default	-	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / T3/E3 Transmit Alarm Indication Signal (TAIS). When this bit is set high in the T3 Mode, the transmitter will generate a properly F-Bit and M-Bit framed 101010... data pattern with both X Bits set to one, all C bits set to zero, and the proper P Bits. This is true regardless of whether the device is in the C-Bit Parity Mode or not. When this bit is set high in the E3 Mode, the transmitter will generate an unframed all ones. When this bit it set low, normal data is transmitted.

0 = do not transmit AIS
1 = transmit AIS

Bit 1 / T3/E3 Transmit Remote Alarm Indication (TRAI). When this bit is set high in the T3 Mode, both X Bits will be set to a zero. When this bit is set high in the E3 Mode, the RAI bit (bit number 11 of each E3 frame) will be set to a one. When this bit it set low in the T3 Mode, both X Bits will be set to one. When this bit is set low in the E3 Mode, the RAI bit will be set to a zero.

0 = do not transmit RAI
1 = transmit RAI

Bit 2 / T3/E3 Transmit Pass Through Enable (TPT).

0 = enable the framer to insert framing and overhead bits
1 = framer will not insert any framing or overhead bits

Bits 3 and 4 / E3 National Bit Control Bits 0 and 1 (E3SnC0 and E3SnC1). These bits determine where the E3 National bit is sourced from. On the receive side, the Sn bit is always routed to the T3E3INFO Register as well as the HDLC controller and the FEAC controller. These bits are ignored in the T3 Mode.

E3SnC1	E3SnC0	Source of the E3 National Bit (Sn)
0	0	force the Sn bit to one
0	1	use the HDLC controller to source the Sn bit
1	0	use the FEAC controller to source the Sn bit
1	1	force the Sn bit to zero

Bit 5 / Transmit T3 Idle Signal Enable (T3IDLE). When this bit is set high, the T3 Idle Signal will be transmitted instead of the normal transmit data. The T3 Idle Signal is defined as a normally T3 framed pattern (i.e. with the proper F Bits and M Bits along with the proper P Bits) where the information bit fields are completely filled with a data pattern of ...1100... and the C Bits in Subframe 3 are set to zero and both X bits are set to one. This bit is ignored in the E3 Mode.

0 = transmit data normally
1 = transmit T3 Idle Signal

Bit 6 / T3/E3 Line Loopback Enable (LLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 7 / T3/E3 Diagnostic Loopback Enable (DLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Bit 8 / E3 Code Violation Enable (E3CVE). This bit is ignored in the T3 Mode. This bit is used in the E3 mode to configure the BiPolar Violation Count Register (BPVCR) to count either BiPolar Violations (BPV) or Code Violations (CV). A BPV is defined as consecutive pulses (or marks) of the same polarity that are not part of a HDB3 code word. A CV is defined in ITU O.161 as consecutive BPVs of the same polarity.

0 = count BPV
1 = count CV

Bits 9 and 10 / T3/E3 Frame Error Counting Control Bits 0 and 1 (FECC0 and FECC1).

FECC1	FECC0	Frame Error Count Register (Fecr) Configuration
0	0	**T3 Mode:** count Loss Of Frame (LOF) Occurrences **E3 Mode:** count Loss Of Frame (LOF) Occurrences
0	1	**T3 Mode:** count both F bit and M bit errors **E3 Mode:** count bit errors in the FAS word
1	0	**T3 Mode:** count only F bit errors **E3 Mode:** count word errors in the FAS word
1	1	**T3 Mode:** count only M bit errors **E3 Mode:** illegal state

Bit 11 / Error Counting Control (ECC). This bit is used to control whether the device will increment the error counters during Loss Of Frame (LOF) conditions. It only affects the error counters that count errors that are based on framed information and these include the following:

- Frame Error Counter (when it is configured to count frame errors, not LOF occurrences)
- T3 Parity Bit Error Counter
- T3 C-Bit Parity Error Counter
- T3 Far End Block Error or E3 RAI Counter.

When this bit is set low, these error counters will not be allowed to increment during LOF conditions. When this bit is set high, these error counters will be allowed to increment during LOF conditions.

0 = stop the FECR/PCR/CPCR/FEBECR error counters from incrementing during LOF
1 = allow the FECR/PCR/CPCR/FEBECR error counters to increment during LOF

Bit 12 / Automatic FEBE Defeat (AFEBED). This bit is ignored in the E3 Mode and in the T3 Mode when the device is not configured in the C-Bit Parity Mode. When this bit is low, the device will automatically insert the FEBE codes into the transmitted data stream by setting all three C Bits in Subframe 4 to zero.

0 = automatically insert FEBE codes in the transmit data stream based on detected errors
1 = use the TFEBE control to determine the state of the FEBE codes

Bit 13 / Transmit FEBE Setting (TFEBE). This bit is only active when AFEBED is active (i.e. AFEBED = 1). When this bit is low, the device will force the FEBE code to 111 continuously. When this bit is set high, the device will force the FEBE code to 000 continuously.

0 = force FEBE to 111 (null state)
1 = force FEBE to 000 (active state)

Bit 14 / T3/E3 Payload Loopback Enable (PLB). See Figures 1A and 1B for a visual description of this loopback.

0 = disable loopback
1 = enable loopback

Register Name: **T3E3EIC**
Register Description: **T3/E3 Error Insert Control Register**
Register Address: **18h**

Bit #	7	6	5	4	3	2	1	0
Name	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / BiPolar Violation Insert (BPVI). A 0 to 1 transition on this bit will cause a single BPV to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no affect when the T3/E3 interface is in the Unipolar Mode (see Section 4.2 for details about the Unipolar Mode). In the Manual Error Insert mode (MEIMS = 1), errors will be inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors will be inserted.

Bit 1 / EXcessive Zero Insert (EXZI). A 0 to 1 transition on this bit will cause a single EXZ event to be inserted into the transmit data stream. An EXZ event is defined as three or more consecutive zeros in the T3 Mode and four or more consecutive zeros in the E3 Mode. Once this bit has been toggled from a 0 to a 1, the device waits for the next possible B3ZS/HDB3 code word insertion and it suppresses that code word from being inserted and hence this creates the EXZ event. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no affect when the T3/E3 interface is in the Unipolar Mode (see Section 4.2 for details about the Unipolar Mode). In the Manual Error Insert mode (MEIMS = 1), errors will be inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors will be inserted.

Bit 2 / T3 Parity Bit Error Insert (T3PBEI). A 0 to 1 transition on this bit will cause a single T3 Parity error event to be inserted into the transmit data stream. A T3 Parity event is defined as flipping the proper polarity of both the P Bits in a T3 Frame (see Section 15.2 for details about the P Bits). Once this bit has been toggled from a 0 to a 1, the device waits for the next T3 frame to flip both P Bits. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no affect when the device is operated in the E3 Mode. In the Manual Error Insert mode (MEIMS = 1), errors will be inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors will be inserted.

Bit 3 / T3 C-Bit Parity Error Insert (T3CPBEI). A 0 to 1 transition on this bit will cause a single T3 C-Bit Parity error event to be inserted into the transmit data stream. A T3 Parity event is defined as flipping the proper polarity of all three CP Bits in a T3 Frame (see Section 15.2 for details about the CP Bits). Once this bit has been toggled from a 0 to a 1, the device waits for the next T3 frame to flip the three CP Bits. This bit must be cleared and set again for a subsequent error to be inserted. Toggling this bit has no affect when the T3 framer is not operated in the C-Bit Parity Mode (see Section 4.2 for details about the C-Bit Parity Mode) or when the device is operated in the E3 Mode. In the Manual Error Insert mode (MEIMS = 1), errors will be inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors will be inserted.

Bit 4 / Frame Bit Error Insert (FBEI). A 0 to 1 transition on this bit will cause the transmit framer to generate framing bit errors. The type of framing bit errors inserted is controlled by the FBEIC0 and FBEIC1 bits (see discussion below). Once this bit has been toggled from a 0 to a 1, the device waits for the next possible framing bit to insert the errors. This bit must be cleared and set again for a subsequent error to be inserted. In the Manual Error Insert mode (MEIMS = 1), errors will be inserted on each toggle of the FTMEI input signal as long as this bit is set high. When this bit is set low, no errors will be inserted.

Bits 5 and 6 / Frame Bit Error Insert Control Bits 0 and 1 (FBEIC0 and FBEIC1).

FBEIC1	FBEIC0	Type Of Framing Bit Error Inserted
0	0	**T3 Mode:** a single F-Bit error **E3 Mode:** a single FAS word of 1111000000 is generated instead of the normal FAS word which is 1111010000 (i.e. only 1 bit inverted)
0	1	**T3 Mode:** a single M-Bit error **E3 Mode:** a single FAS word of 0000101111 is generated instead of the normal FAS word which is 1111010000 (i.e. all FAS bits are inverted)
1	0	**T3 Mode:** 4 consecutive F-Bit errors (causes the far end to lose synchronization) **E3 Mode:** 4 consecutive FAS words of 1111000000 are generated instead of the normal FAS word which is 1111010000 (i.e. only 1 bit inverted; causes the far end to lose synchronization)
1	1	**T3 Mode:** 3 consecutive M-Bit errors (causes the far end to lose synchronization) **E3 Mode:** 4 consecutive FAS words of 0000101111 are generated instead of the normal FAS word which is 1111010000 (i.e. all FAS bits are inverted; causes the far end to lose synchronization)

Bit 7 / Manual Error Insert Mode Select (MEIMS). When this bit is set low, the device will insert errors on each 0 to 1 transition of the BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bits. When this bit is set high, the device will insert errors on each 0 to 1 transition of the FTMEI input signal. The appropriate BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bit must be set to one for this to occur. If all of the BPVI, EXZI, T3PBEI, T3CPBEI, and FBEI control bits are set to zero, no errors are inserted.

0 = use 0 to 1 transition on the BPVI, EXZI, T3PBEI, T3CPBEI, or FBEI control bits to insert errors
1 = use 0 to 1 transition on the FTMEI input signal to insert errors

5.3 T3 / E3 FRAMER STATUS and INTERRUPT REGISTER DESCRIPTION

Register Name: **T3E3SR**
Register Description: **T3/E3 Status Register**
Register Address: **12h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	RSOF	TSOF	T3IDLE	RAI	AIS	LOF	LOS
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Default	-	-	-	-	-	-	-	-

Note: See Figure 5.3A for details on the signal flow for the status bits in the T3E3SR register.
Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Loss Of Signal Occurrence (LOS). This latched read only alarm status bit will be set to a one when the T3 or E3 framer detects a loss of signal. This bit will be cleared when read unless a LOS condition still exists. A change in state of the LOS can cause a hardware interrupt to occur if the LOS bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. The LOS alarm criteria is described in Tables 5.3A and 5.3B

Bit 1 / Loss Of Frame Occurrence (LOF). This latched read only alarm status bit will be set to a one when the T3 or E3 framer detects a loss of frame. This bit will be cleared when read unless a LOF condition still exists. A change in state of the LOF can cause a hardware interrupt to occur if the LOF bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. The LOF alarm criteria is described in Tables 5.3A and 5.3B

Bit 2 / Alarm Indication Signal Detected (AIS). This latched read only alarm status bit will be set to a one when the T3 or E3 framer detects an incoming Alarm Indication Signal. This bit will be cleared when read unless an AIS signal is still present. A change in state of the AIS detection can cause a hardware interrupt to occur if the AIS bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. The AIS alarm detection criteria is described in Tables 5.3A and 5.3B

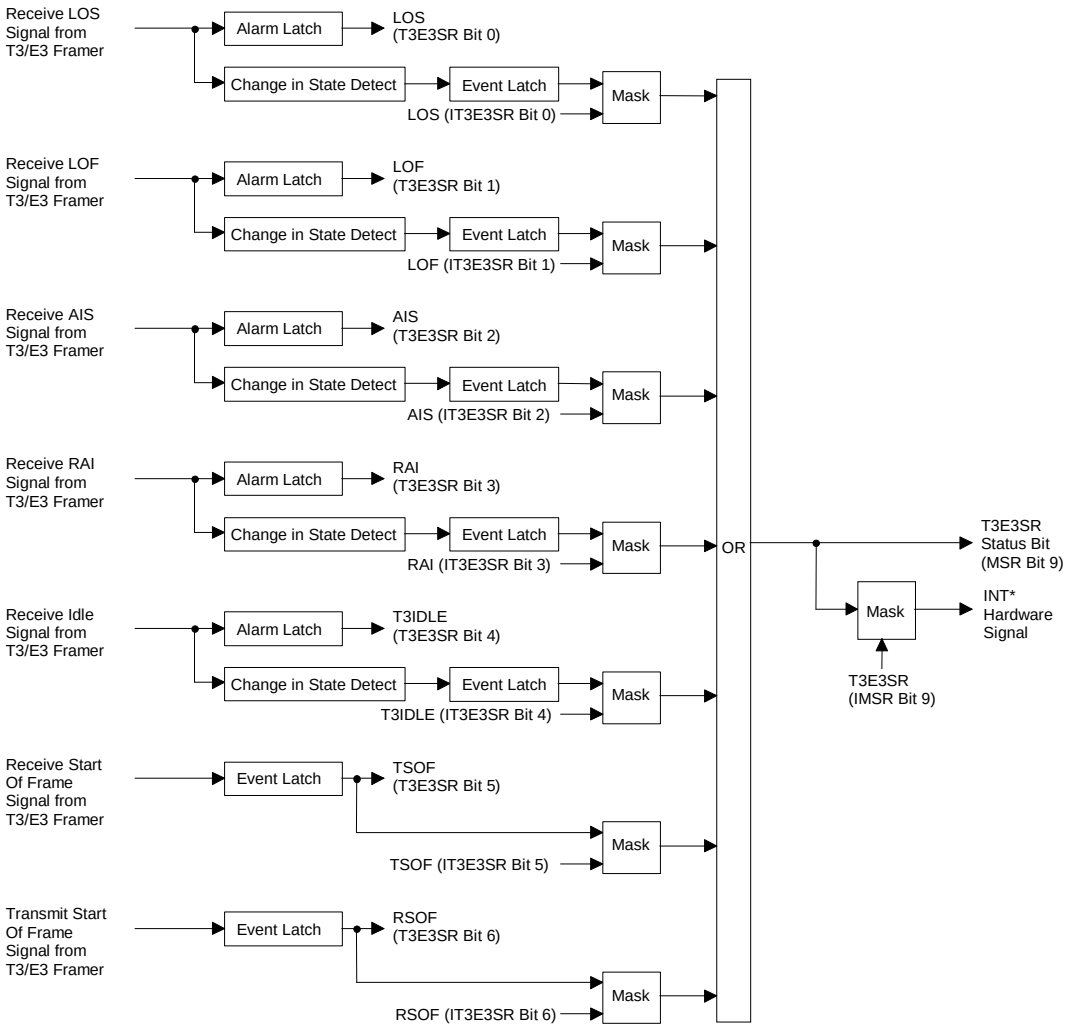
Bit 3 / Remote Alarm Indication Detected (RAI). This latched read only alarm status bit will be set to a one when the T3 or E3 framer detects an incoming Remote Alarm Indication (RAI) signal. This bit will be cleared when read unless an RAI signal is still present. A change in state of the RAI detection can cause a hardware interrupt to occur if the RAI bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. The RAI alarm detection criteria is described in Tables 5.3A and 5.3B. RAI can also be indicated via the FEAC codes when the device is operated in the C-Bit Parity Mode.

Bit 4 / T3 Idle Signal Detected (T3IDLE). This latched read only alarm status bit will be set to a one when the T3 framer detects an incoming idle signal. This bit will be cleared when read unless the idle signal is still present. A change in state of idle detection can cause a hardware interrupt to occur if the IDLE bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The IDLE detection criteria is described in Table 5.3A. The interrupt will be allowed to clear when this bit is read. When the DS3112 is operated in the E3 mode, this status bit should be ignored.

Bit 5 / Transmit T3/E3 Start Of Frame (TSOF). This latched read only event status bit will be set to a one on each T3/E3 transmit frame boundary. This bit is a software version of the FTSOF hardware signal and it will be cleared when read. The setting of this bit can cause a hardware interrupt to occur if the TSOF bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one.

Bit 6 / Receive T3/E3 Start Of Frame (RSOF). This latched read only event status bit will be set to a one on each T3/E3 receive frame boundary. This bit is a software version of the FRSOF hardware signal and it will be cleared when read. The setting of this bit can cause a hardware interrupt to occur if the RSOF bit in the Interrupt Mask for T3E3SR (IT3E3SR) register is set to a one and the T3E3SR bit in the Interrupt Mask for MSR (IMSR) register is set to a one.

T3E3SR Status Bit Flow Figure 5.3A



Note: All event and alarm latches above are cleared when the T3E3SR register is read.

Register Name: **IT3E3SR**
Register Description: **Interrupt Mask for T3/E3 Status Register**
Register Address: **14h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	RSOF	TSOF	T3IDLE	RAI	AIS	LOF	LOS
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Loss Of Signal Occurrence (LOS).
0 = interrupt masked
1 = interrupt unmasked

Bit 1 / Loss Of Frame Occurrence (LOF).
0 = interrupt masked
1 = interrupt unmasked

Bit 2 / Alarm Indication Signal Detected (AIS).
0 = interrupt masked
1 = interrupt unmasked

Bit 3 / Remote Alarm Indication Detected (RAI).
0 = interrupt masked
1 = interrupt unmasked

Bit 4 / T3 Idle Signal Detected (T3IDLE).
0 = interrupt masked
1 = interrupt unmasked

Bit 5 / Transmit T3/E3 Start Of Frame (TSOF).
0 = interrupt masked
1 = interrupt unmasked

Bit 6 / Receive T3/E3 Start Of Frame (RSOF).
0 = interrupt masked
1 = interrupt unmasked

T3 Alarm Criteria Table 5.3A

Alarm/ Condition	Definition	Set Criteria	Clear Criteria
AIS	**Alarm Indication Signal** Properly framed 1010... pattern which is aligned with the 1 just after each overhead bit and all C Bits are set to zero	In each 84 bit information field, the properly aligned 10... pattern is detected with less than 4 bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms) and all C Bits are majority decoded to be zero during this time	In each 84 bit information field, the properly aligned 10... pattern is detected with 4 or more bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95ms)
LOS	**Loss Of Signal**	192 consecutive zeros	No EXZ events over a 192 bit window that starts with the first one received
LOF	**Loss Of Frame** Too many F Bits or M Bits in error	3 or more F bits in error out of 16 consecutive or 2 or more M bits in error out of 4 consecutive	Synchronization occurs
RAI (note: RAI can also be indicated via FEAC codes in the C-Bit Parity Mode)	**Remote Alarm Indication** (this is also referred to as SEF/AIS in Bellcore GR-820) X1 = X2 = 0 (active) X1 = X2 = 1 (inactive)	X1 and X2 = 0 for 4 consecutive M frames (426us)	X1 and X2 = 1 for 4 consecutive M frames (426us)
Idle Signal	Properly framed 1100... pattern which is aligned with the 11 just after each overhead bit and the C Bits in Subframe 3 are zero	In each 84 bit information field, the properly aligned 1100... pattern is detected with less than 4 bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95 ms) and the C Bits in Subframe 3 are majority decoded to be zero during this time	In each 84 bit information field, the properly aligned 1100... pattern is detected with 4 or more bit errors (out of 84 possible) for 1024 consecutive information bit fields (1.95 ms)

E3 Alarm Criteria Table 5.3B

Alarm/ Condition	Definition	Set Criteria	Clear Criteria
AIS	**Alarm Indication Signal** Unframed all ones	4 or less zeros in 2 consecutive 1536 bit frames	5 or more zeros in 2 consecutive 1536 bit frames
LOS	**Loss Of Signal**	192 consecutive zeros	No EXZ events over a 192 bit window that starts with the first one received
LOF	**Loss Of Frame** Too many FAS errors	4 consecutive bad FAS	3 consecutive good FAS
RAI	**Remote Alarm Indication** inactive: bit 11 of the frame = 0 active: bit 11 of the frame = 1	Bit 11 = 1 for 4 consecutive frames (6144 bits / 179 us)	Bit 11 = 0 for 4 consecutive frames (6144 bits / 179 us)

Register Name: **T3E3INFO**
Register Description: **T3/E3 Information Register**
Register Address: **16h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	SEFE	EXZ	MBE	FBE	ZSCD	COFA
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	RAIC	AISC	LOFC	LOSC	T3AIC	E3Sn
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.
Note: The status bits in the T3E3INFO cannot cause a hardware interrupt to occur.

Bit 0 / Change Of Frame Alignment Detected (COFA). This latched read only event status bit will be set to a one when the T3/E3 framer has experienced a Change Of Frame Alignment (COFA). A COFA occurs when the device achieves synchronization in a different alignment than it had previously. If the device has never acquired synchronization before, then this status bit is meaningless. This bit will be cleared when read and will not be set again until the framer has lost synchronization and reacquired synchronization in a different alignment.

Bit 1 / Zero Suppression Codeword Detected (ZSCD). This latched read only event status bit will be set to a one when the T3/E3 framer has detected a B3ZS/HDB3 codeword. This bit will be cleared when read and will not be set again until the framer has detected another B3ZS/HDB3 codeword.

Bit 2 / F Bit or FAS Error Detected (FBE). This latched read only status bit will be set to a one when the DS3112 has detected an error in either the F Bits (T3 mode) or the FAS word (E3 mode). This bit will be cleared when read and will not be set again until the device detects another error.

Bit 3 / M Bit Error Detected (MBE). This latched read only event status bit will be set to a one when the DS3112 has detected an error in the M Bits. This bit will be cleared when read and will not be set again until the device detects another error in one of the M Bits. This status bit has no meaning in the E3 mode and should be ignored.

Bit 4 / EXcessive Zeros Detected (EXZ). This latched read only event status bit will be set to a one each time the DS3112 has detected a consecutive string of either 3 or more zeros (T3 mode) or 4 or more zeros (E3 mode). This bit will be cleared when read and will not be set again until the device detects another EXcessive Zero event.

Bit 5 / Severely Errored Framing Event Detected (SEFE). This latched read only event status bit will be set to a one each time the DS3112 has detected either 3 or more F Bits in error out of 16 consecutive F Bits (T3 mode) or four bad FAS words in a row (E3 mode). This bit will be cleared when read and will not be set again until the device detects another SEFE event.

Bit 8 / E3 National Bit (E3Sn). This read only real time status bit reports the incoming E3 National Bit (Sn). It is loaded at the start of each E3 frame as the Sn bit is decoded. The Host can use the RSOF status bit in the T3/E3 Status Register (T3E3SR) to determine when to read this bit.

Bit 9 / T3 Application ID Channel Status (T3AIC). This read only real time status bit can be used to help determine whether an incoming T3 data stream is in C-Bit Parity mode or M23 mode. In C-Bit Parity mode, it is recommended that the first C Bit in each M Frame be set to one. In M23 mode, the first C Bit in each M frame should be toggling between 0 and 1 to indicate that the bits need to be stuffed or not. This bit will be set to a one when the device detects that the first C Bit in the M Frame is set to one for 1020 times or more out of 1024 consecutive M Frames (109ms). It will be allowed to be cleared when the device detects that the first C Bit is set to one less than 1020 times out of 1024 consecutive M Frames (109ms). This status bit has no meaning in the E3 mode and should be ignored.

Bit10 / Loss Of Signal Clear Detected (LOSC). This latched read only event status bit will be set to a one each time the T3/E3 framer exits a Loss Of Signal (LOS) state. This bit will be cleared when read and will not be set again until the device once again exits the LOS state. The LOS alarm criteria is described in Tables 5.3A and 5.3B. This status bit is useful in helping the Host determine if the LOS persists as defined in ANSI T1.231.

Bit11 / Loss Of Frame Clear Detected (LOFC). This latched read only event status bit will be set to a one each time the T3/E3 framer exits a Loss Of Frame (LOF) state. This bit will be cleared when read and will not be set again until the device once again exits the LOF state. The LOF alarm criteria is described in Tables 5.3A and 5.3B. This status bit is useful in helping the Host determine if the LOF persists as defined in ANSI T1.231.

Bit12 / Alarm Indication Signal Clear Detected (AISC). This latched read only event status bit will be set to a one each time the T3/E3 framer no longer detects the AIS alarm state. This bit will be cleared when read and will not be set again until the device once again exits the AIS alarm state. The AIS alarm criteria is described in Tables 5.3A and 5.3B. This status bit is useful in helping the Host determine if the AIS persists as defined in ANSI T1.231.

Bit13 / Remote Alarm Indication Clear Detected (RAIC). This latched read only event status bit will be set to a one each time the T3/E3 framer no longer detects the RAI alarm state. This bit will be cleared when read and will not be set again until the device once again exits the RAI alarm state. The RAI alarm criteria is described in Tables 5.3A and 5.3B. This status bit is useful in helping the Host determine if the RAI persists as defined in ANSI T1.231.

5.4 T3 / E3 PERFORMANCE ERROR COUNTERS

There are six error counters in the DS3112. All of the errors counters are 16 bits in length. The Host has three options as to how these errors counters are updated. The device can be configured to automatically update the counters once a second or manually via either an internal software bit (MECU) or an external signal (FRMECU). See Section 4.2 for details. All the error counters saturate when full and will not rollover.

Register Name: **BPVCR**
Register Description: **BiPolar Violation Count Register**
Register Address: **20h**

Bit #	7	6	5	4	3	2	1	0
Name	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit BiPolar Violation Counter (BPV0 to BPV15). These bits report the number of BiPolar Violations (BPV). In the E3 Mode, this counter can also be configured via the E3CVE bit in the T3E3 Control Register (see Section 5.2) to count Code Violations (CV). A BPV is defined as consecutive pulses (or marks) of the same polarity that are not part of a B3ZS/HDB3 code word. A CV is defined in ITU O.161 as consecutive BPVs of the same polarity.

Register Name: **EXZCR**
Register Description: **EXcessive Zero Count Register**
Register Address: **22h**

Bit #	7	6	5	4	3	2	1	0
Name	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit EXcessive Zero Counter (EXZ0 to EXZ15). These bits report the number of EXcessive Zero occurrences (EXZ). An EXZ occurrence is defined as three or more consecutive zeros in the T3 Mode and four or more consecutive zeros in the E3 Mode. As an example, a string of eight consecutive zeros would only increment this counter once.

Register Name: **FECR**
Register Description: **Frame Error Count Register**
Register Address: **24h**

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit Framing Bit Error Counter (FE0 to FE15). These bits report either the number of Loss Of Frame (LOF) occurrences or the number of framing bit errors received. The FECR is configured via the Host by the Frame Error Counting Control Bits (FECC0 and FECC1) in the T3E3 Control Register (see Section 5.2). The possible configurations are shown below.

FECC1	FECC0	Frame Error Count Register (FECR) Configuration
0	0	**T3 Mode:** count Loss Of Frame (LOF) Occurrences **E3 Mode:** count Loss Of Frame (LOF) Occurrences
0	1	**T3 Mode:** count both F bit and M bit errors **E3 Mode:** count bit errors in the FAS word
1	0	**T3 Mode:** count only F bit errors **E3 Mode:** count word errors in the FAS word
1	1	**T3 Mode:** count only M bit errors **E3 Mode:** illegal state

When the FECR is configured to count LOF occurrences, the FECR increments by one each time the device loses receive synchronization. When the FECR is configured to count framing bit errors, it can be configured via the ECC control bit in the T3/E3 Control Register (see Section 5.2) to either continue counting frame bit errors during a LOF or not.

Register Name: **PCR**
Register Description: **T3 Parity Bit Error Count Register**
Register Address: **26h**

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit T3 Parity Bit Error Counter (PE0 to PE15). These bits report the number of T3 Parity Bit errors. In the E3 Mode, this counter is meaningless and should be ignored. A Parity Bit error is defined as an occurrence when the two Parity Bits do not match one another or when the two Parity Bits do not match the parity calculation made on the information bits. Via the ECC control bit in the T3/E3 Control Register (see Section 5.2), the PCR can be configured to either continue counting parity bit errors during a LOF or not.

Register Name: **CPCR**
Register Description: **T3 C-Bit Parity Bit Error Count Register**
Register Address: **28h**

Bit #	7	6	5	4	3	2	1	0
Name	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit T3 C-Bit Parity Bit Error Counter (CPE0 to CPE15). These bits report the number of T3 C-Bit Parity Bit errors. When the device is not in the C-Bit parity Mode or when the device is in the E3 Mode, this counter is meaningless and should be ignored. A C-Bit Parity Bit error is defined as an occurrence when the majority decoded three CP Parity Bits do not match the parity calculation made on the information bits. Via the ECC control bit in the T3/E3 Control Register (see Section 5.2), the CPCR can be configured to either continue counting C-Bit parity bit errors during a LOF or not.

Register Name: **FEBECR**
Register Description: **T3 Far End Block Error or E3 RAI Count Register**
Register Address: **2Ah**

Bit #	7	6	5	4	3	2	1	0
Name	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / 16-Bit T3 Far End Block Error or E3 RAI Counter (FEBE0 to FEBE15). In the T3 C-Bit Parity Mode, these bits report the number of T3 Far End Block Errors (FEBE). This counter increments each time the three FEBE bits do not equal 111. In the E3 Mode, these bits report the number of times the RAI bit is received in the "disturbed state" (i.e. the number of times that it is set to a one). In the T3 mode, when the device is not in the C-Bit parity Mode, this counter is meaningless and should be ignored. Via the ECC control bit in the T3/E3 Control Register (see Section 5.2), the FEBECR can be configured to either continue counting FEBEs or active RAI bits during a LOF or not.

SECTION 6: M13 / E13 / G747 MULTIPLEXER AND T2 / E2 / G747 FRAMER

6.1 GENERAL DESCRIPTION

Note: If the DS3112 is used as a stand alone T3/E3 framer and the multiplexer functionality is disabled, then the registers and functionality described in this section are not applicable and should be ignored by the Host.

On the receive side, the T2/E2/G747 framer locates the frame boundaries of the incoming T2/E2/G747 datastream and monitors the datastream for alarms and errors. Alarms are detected and reported in T2/E2 Status Registers (T2E2SR1 and T2E2SR2) which are described in Section 6.3. The Host can force the T2/E2/G747 framer to resynchronize via the T2E2RSY control bit in the MRID register (see Section 4.1). On the transmit side, the device formats the outgoing datastream with the proper framing pattern and overhead and can generate alarms. It can also inject errors for diagnostic testing purposes. The transmit side of the framer is called the "formatter".

T1/E1 AIS Generation

The DS3112 can generate an Alarm Indication Signal (AIS) for the T1 and E1 datastreams in both the transmit and receive directions. AIS for T1 and E1 signals is defined as an unframed all ones pattern. On reset, the DS3112 will force AIS in both the transmit and receive directions on all 28 T1 and 16/21 E1 datastreams. It is the Host's task to configure the device to pass normal traffic via the T1E1RAIS1, T1E1RAIS2, T1E1TAIS1, and T1E1TAIS2 registers. See Section 6.4 for more details.

6.2 T2 / E2 / G747 FRAMER CONTROL REGISTER DESCRIPTION

Register Name: **T2E2CR1**
Register Description: **T2/E2 Control Register 1**
Register Address: **30h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	TRAI7	TRAI6	TRAI5	TRAI4	TRAI3	TRAI2	TRAI1
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	TAIS7	TAIS6	TAIS5	TAIS4	TAIS3	TAIS2	TAIS1
Default	-	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 6 / T2/E2/G747 Transmit Remote Alarm Indication (TRAIn where n = 1 to 7). When this bit is set high in the T3 Mode, the X Bit will be set to zero. When this bit is set high in the E3 Mode, the RAI bit (bit number 11 of each E2 frame) will be set to a one. In the E3 mode, TRAI5 to TRAI7 (bits 4 to 6) are disabled and should be set low by the Host. When this bit is set high in the G747 Mode, the RAI bit (bit number 1 of Set 2 in each G747 frame) will be set to a one. When this bit it set low in the T3 Mode, the X Bit will be set to a one. When this bit is set low in the E3 and G747 Modes, the RAI bit will be set to zero.

0 = do not transmit RAI
1 = transmit RAI

Bits 8 to 14 / T2/E2/G747 Transmit Alarm Indication Signal (TAISn where n = 1 to 7). When this bit is set high, the transmit formatter will generate an unframed all ones pattern. When this bit it set low, normal data is transmitted. In the E3 mode, TAIS5 to TAIS7 (bits 4 to 6) are disabled and should be set low by the Host.

0 = do not transmit AIS
1 = transmit AIS

Register Name: **T2E2CR2**
Register Description: **T2/E2 Control Register 2**
Register Address: **32h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	LOFG7	LOFG6	LOFG5	LOFG4	LOFG3	LOFG2	LOFG1
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	E2Sn4	E2Sn3	E2Sn2	E2Sn1
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 6 / T2/E2/G747 Transmit Loss Of Frame Generation (LOFGn where n = 1 to 7). A 0 to 1 transition on this bit will cause the T2/E2/G747 transmit formatter to generate enough framing bit errors to cause the far end to lose frame synchronization. This bit must be cleared and set again for a subsequent set of errors to be generated.

	Framing Errors Generated
T3 Mode	4 consecutive F Bit errors
E3 Mode	4 consecutive FAS words of 0000101111 generated instead of the normal FAS word which is 1111010000 (i.e. all FAS bits are inverted)
G747 Mode	4 consecutive FAS words of 000101111 generated instead of the normal FAS word which is 111010000 (i.e. all FAS bits are inverted)

Bits 8 to 11 / E2 Transmit National Bit Setting (E2Snn where n = 1 to 4). These bits are ignored in the T3 and G747 modes. The received Sn can be read from the T2E2 Status Register 2.

0 = force the Sn bit to zero
1 = force the Sn bit to one

6.3 T2 / E2 / G747 FRAMER STATUS AND INTERRUPT REGISTER DESCRIPTION

Register Name: **T2E2SR1**
Register Description: **T2/E2 Status Register 1**
Register Address: **34h**

Bit #	7	6	5	4	3	2	1	0
Name	IELOF	LOF7	LOF6	LOF5	LOF4	LOF3	LOF2	LOF1
Default	0	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	IEAIS	AIS7	AIS6	AIS5	AIS4	AIS3	AIS2	AIS1
Default	0	-	-	-	-	-	-	-

Note: See Figure 6.3A for details on the signal flow for the status bits in the T2E2SR1 register.
Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 6 / Loss Of Frame Occurrence (LOFn when n = 1 to 7). This latched read only alarm status bit will be set to a one each time the corresponding T2/E2/G747 framer detects a Loss Of Frame (LOF). This bit will be cleared when read unless a LOF condition still exists in that T2/E2/G747 framer. A change in state of the LOF in one or more of the T2/E2/G747 framers can cause the T2E2SR1 status bit (in the MSR register) to be set and a hardware interrupt to occur if the IELOF bit is set to a one and the T2E2SR1 bit in the Interrupt Mask for MSR (IMSR) register is set to a one. See Figure 6.3A. The interrupt will be allowed to clear when this bit is read. The LOF alarm criteria is described in Tables 6.3A, 6.3B and 6.3C. In the E3 Mode, LOF5 to LOF7 (bits 4 to 6) are meaningless and should be ignored.

Bit 7 / Interrupt Enable for Loss of Frame Occurrence (IELOF). This bit should be set to one if the Host wishes to have T2/E2/G747 LOF occurrences cause a hardware interrupt or the setting of the T2E2SR1 status bit in the MSR register. See Figure 6.3A. The T2E2SR1 bit in the Interrupt Mask for the Master Status Register (IMSR) must also be set to one for an interrupt to occur.

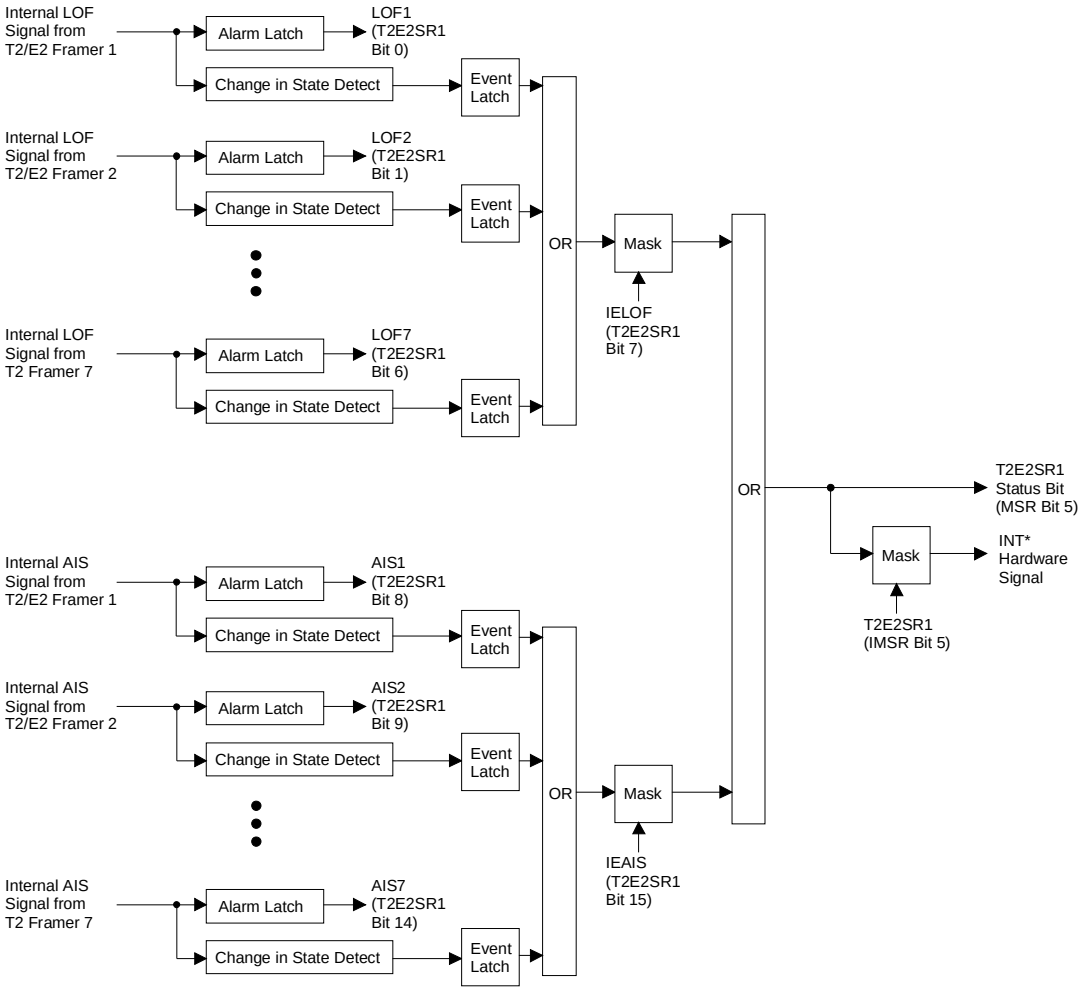
0 = interrupt masked
1 = interrupt unmasked

Bits 8 to 14 / Alarm Indication Signal Detected (AISn when n = 1 to 7). This latched read only alarm status bit will be set to a one each time the corresponding T2/E2/G747 framer detects an incoming AIS alarm. This bit will be cleared when read unless the AIS alarm still exists in that T2/E2/G747 framer. A change in state of the AIS detector in one or more of the T2/E2/G747 framers can cause the T2E2SR1 status bit (in the MSR register) to be set and a hardware interrupt to occur if the IEAIS bit is set to a one and the T2E2SR1 bit in the Interrupt Mask for MSR (IMSR) register is set to a one. See Figure 6.3A. The interrupt will be allowed to clear when this bit is read. The AIS alarm criteria is described in Tables 6.3A, 6.3B and 6.3C. In the E3 Mode, AIS5 to AIS7 (bits 4 to 6) are meaningless and should be ignored.

Bit 15 / Interrupt Enable for Alarm Indication Signal (IEAIS). This bit should be set to one if the Host wishes to have T2/E2/G747 AIS detection occurrences cause a hardware interrupt or the setting of the T2E2SR1 status bit in the MSR register. See Figure 6.3A. The T2E2SR1 bit in the Interrupt Mask for the Master Status Register (IMSR) must also be set to one for an interrupt to occur.

0 = interrupt masked
1 = interrupt unmasked

T2E2SR1 Status Bit Flow Figure 6.3A



Note: All event and alarm latches above are cleared when the T2E2SR1 register is read.

Register Name: **T2E2SR2**
Register Description: **T2/E2 Status Register 2**
Register Address: **36h**

Bit #	7	6	5	4	3	2	1	0
Name	IERAI	RAI7	RAI6	RAI5	RAI4	RAI3	RAI2	RAI1
Default	0	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	E2SOF4	E2SOF3	E2SOF2	E2SOF1	E2Sn4	E2Sn3	E2Sn2	E2Sn1
Default	-	-	-	-	-	-	-	-

Note: See Figure 6.3B for details on the signal flow for the status bits in the T2E2SR2 register.
Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 6 / Remote Alarm Indication Signal Detected (RAIn when n = 1 to 7). This latched read only alarm status bit will be set to a one each time the corresponding T2/E2/G747 framer detects an incoming RAI alarm. This bit will be cleared when read unless the RAI alarm still exists in that T2/E2/G747 framer. A change in state of the RAI in one or more of the T2/E2/G747 framers can cause the T2E2SR2 status bit (in the MSR register) to be set and a hardware interrupt to occur if the IERAI bit is set to a one and the T2E2SR2 bit in the Interrupt Mask for MSR (IMSR) register is set to a one. See Figure 6.3B. The interrupt will be allowed to clear when this bit is read. The RAI alarm criteria is described in Tables 6.3A, 6.3B and 6.3C. In the E3 Mode, RAI5 to RAI7 (bits 4 to 6) are meaningless and should be ignored.

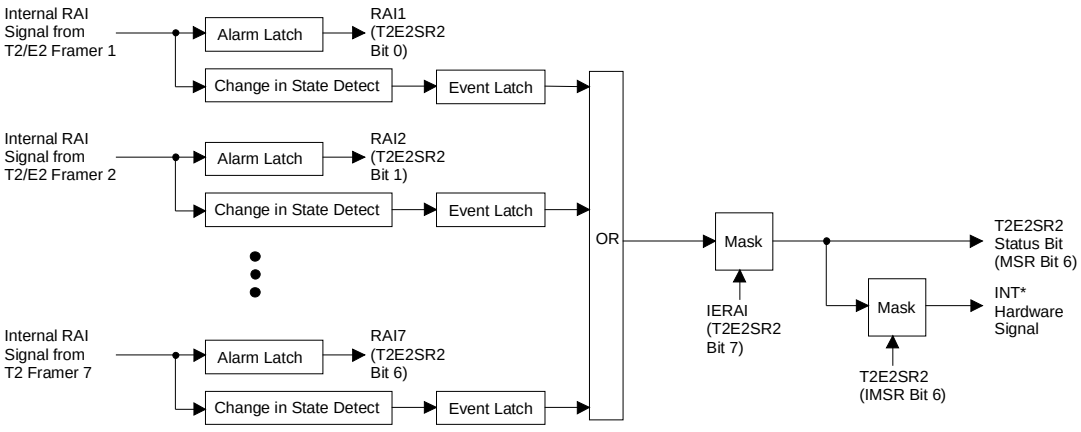
Bit 7 / Interrupt Enable for Remote Alarm Indication Signal (IERAI). This bit should be set to one if the Host wishes to have RAI detection occurrences cause a hardware interrupt or the setting of the T2E2SR2 status bit in the MSR register. See Figure 6.3B. The T2E2SR2 bit in the Interrupt Mask for the Master Status Register (IMSR) must also be set to one for an interrupt to occur.

0 = interrupt masked
1 = interrupt unmasked

Bits 8 to 11 / E2 Receive National Bit (E2Snn when n = 1 to 4). This read only real time status bit reports the incoming E2 National Bit (Sn). It is loaded at the start of each E2 frame as the Sn bit is decoded. The Host can use the E2SOF status bit to determine when to read this bit. In the T3 and G747 Modes, this bit is meaningless and should be ignored. This bit cannot cause an interrupt to occur.

Bits 12 to 15 / E2 Receive Start Of Frame (E2SOFn where n = 1 to 4). This latched read only event status bit will be set to a one on each E2 receive frame boundary. This bit will be cleared when read. The setting of this status bit cannot cause an interrupt to occur.

T2E2SR2 Status Bit Flow Figure 6.3B



Note: All event and alarm latches above are cleared when the T2E2SR2 register is read.

T2 Alarm Criteria Table 6.3A

Alarm/ Condition	Definition	Set Criteria	Clear Criteria
AIS	**Alarm Indication Signal** Unframed all ones	8 or less zeros in 4 consecutive M frames (4704 bits)	9 or more zeros in 4 consecutive M frames (4704 bits)
LOF	**Loss Of Frame** Too many F Bits or M Bits in error	2 or more F Bits in error out of 5 or 2 or more M Bits in error out of 4	Synchronization occurs
RAI	**Remote Alarm Indication** X = 0 (active) X = 1 (inactive)	X = 0 for 4 consecutive M frames (4704 bits)	X = 1 for 4 consecutive M frames (4704 bits)

E2 Alarm Criteria Table 6.3B

Alarm/ Condition	Definition	Set Criteria	Clear Criteria
AIS	**Alarm Indication Signal** Unframed all ones	4 or less zeros in each of 2 consecutive 848 bit frames	5 or more zeros in each of 2 consecutive 848 bit frames
LOF	**Loss Of Frame** Too many FAS errors	4 consecutive bad FAS	3 consecutive good FAS
RAI	**Remote Alarm Indication** inactive: bit 11 of the frame = 0 active: bit 11 of the frame = 1	Bit 11 = 1 for 4 consecutive frames (3392 bits)	Bit 11 = 0 for 4 consecutive frames (3392 bits)

G747 Alarm Criteria Table 6.3C

Alarm/ Condition	Definition	Set Criteria	Clear Criteria
AIS	**Alarm Indication Signal** Unframed all ones	4 or less zeros in each of 2 consecutive 840 bit frames	5 or more zeros in each of 2 consecutive 840 bit frames
LOF	**Loss Of Frame** Too many FAS errors	4 consecutive bad FAS	3 consecutive good FAS
RAI	**Remote Alarm Indication** inactive: bit 1 of Set 2 = 0 active: bit 1 of Set 2 = 1	Bit 1 of Set 2 = 1 for 4 consecutive frames (3360 bits)	Bit 1 of Set 2 = 0 for 4 consecutive frames (3360 bits)

6.4 T1 / E1 AIS GENERATION CONTROL REGISTER DESCRIPTION

Via the T1/E1 Alarm Indication Signal (AIS) Control Registers, the Host can configure the DS3112 to generate an unframed all ones signal in either the transmit or receive paths on the 28 T1 ports or the 16/21 E1 ports. On reset, the device will force AIS in both the transmit and receive paths and it is up to the Host to modify the T1/E1 AIS Generation Control Registers to allow normal T1/E1 traffic to traverse the DS3112. See the Block Diagrams in Section 1 for details on where the AIS signal is injected into the data flow. When the M13/E13 multiplexer function is disabled in the DS3112 (see the UNCHEN control bit in the Master Control Register 1 in Section 4.2 for details), the T1/E1 AIS Generation Control Registers are meaningless and can be set to any value.

Register Name: **T1E1RAIS1**
Register Description: **T1/E1 Receive Path AIS Generation Control Register 1**
Register Address: **40h**

Bit #	7	6	5	4	3	2	1	0
Name	AIS8	AIS7	AIS6	AIS5	AIS4	AIS3	AIS2	AIS1
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	AIS16	AIS15	AIS14	AIS13	AIS12	AIS11	AIS10	AIS9
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / Receive AIS Generation Control for T1/E1 Ports 1 to 16 (AIS1 to AIS2). These bits determine whether the device will replace the demultiplexed T1/E1 datastream with an unframed all ones AIS signal. AIS1 controls the data at LRDAT1, AIS2 controls the data at LRDAT2, and so on. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the AIS4, AIS8, AIS12, and AIS16 bits have no affect in the G747 Mode.

0 = send AIS to the LRDAT output
1 = send normal data to the LRDAT output

Register Name: **T1E1RAIS2**
Register Description: **T1/E1 Receive Path AIS Generation Control Register 2**
Register Address: **42h**

Bit #	7	6	5	4	3	2	1	0
Name	AIS24	AIS23	AIS22	AIS21	AIS20	AIS19	AIS18	AIS17
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	AIS28	AIS27	AIS26	AIS25
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 11 / Receive AIS Generation Control for T1 Ports 17 to 28 (AIS17 to AIS28). These bits determine whether the device will replace the demultiplexed T1/E1 datastream with an unframed all ones AIS signal. AIS17 controls the data at LRDAT17, AIS18 controls the data at LRDAT18, and so on. Since ports 17 to 28 are not active in the E3 Mode, these bits have no affect in the E3 Mode. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the AIS20, AIS24 and AIS28 bits have no affect in the G747 Mode.

0 = send AIS to the LRDAT output
1 = send normal data to the LRDAT output

Register Name: **T1E1TAIS1**
Register Description: **T1/E1 Transmit Path AIS Generation Control Register 1**
Register Address: **44h**

Bit #	7	6	5	4	3	2	1	0
Name	AIS8	AIS7	AIS6	AIS5	AIS4	AIS3	AIS2	AIS1
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	AIS16	AIS15	AIS14	AIS13	AIS12	AIS11	AIS10	AIS9
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / Transmit AIS Generation Control for T1/E1 Ports 1 to 16 (AIS1 to AIS2). These bits determine whether the device will replace the data input from the 28 T1 datastreams or 16/21 E1 datastreams with an unframed all ones AIS signal. AIS1 controls the data from LTDAT1, AIS2 controls the data from LTDAT2, and so on. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the AIS4, AIS8, AIS12 and AIS16 bits have no affect in the G747 Mode.

0 = replace data from LTDAT with AIS
1 = allow normal data from LTDAT to flow through to the multiplexer

Register Name: **T1E1TAIS2**
Register Description: **T1/E1 Transmit Path AIS Generation Control Register 2**
Register Address: **46h**

Bit #	7	6	5	4	3	2	1	0
Name	AIS24	AIS23	AIS22	AIS21	AIS20	AIS19	AIS18	AIS17
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	AIS28	AIS27	AIS26	AIS25
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 11 / Transmit AIS Generation Control for T1 Ports 17 to 28 (AIS17 to AIS28). These bits determine whether the device will replace the data input from the 28 T1 datastreams or 16/21 E1 datastreams with an unframed all ones AIS signal. AIS17 controls the data from LTDAT17, AIS18 controls the data from LTDAT18, and so on. Since ports 17 to 28 are not active in the E3 Mode, these bits have no affect in the E3 Mode. Since ports 22 to 28 are not active in the G747 Mode, these bits have no affect in the G747 Mode. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the AIS20, AIS24 and AIS28 bits have no affect in the G747 Mode.

0 = replace data from LTDAT with AIS
1 = allow normal data from LTDAT to flow through to the multiplexer

SECTION 7: T1 / E1 LOOPBACK AND DROP AND INSERT FUNCTIONALITY

7.1 GENERAL DESCRIPTION

On the T1 and E1 ports, the DS3112 has loopback capability in both directions. There is a per port Line Loopback which loops the receive side back to the transmit side and a per port Diagnostic Loopback which loops the transmit side back to the receive side. In addition, the device can detect the T1 Line Loopback Command as well as generate it. Also, the DS3112 has two Drop and Insert Ports which allow any two of the 28 T1 or 16/21 E1 datastreams to be dropped or inserted from two auxiliary ports. All of these functions are described below.

T1/E1 Line Loopback

Each of the 28 T1 or 16/21 E1 receive demultiplexed ports can be looped back to the transmit side. This loopback is called a Line Loopback and is shown in the Block Diagrams in Section 1. When the Line Loopback is invoked, the normal transmit data input at the LTCLK and LTDAT inputs is ignored and replaced with the data from the associated receive port. The Line Loopback is invoked by the Host via the T1E1LLB1 and T1E1LLB2 control registers (see Section 7.2).

T1/E1 Diagnostic Loopback

Each of the 28 T1 or 16/21 E1 transmit multiplexed ports can be looped back to the receive side. This loopback is called a Diagnostic Loopback and is shown in the Block Diagrams in Section 1. When the Diagnostic Loopback is invoked, the normal receive data output at the LRCLK and LRDAT outputs is replaced with the data from the associated transmit port. The Diagnostic Loopback is invoked by the Host via the T1E1DLB1 and T1E1DLB2 control registers (see Section 7.2).

T1 Line Loopback Command

M13 systems have the ability to request that a T1 line be looped back. This is achieved by inverting the C3 bit. See Section 14.2 for details on M13 formats and operation. The DS3112 will detect when the C3 bit has been inverted and will indicate which T1 line is being requested to be placed into Line Loopback via the T1LBSR1 and T1LBSR2 registers (see Section 7.3). When the Host detects that the a T1 line is being requested to be placed into loopback, it should set the appropriate control bit in either the T1E1LLB1 or T1E1LLB2 register. The DS3112 can also generate a T1 Line Loopback Command by inverting the C3 bit. This is accomplished via the T1LBCR1 and L1LBCR2 registers (see Section 7.2). Please note that when E3 or G747 mode is enabled, the T1 Line Loopback Command functionality is not applicable.

T1/E1 Drop and Insert

The DS3112 has the ability to drop any of the 28 T1 or 16/21 E1 receive channels to either one of two drop ports. The drop ports are Drop Port A and Drop Port B and they consist of the outputs LRCLKA/LRDATA and LRCLKB/LRDATB respectively. See the Block Diagrams in Section 1 for more details. The Host can determine which T1/E1 port should be dropped via the T1E1SDP control register (see Section 7.4). When a T1/E1 channel is dropped to either Drop Port A or B, the demultiplexed data is still output at the normal LRCLK and LRDAT outputs. On the transmit side, there are a complimentary pair of Insert Ports which are controlled via the T1E1SIP control register (see Section 7.4). When enabled, the inserted port data and clock (LTDATA/LTDATB and LTCLKA/LTCLKB respectively) replaces the data that would normally be multiplexed in at LTDAT and LTCLK inputs.

7.2 T1 / E1 LOOPBACK CONTROL REGISTER DESCRIPTION

Register Name: **T1E1LLB1**
Register Description: **T1/E1 Line Loopback Control Register 1**
Register Address: **50h**

Bit #	7	6	5	4	3	2	1	0
Name	LLB8	LLB7	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	LLB16	LLB15	LLB14	LLB13	LLB12	LLB11	LLB10	LLB9
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / T1/E1 Line Loopback Enable for Ports 1 to 16 (LLB1 to LLB16). These bits enable or disable the T1/E1 Line LoopBack (LLB). See the Block Diagrams in Section 1 for a visual description of this loopback. LLB1 corresponds to T1/E1 Port 1, LLB2 corresponds to T1/E1 Port 2, and so on. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the LLB4, LLB8, LLB12 and LLB16 bits have no affect in the G747 Mode.

0 = disable loopback
1 = enable loopback

Register Name: **T1E1LLB2**
Register Description: **T1/E1 Line Loopback Control Register 2**
Register Address: **52h**

Bit #	7	6	5	4	3	2	1	0
Name	LLB24	LLB23	LLB22	LLB21	LLB20	LLB19	LLB18	LLB17
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LLB28	LLB27	LLB26	LLB25
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 11 / T1 Line Loopback Enable for Ports 17 to 28 (LLB17 to LLB28). These bits enable or disable the T1 Line LoopBack (LLB). See the Block Diagrams in Section 1 for a visual description of this loopback. LLB1 corresponds to T17 Port 17, LLB18 corresponds to T1 Port 18, and so on. Since ports 17 to 28 are not active in the E3 Mode, these bits have no affect in the E3 Mode. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the LLB20, LLB24 and LLB28 bits have no affect in the G747 Mode.

0 = disable loopback
1 = enable loopback

Register Name: **T1E1DLB1**
Register Description: **T1/E1 Diagnostic Loopback Control Register 1**
Register Address: **54h**

Bit #	7	6	5	4	3	2	1	0
Name	DLB8	DLB7	DLB6	DLB5	DLB4	DLB3	DLB2	DLB1
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	DLB16	DLB15	DLB14	DLB13	DLB12	DLB11	DLB10	DLB9
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / T1/E1 Diagnostic Loopback Enable for Ports 1 to 16 (DLB1 to DLB16). These bits enable or disable the T1/E1 Diagnostic LoopBack (DLB). See the Block Diagrams in Section 1 for a visual description of this loopback. DLB1 corresponds to T1/E1 Port 1, DLB2 corresponds to T1/E1 Port 2, and so on. If the device is configured in Low Speed T1/E1 Port Loop Timed mode (if LLTM bit in the MC1 register is set to a one) then only data will be looped back - the clock will not be looped back. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the DLB4, DLB8, DLB12 and DLB16 bits have no affect in the G747 Mode.

0 = disable loopback
1 = enable loopback

Register Name: **T1E1DLB2**
Register Description: **T1/E1 Diagnostic Loopback Control Register 2**
Register Address: **56h**

Bit #	7	6	5	4	3	2	1	0
Name	DLB24	DLB23	DLB22	DLB21	DLB20	DLB19	DLB18	DLB17
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	DLB28	DLB27	DLB26	DLB25
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 17 to 28 / T1 Diagnostic Loopback Enable for Ports 17 to 28 (DLB17 to DLB28). These bits enable or disable the T1 Diagnostic LoopBack (DLB). See the Block Diagrams in Section 1 for a visual description of this loopback. DLB1 corresponds to T17 Port 17, DLB18 corresponds to T1 Port 18, and so on. Since ports 17 to 28 are not active in the E3 Mode, these bits have no affect in the E3 Mode. Since ports 4, 8, 12, 16, 20, 24, and 28 are not active in the G747 Mode, the DLB20, DLB24 and DLB28 bits have no affect in the G747 Mode. If the device is configured in Low Speed T1/E1 Port Loop Timed mode (if LLTM bit in the MC1 register is set to a one), then only data will be looped back, the clock will not be looped back.

0 = disable loopback
1 = enable loopback

Register Name: **T1LBCR1**
Register Description: **T1 Line Loopback Command Register 1**
Register Address: **58h**

Bit #	7	6	5	4	3	2	1	0
Name	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	LB16	LB15	LB14	LB13	LB12	LB11	LB10	LB9
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / T1 Line Loopback Far End Activate Command for Ports 1 to 16 (LB1 to LB16). These bits cause the appropriate T2 transmit formatter to generate a Line Loopback command for the far end. When this bit is set high, the T2 transmit formatter will force the C3 bit to be the inverse of the C1 and C2 bits. The T2 transmit formatter will continue to force the C3 bit to be the inverse of the C1 and C2 bits as long as this bit is held high. When this bit is set low, C3 will match the C1 and C2 bits. LB1 corresponds to T1/E1 Port 1, LB2 corresponds to T1/E1 Port 2, and so on. These bits are meaningless in the E3 and G747 modes and should be set to 0.

0 = do not generate the line loopback command by inverting the C3 bit
1 = generate the line loopback command by inverting the C3 bit

Register Name: **T1LBCR2**
Register Description: **T1 Line Loopback Command Register 2**
Register Address: **5Ah**

Bit #	7	6	5	4	3	2	1	0
Name	LB24	LB23	LB22	LB21	LB20	LB19	LB18	LB17
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LB28	LB27	LB26	LB25
Default	-	-	-	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 17 to 28 / T1 Line Loopback Far End Activate Command for Ports 17 to 28 (LB17 to LB28). These bits cause the appropriate T2 transmit formatter to generate a Line Loopback command for the far end. When this bit is set high, the T2 transmit formatter will force the C3 bit to be the inverse of the C1 and C2 bits. The T2 transmit formatter will continue to force the C3 bit to be the inverse of the C1 and C2 bits as long as this bit is held high. When this bit is set low, C3 will match the C1 and C2 bits. LB17 corresponds to T1/E1 Port 17, L18 corresponds to T1/E1 Port 18, and so on. These bits are meaningless in the E3 and G747 modes and should be set to 0.

0 = do not generate the line loopback command by inverting the C3 bit
1 = generate the line loopback command by inverting the C3 bit

7.3 T1 LINE LOOPBACK COMMAND STATUS REGISTER DESCRIPTION

Register Name: **T1LBSR1**
Register Description: **T1 Line Loopback Command Status Register 1**
Register Address: **5Ch**

Bit #	7	6	5	4	3	2	1	0
Name	LLB8	LLB7	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	LLB16	LLB15	LLB14	LLB13	LLB12	LLB11	LLB10	LLB9
Default	-	-	-	-	-	-	-	-

Note: See Figure 7.3A for details on the signal flow for the status bits in the T1LBSR1 and T1LBSR2 registers.
Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / T1 Line Loopback Command Status for Ports 1 to 16 (LLB1 to LLB16). These read only real time status bits will be set to a one when the corresponding T2 framer detects that the C3 bit is the inverse of the C1 and C2 bits for 5 consecutive frames. These bits will be allowed to clear when the C3 bit is not the inverse of the C1 and C2 bits for 5 consecutive frames. LLB1 corresponds to T1/E1 Port 1, LLB2 corresponds to T1/E1 Port 2, and so on. The setting of any of the bits in T1LBSR1 or T1LBSR2 can cause a hardware interrupt to occur if the T1LB bit in the Interrupt Mask for MSR (IMSR) is set to a one. In the E3 and G747 Modes, these bits are meaningless and should be ignored.

Register Name: **T1LBSR2**
Register Description: **T1 Line Loopback Command Status Register 2**
Register Address: **5Eh**

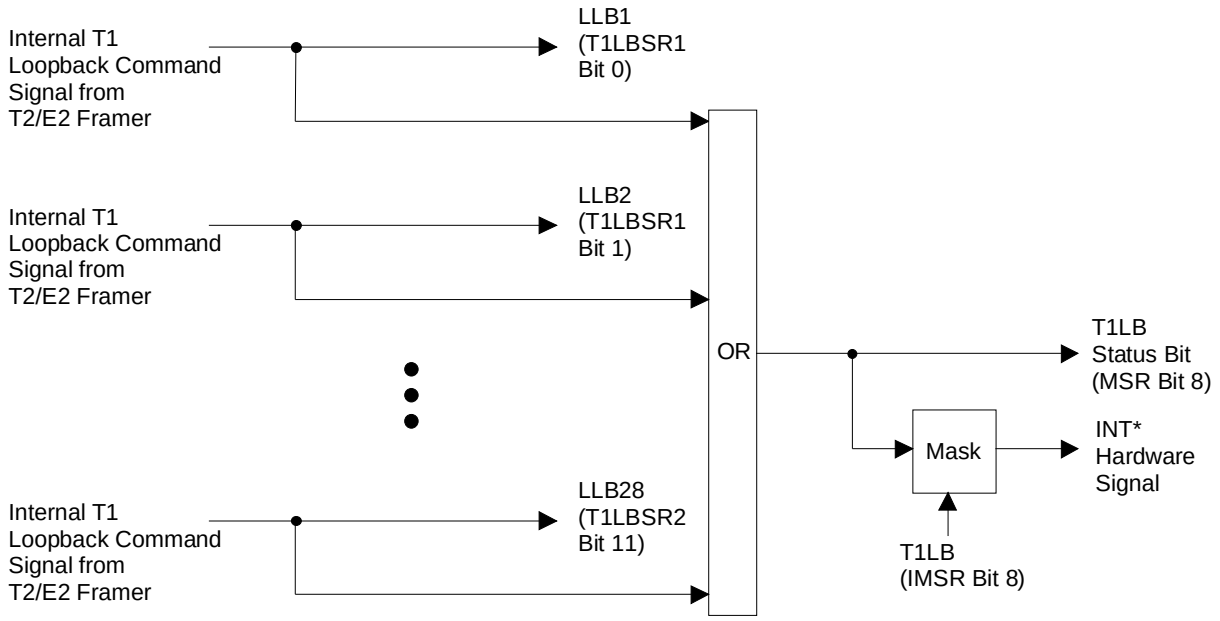
Bit #	7	6	5	4	3	2	1	0
Name	LLB24	LLB23	LLB22	LLB21	LLB20	LLB19	LLB18	LLB17
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	LLB28	LLB27	LLB26	LLB25
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 11 / T1 Line Loopback Command Status for Ports 17 to 28 (LLB17 to LLB28). These read only real time status bits will be set to a one when the corresponding T2 framer detects that the C3 bit is the inverse of the C1 and C2 bits for 5 consecutive frames. These bits will be allowed to clear when the C3 bit is not the inverse of the C1 and C2 bits for 5 consecutive frames. LLB17 corresponds to T1/E1 Port 17, LLB18 corresponds to T1/E1 Port 18, and so on. The setting of any of the bits in T1LBSR1 or T1LBSR2 can cause a hardware interrupt to occur if the T1LB bit in the Interrupt Mask for MSR (IMSR) is set to a one. In the E3 and G747 Modes, these bits are meaningless and should be ignored.

T1LBSR1 and T1LBSR2 Status Bit Flow Figure 7.3A



7.4 T1 / E1 DROP AND INSERT CONTROL REGISTER DESCRIPTION

Register Name: **T1E1SDP**
Register Description: **T1/E1 Select Register for Receive Drop Ports A and B**
Register Address: **60h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	n/a	DPAS4	DPAS3	DPAS2	DPAS1	DPAS0
Default	-	-	-	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	DPBS4	DPBS3	DPBS2	DPBS1	DPBS0
Default	-	-	-	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 4 / T1/E1 Drop Port A Select Bits (DPAS0 to DPAS4).
Bits 8 to 12 / T1/E1 Drop Port B Select Bits (DPBS0 to DPBS4).
These bits select which of the 28 T1 ports or 16 E1 ports (if any) should be output at either Drop Port A or Drop Port B. If no port is selected, the LRDATA, LRCLKA, LRDATB, and LRCLKB output pins will be forced low.

DPxS4:0

00000	no port	01000	Port 8	10000	Port 16	11000	Port 24
00001	Port 1	01001	Port 9	10001	Port 17	11001	Port 25
00010	Port 2	01010	Port 10	10010	Port 18	11010	Port 26
00011	Port 3	01011	Port 11	10011	Port 19	11011	Port 27
00100	Port 4	01100	Port 12	10100	Port 20	11100	Port 28
00101	Port 5	01101	Port 13	10101	Port 21	11101	no port
00110	Port 6	01110	Port 14	10110	Port 22	11110	no port
00111	Port 7	01111	Port 15	10111	Port 23	11111	no port

Register Name: **T1E1SIP**
Register Description: **T1/E1 Select Register for Transmit Insert Ports A and B**
Register Address: **62h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	n/a	IPAS4	IPAS3	IPAS2	IPAS1	IPAS0
Default	-	-	-	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	IPBS4	IPBS3	IPBS2	IPBS1	IPBS0
Default	-	-	-	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 4 / T1/E1 Insert Port A Select Bits (IPAS0 to IPAS4).
Bits 8 to 12 / T1/E1 Insert Port B Select Bits (IPBS0 to IPBS4).
These bits select if clock and data from either of the two insert ports (Insert Port A or Insert Port B) should replace the clock and data presented at one of the 28 T1 ports or 16/21 E1 ports. If no port is selected, the clock and data presented at the LTDATA, LTCLKA, LTDATB, and LTCLKB input pins is ignored. The same port should not be selected for both Insert Port A and Insert Port B.

IPxS4:0

00000	no port	01000	Port 8	10000	Port 16	11000	Port 24
00001	Port 1	01001	Port 9	10001	Port 17	11001	Port 25
00010	Port 2	01010	Port 10	10010	Port 18	11010	Port 26
00011	Port 3	01011	Port 11	10011	Port 19	11011	Port 27
00100	Port 4	01100	Port 12	10100	Port 20	11100	Port 28
00101	Port 5	01101	Port 13	10101	Port 21	11101	no port
00110	Port 6	01110	Port 14	10110	Port 22	11110	no port
00111	Port 7	01111	Port 15	10111	Port 23	11111	no port

SECTION 8: BERT

8.1 GENERAL DESCRIPTION

The BERT Block is capable of generating and detecting the following patterns:

- the pseudorandom patterns 2^7 – 1, 2^11 – 1 , 2^15 – 1 , and QRSS
- a repetitive pattern from 1 to 32 bits in length
- alternating (16-bit) words which flip every 1 to 256 words

The BERT receiver has a 32-bit Bit Counter and a 24-bit Error Counter. It can generate interrupts on detecting a bit error, a change in synchronization, or if an overflow occurs in the Bit and Error Counters. See Section 8.2 for details on status bits and interrupts from the BERT Block. To activate the BERT Block, the Host must configure the BERT mux via the BERT Mux Control register (see Section 8.2). Data can be routed to the receive side of the BERT from either the T3/E3 framer or from one of the 28 T1 or 16/21 E1 receive ports. Data from the transmit side of the BERT can be inserted either into the T3/E3 framer or into one of the 28 T1 or 16/21 E1 transmit ports. See Figures 1A and 1B for a visual description of where data to and from the BERT can be placed.

8.2 BERT REGISTER DESCRIPTION

Register Name: **BERTMC**
Register Description: **BERT Mux Control Register**
Register Address: **0x6Eh**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	n/a	RBPS4	RBPS3	RBPS2	RBPS1	RBPS0
Default	-	-	-	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	TBPS4	TBPS3	TBPS2	TBPS1	TBPS0
Default	-	-	-	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 4 / Receive BERT Port Select Bits 0 to 4 (RBPS0 to RBPS4). These bits determine if data from any of the 28 T1 or 16/21 E1 receive ports or the T3/E3 receive framer (with or without the overhead bits) will be routed to the receive side of the BERT. If these bits are set to 11101, only the T3/E3 payload data will be routed to the receive BERT. If these bits are set to 11110, all T3/E3 data (payload and the overhead bits) will be routed to the receive BERT.

RBPS4:0

00000	no data	01000	Port 8
00001	Port 1	01001	Port 9
00010	Port 2	01010	Port 10
00011	Port 3	01011	Port 11
00100	Port 4	01100	Port 12
00101	Port 5	01101	Port 13
00110	Port 6	01110	Port 14
00111	Port 7	01111	Port 15
10000	Port 16	11000	Port 24
10001	Port 17	11001	Port 25
10010	Port 18	11010	Port 26
10011	Port 19	11011	Port 27
10100	Port 20	11100	Port 28
10101	Port 21	11101	T3/E3 Framer (payload bits only)
10110	Port 22	11110	T3/E3 Framer (payload + overhead bits)
10111	Port 23	11111	illegal state

Bits 8 to 12 / Transmit BERT Port Select Bits 0 to 4 (TBPS0 to TBPS4). These bits determine if the transmit BERT will be used to replace the normal transmit data on any of the 28 T1 or 16/21 E1 transmit ports or at the T3/E3 transmit formatter. If these bits are set to 11101, data from the transmit BERT is only placed in the payload bit positions of the T3/E3 data stream. If these bits are set to 11110, then data from the transmit BERT is placed into all bit positions of the T3/E3 data stream (payload and the overhead bits).

TBPS4:0

00000	no data	01000	Port 8
00001	Port 1	01001	Port 9
00010	Port 2	01010	Port 10
00011	Port 3	01011	Port 11
00100	Port 4	01100	Port 12
00101	Port 5	01101	Port 13
00110	Port 6	01110	Port 14
00111	Port 7	01111	Port 15
10000	Port 16	11000	Port 24
10001	Port 17	11001	Port 25
10010	Port 18	11010	Port 26
10011	Port 19	11011	Port 27

TBPS4:0

10100	Port 20	11100	Port 28
10101	Port 21	11101	T3/E3 Framer (payload bits only)
10110	Port 22	11110	T3/E3 Framer (payload + overhead bits)
10111	Port 23	11111	illegal state

Register Name: **BERTC0**
Register Description: **BERT Control Register 0**
Register Address: **70h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	TINV	RINV	PS2	PS1	PS0	LC	RESYNC
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	IESYNC	IEBED	IEOF	n/a	RPL3	RPL2	RPL1	RPL0
Default	0	0	0	-	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Force Resynchronization (RESYNC). A low to high transition will force the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the Host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Bit 1 / Load Bit and Error Counters (LC). A low to high transition latches the current bit and error counts into the Host accessible registers BERTBC and BERTEC and clears the internal count. This bit should be toggled from low to high whenever the Host wishes to begin a new acquisition period. Must be cleared and set again for a subsequent loads.

Bits 2 to 4 / Pattern Select Bits 0 (PS0 to PS2).

000 = Pseudorandom Pattern 2^7 – 1 (ANSI T1.403-1999 Annex B)
001 = Pseudorandom Pattern 2^11 – 1 (ITU O.153)
010 = Pseudorandom Pattern 2^15 – 1 (ITU O.151)
011 = Pseudorandom Pattern QRSS (2E20 - 1 with a one forced if the next 14 positions are zero)
100 = Repetitive Pattern
101 = Alternating Word Pattern
110 = illegal state
111 = illegal state

Bit 5 / Receive Invert Data Enable (RINV).

0 = do not invert the incoming data stream
1 = invert the incoming data stream

Bit 6 / Transmit Invert Data Enable (TINV).

0 = do not invert the outgoing data stream
1 = invert the outgoing data stream

Bits 8 to 11 / Repetitive Pattern Length Bits 5 (RPL0 to RPL3).
RPL0 is the LSB and RPL3 is the MSB of a nibble that describes the how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns less than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6 bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101).

Repetitive Pattern Length Map

Length	Code	Length	Code	Length	Code	Length	Code
17 Bits	0000	18 Bits	0001	19 Bits	0010	20 Bits	0011
21 Bits	0100	22 Bits	0101	23 Bits	0110	24 Bits	0111
25 Bits	1000	26 Bits	1001	27 Bits	1010	28 Bits	1011
29 Bits	1100	30 Bits	1101	31 Bits	1101	32 Bits	1111

Bit 13 / Interrupt Enable for Counter Overflow (IEOF). Allows the receive BERT to cause an interrupt if either the Bit Counter or the Error Counter overflows. See Figure 8.2A.

0 = interrupt masked
1 = interrupt enabled

Bit 14 / Interrupt Enable for Bit Error Detected (IEBED). Allows the receive BERT to cause an interrupt if a bit error is detected. See Figure 8.2A.

0 = interrupt masked
1 = interrupt enabled

Bit 15 / Interrupt Enable for Change of Synchronization Status (IESYNC). Allows the receive BERT to cause an interrupt if there is a change of state in the synchronization status (i.e. the receive BERT either goes into or out of synchronization). See Figure 8.2A.

0 = interrupt masked
1 = interrupt enabled

Register Name: **BERTC1**
Register Description: **BERT Control Register 1**
Register Address: **72h**

Bit #	7	6	5	4	3	2	1	0
Name	EIB2	EIB1	EIB0	SBE	n/a	n/a	n/a	TC
Default	-	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	AWC7	AWC6	AWC5	AWC4	AWC3	AWC2	AWC1	AWC0
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Transmit Pattern Load (TC). A low to high transition loads the pattern generator with Repetitive or Pseudorandom pattern that is to be generated. This bit should be toggled from low to high whenever the Host wishes to load a new pattern. Must be cleared and set again for a subsequent loads.

Bit 4 / Single Bit Error Insert (SBE). A low to high transition will create a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 5 to 7 / Error Insert Bits (EIB0 to EIB2).
Will automatically insert bit errors at the prescribed rate into the generated data pattern. Useful for verifying error detection operation.

EIB2	EIB1	EIB0	Error Rate Inserted
0	0	0	no errors automatically inserted
0	0	1	10^-1 (1 error per 10 bits)
0	1	0	10^-2 (1 error per 100 bits)
0	1	1	10^-3 (1 error per 1 kbits)
1	0	0	10^-4 (1 error per 10 kbits)
1	0	1	10^-5 (1 error per 100 kbits)
1	1	0	10^-6 (1 error per 1M bits)
1	1	1	10^-7 (1 error per 10M bits)

Bits 8 to 15 / Alternating Word Count Rate (AWC0 to AWC7). When the BERT is programmed in the alternating word mode, the word in BERTRP0 will be transmitted for the count loaded into this register plus one, then flip to the other word loaded in BERTRP1 and again repeat for the same number of times. The valid count range is from 00h to FFh.

AWC Value	Alternating Count Action
00h	send the word in BERTRP0 **1** time followed by the word in BERTRP1 **1** time…
01h	send the word in BERTRP0 **2** times followed by the word in BERTRP1 **2** times…
02h	send the word in BERTRP0 **3** times followed by the word in BERTRP1 **3** times…
06h	send the word in BERTRP0 **7** times followed by the word in BERTRP1 **7** times…
07h	send the word in BERTRP0 **8** times followed by the word in BERTRP1 **8** times…
FFh	send the word in BERTRP0 **256** times followed by the word in BERTRP1 **256** times…

Register Name: **BERTRP0**
Register Description: **BERT Repetitive Pattern 0 (lower word)**
Register Address: **74h**

Bit #	7	6	5	4	3	2	1	0
Name	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
Default	0	0	0	0	0	0	0	0

Register Name: **BERTRP1**
Register Description: **BERT Repetitive Pattern 1 (upper word)**
Register Address: **76h**

Bit #	7	6	5	4	3	2	1	0
Name	RP23	RP22	RP21	RP20	RP19	RP18	RP17	RP16
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RP31	RP30	RP29	RP28	RP27	RP26	RP25	RP24
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 31 / BERT Repetitive Pattern Set (RP0 TO RP31). RP0 is the LSB and RP31 is the MSB. These registers must be properly loaded for the BERT to properly generate and synchronize to either a repetitive pattern, a pseudorandom pattern, or a alternating word pattern. For a repetitive pattern that is less than 17 bits, then the pattern should be repeated so that all 32 bits are used to describe the pattern. For example if the pattern was the repeating 5-bit pattern …01101… (where right most bit is one sent first and received first) then BERTRP0 should be loaded with xB5AD and BERTRP1 should be loaded with x5AD6. For a pseudorandom pattern, both registers should be loaded with all ones (i.e. xFFFF). For an alternating word pattern, one word should be placed into BERTRP0 and the other word should be placed into BERTRP1. For example, if the DDS stress pattern "7E" is to be described, the user would place x0000 in BERTRP0 and x7E7E in BERTRP1 and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

Register Name: **BERTBC0**
Register Description: **BERT 32-Bit Bit Counter (lower word)**
Register Address: **78h**

Bit #	7	6	5	4	3	2	1	0
Name	BBC7	BBC6	BBC5	BBC4	BBC3	BBC2	BBC1	BBC0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BBC15	BBC14	BBC13	BBC12	BBC11	BBC10	BBC9	BBC8
Default	0	0	0	0	0	0	0	0

Register Name: **BERTBC1**
Register Description: **BERT 32-Bit Bit Counter (upper word)**
Register Address: **7Ah**

Bit #	7	6	5	4	3	2	1	0
Name	BBC23	BBC22	BBC21	BBC20	BBC19	BBC18	BBC17	BBC16
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BBC31	BBC30	BBC29	BBC28	BBC27	BBC26	BBC25	BBC24
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 31 / BERT 32-Bit Bit Counter (BBC0 to BBC31). This 32-bit counter will increment for each data bit (i.e. clock received). This counter is not disabled when the receive BERT loses synchronization. This counter can be cleared by toggling the LC control bit in BERTC0. This counter saturates and will not rollover. Upon saturation, the BBCO status bit in the BERTEC0 register will be set. This error counter starts counting when the BERT goes into receive synchronization (RLOS = 0 or SYNC = 1) and it will not stop counting when the BERT loses synchronization. It is recommended that the Host toggle the LC bit in BERTC0 register once the BERT has synchronized and then toggle the LC bit again when the error checking period is complete. If the device loses synchronization during this period, then the counting results are suspect.

Register Name: **BERTEC0**
Register Description: **BERT 24-Bit Error Counter (lower) and Status Information**
Register Address: **7Ch**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	RA1	RA0	RLOS	BED	BBCO	BECO	SYNC
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Real Time Synchronization Status (SYNC). Read only real time status of the synchronizer (this bit is not latched). Will be set when the incoming pattern matches for 32 consecutive bit positions. Will be cleared when 6 or more bits out of 64 are received in error.

Bit 1 / BERT Error Counter Overflow (BECO). A latched read only event status bit which is set when the 24-bit BERT Error Counter (BEC) saturates. Cleared when read and will not be set again until another overflow occurs (i.e. the BEC counter must be cleared and allowed to overflow again). The setting of this status bit can cause a hardware interrupt to occur if the IEOF bit in BERT Control Register 0 is set to a one and the BERT bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. See Figure 8.2A.

Bit 2 / BERT Bit Counter Overflow (BBCO). A latched read only event status bit which is set when the 32-bit BERT Bit Counter (BBC) saturates. Cleared when read and will not be set again until another overflow occurs (i.e. the BBC counter must be cleared and allowed to overflow again). The setting of this status bit can cause a hardware interrupt to occur if the IEOF bit in BERT Control Register 0 is set to a one and the BERT bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. See Figure 8.2A.

Bit 3 / Bit Error Detected (BED). A latched read only event status bit which is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors. This bit will be cleared when read. The setting of this status bit can cause a hardware interrupt to occur if the IEBED bit in BERT Control Register 0 is set to a one and the BERT bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. See Figure 8.2A.

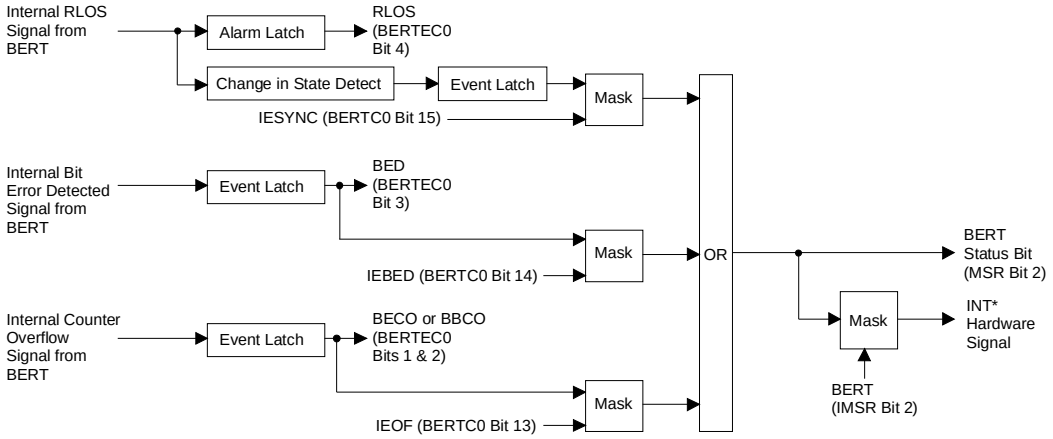
Bit 4 / Receive Loss Of Synchronization (RLOS). A latched read only alarm status bit which is set whenever the receive BERT begins searching for a pattern. Once synchronization is achieved, this bit will remain set until read. A change in this status bit (i.e. the synchronizer goes into or out of synchronization) can cause a hardware interrupt to occur if the IESYNC bit in BERT Control Register 0 is set to a one and the BERT bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read. See Figure 8.2A.

Bit 5 / Receive All Zeros (RA0). A latched read only alarm status bit which is set when 31 consecutive zeros are received. Allowed to be cleared once a one is received.

Bit 6 / Receive All Ones (RA1). A latched read only alarm status bit which is set when 31 consecutive ones are received. Allowed to be cleared once a zero is received.

Bits 8 to 15 / BERT 24-Bit Error Counter (BEC0 to BEC7). Lower byte of the 24-bit counter. See the BERTEC1 register description for details.

BERT Status Bit Flow Figure 8.2A



Note: All event and alarm latches above are cleared when the BERTEC0 register is read.

Register Name: **BERTEC1**
Register Description: **BERT 24-Bit Error Counter (upper)**
Register Address: **7Eh**

Bit #	7	6	5	4	3	2	1	0
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 15 / BERT 24-Bit Error Counter (BEC8 to BEC23). Upper two bytes of the 24-bit counter. This 24-bit counter will increment for each data bit received in error. This counter is not disabled when the receive BERT loses synchronization. This counter can be cleared by toggling the LC control bit in BERTBC0. This counter saturates and will not rollover. Upon saturation, the BECO status bit in the BERTEC0 register will be set. This error counter starts counting when the BERT goes into receive synchronization (RLOS = 0 or SYNC = 1) and it will not stop counting when the BERT loses synchronization. It is recommended that the Host toggle the LC bit in BERTC0 register once the BERT has synchronized and then toggle the LC bit again when the error checking period is complete. If the device loses synchronization during this period, then the counting results are suspect.

SECTION 9: HDLC CONTROLLER

9.1 GENERAL DESCRIPTION

The DS3112 contains an onboard HDLC controller with 256 byte buffers in both the transmit and receive paths. When the device is operated in the T3 Mode, the HDLC controller is only active in the C-Bit Parity Mode. When the device is operated in the E3 mode, the user has the option to connect the HDLC controller to the Sn bit position. On the receive side, the HDLC controller is always connected to the receive E3 framer. If the Host does not wish to use the HDLC controller for the Sn bit, then the status updates provided by the HDLC controller are ignored. On the transmit side, the Host selects the source of the Sn via the E3SnC0 and E3SnC1 controls bits in the T3/E3 Control Register (see Section 5.2 for details).

Receive Operation

On reset, the receive HDLC controller will flush the receive FIFO and begin searching for a new incoming HDLC packet. The receive HDLC controller performs a bit by bit search for a HDLC packet and when one is detected, it will zero destuff the incoming datastream and automatically byte align to it and place the incoming bytes as they are received into the receive FIFO. The first byte of each packet is marked in the receive FIFO by setting the Opening Byte (OBYTE) bit. Upon detecting a closing flag, the device will check the 16-bit CRC to see if the packet is valid or not and then mark the last byte of the packet in the receive FIFO by setting the Closing Byte (CBYTE) bit. The CRC is not passed to the receive FIFO. When the CBYTE bit is set, the Host can obtain the status of the incoming packet via the Packet Status bits (PS0 and PS1). Incoming packets can be separated by a single flag or even by two flags that share a common zero. If the receive FIFO ever fills beyond capacity, the new incoming packet data will be discarded and the Receive FIFO Overrun (ROVR) status bit will be set. If such a scenario occurs, then the last packet in the FIFO is suspect and should be discarded. When an overflow occurs, the receive HDLC will stop accepting packets until either the FIFO is completely emptied or reset. If the receive HDLC controller ever detects an incoming abort (7 or more ones in a row), it will set the Receive Abort Sequence Detected (RABT) status bit. If an abort sequence is detected in the middle of an incoming packet, then the receive HDLC controller will set the Packet Status bits accordingly.

The receive HDLC has been designed to minimize it's real time Host support requirements. The receive FIFO is 256 bytes which is deep enough to store the three T3 packets (Path ID, Idle Signal ID, and Test Signal ID) that can arrive once a second. Hence in T3 applications, the Host only needs to access the receive HDLC once a second to retrieve the three messages. The Host will be notified when a new message has begun (Receive Packet Start status bit) to be received and when a packet has completed (Receive Packet End status bit). Also the Host can be notified when the FIFO has filled beyond a programmable level called the high water mark. The Host will read the incoming packet data out of the receive FIFO a byte at a time. When the receive FIFO is empty, the REMPTY bit in the FIFO will be set.

Transmit Operation

On reset, the transmit HDLC controller will flush the transmit FIFO and transmit an abort followed by either 7Eh or FFh (depends on the setting of the TFS control bit) continuously. The transmit HDLC then waits until there are at least two bytes in the transmit FIFO before beginning to send the packet. The transmit HDLC will automatically add an opening flag of 7Eh to the beginning of the packet and zero stuff the outgoing datastream. When the transmit HDLC controller detects that the TMEND bit in the transmit FIFO is set, it will automatically calculate and add in the 16-bit CRC checksum followed by a closing flag of 7Eh. If the FIFO is empty, then it will begin sending either 7Eh or FFh continuously. If there is some more data in the FIFO, then the transmit HDLC will automatically add in the opening flag and begin sending the next packet. Between consecutive packets, there are always at least two flags of 7Eh. If the transmit FIFO ever empties when a packet is being sent (i.e. before the TMEND bit is set), then the transmit HDLC controller will send an abort of seven ones in a row (FEh) followed by a continuous transmission of either 7Eh (flags) or FFh (idle) and the Transmit FIFO Underrun (TUDR) status bit will be set. When the FIFO underruns, the transmit HDLC controller should be reset by the Host.

The transmit HDLC has been designed to minimize it's real time Host support requirements. The transmit FIFO is 256 bytes which is deep enough to store the three T3 packets (Path ID, Idle Signal ID, and Test Signal ID) that need to be sent once a second. Hence in T3 applications, the Host only needs to access the transmit HDLC once a second to load up the three messages. Once the Host has loaded an outgoing packet, it can monitor the Transmit Packet End (TEND) status bit to know when the packet has finished being transmitted. Also the Host can be notified when the FIFO has emptied below a programmable level called the low water mark. The Host must never overfill the FIFO. To keep this from occurring, the Host can obtain the real time depth of the transmit FIFO via the Transmit FIFO Level bits in the HDLC Status Register (HSR).

9.2 HDLC CONTROL AND FIFO REGISTER DESCRIPTION

Register Name: **HCR**
Register Description: **HDLC Control Register**
Register Address: **80h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	RHR	THR	TFS	n/a	TCRCI	TZSD	TCRCD
Default	-	0	0	0	-	-	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RHWMS2	RHWMS1	RHWMS0	TLWMS2	TLWMS1	TLWMS0	RID	TID
Default	0	0	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Transmit CRC Defeat (TCRCD). When this bit is set low, the HDLC will automatically calculate and append the 16 bit CRC to the outgoing HDLC message. When this bit is set high, the device will not append the CRC to the outgoing message.

0 = enable CRC generation (normal operation)
1 = disable CRC generation

Bit 1 / Transmit Zero Stuffer Defeat (TZSD). When this bit is set low, the HDLC will automatically enable the zero stuffer in between the opening and closing flags of the HDLC message. When this bit is set high, the device will not enable the zero stuffer under any condition.

0 = enable zero stuffer (normal operation)
1 = disable zero stuffer

Bit 2 / Transmit CRC Invert (TCRCI). When this bit is set low, the HDLC will allow the CRC to be generated normally. When this bit is set high, the device will invert all 16 bits of the generated CRC. This bit is ignored when the CRC generation is disabled (TCRCD = 1). This bit is useful in testing HDLC operation.

0 = do not invert the generated CRC (normal operation)
1 = Invert the generated CRC

Bit 4 / Transmit Flag/Idle Select (TFS). This control bit determines whether flags or idle bytes will be transmitted in between packets.

0 = 7Eh (flags)
1 = FFh (idle)

Bit 5 / Transmit HDLC Reset (THR). A 0 to 1 transition will reset the Transmit HDLC controller. Must be cleared and set again for a subsequent reset. A reset will flush the current contents of the transmit FIFO and cause one FEh abort sequence (7 ones is a row) to be sent followed by either 7Eh (flags) or FFh (idle) until a new packet is initiated by writing new data (at least two bytes) into the FIFO.

Bit 6 / Receive HDLC Reset (RHR). A 0 to 1 transition will reset the Receive HDLC controller. Must be cleared and set again for a subsequent reset. A reset will flush the current contents of the receive FIFO and cause the receive HDLC controller to begin searching for a new incoming HDLC packet.

Bit 8 / Transmit Invert Data (TID). The control bit determines whether all of the data from the HDLC controller (including flags and CRC checksum) will be inverted after processing.

0 = do not invert data (normal operation)
1 = invert all data

Bit 9 / Receive Invert Data (RID). The control bit determines whether all of the data into the HDLC controller (including flags and CRC checksum) will be inverted before processing.

0 = do not invert data (normal operation)
1 = invert all data

Bits 10 to 12 / Transmit Low Water Mark Select Bits (TLWMS0 to TLWMS2). These control bits determine when the HDLC controller should set the TLWM status bit in the HDLC Status Register (HSR). When the transmit FIFO contains less than the number of bytes configured by these bits, the TLWM status bit will be set to a one.

TLWMS2	TLWMS1	TLWMS0	Transmit Low Water Mark (in bytes)
0	0	0	16
0	0	1	48
0	1	0	80
0	1	1	112
1	0	0	144
1	0	1	176
1	1	0	208
1	1	1	240

Bits 13 to 15 / Receive High Water Mark Select Bits (RHWMS0 to RHWMS2). These control bits determine when the HDLC controller should set the RHWM status bit in the HDLC Status Register (HSR). When the receive FIFO contains more than the number of bytes configured by these bits, the RHWM status bit will be set to a one.

RHWMS2	RHWMS1	RHWMS0	Receive High Water Mark (in bytes)
0	0	0	16
0	0	1	48
0	1	0	80
0	1	1	112
1	0	0	144
1	0	1	176
1	1	0	208
1	1	1	240

Register Name: **RHDLC**
Register Description: **Receive HDLC FIFO**
Register Address: **82h**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	REMPTY	n/a	n/a	n/a	PS1	PS0	CBYTE	OBYTE
Default	-	-	-	-	-	-	-	-

Note: When the CPU bus is operated in the 8-bit mode (CMS = 1), the Host should always read the lower byte (bits 0 to 7) first followed by the upper byte (bits 8 to 15).
Note: Bits that are underlined are read only; all other bits are read-write.

Note: Packets with three or less bytes (including the CRC FCS) in between flags are invalid and the data that appears in the FIFO in such instances is meaningless. If only one byte is received between flags, then both the CBYTE and OBYTE bits will be set. If two bytes are received, then OBYTE will be set for the first one received and CBYTE will be set for the second byte received. If three bytes are received, then OBYTE will be set for the first one received and CBYTE will be set for the third byte received. In all of these cases, the Packet Status will be reported as PS0 = 0 / PS1 = 1 and the data in the FIFO should be ignored.

Bits 0 to 7 / Receive FIFO Data (D0 to D7). Data from the Receive FIFO can be read from these bits. D0 is the LSB and is received first while D7 is the MSB and is received last.

Bit 8 / Opening Byte (OBYTE). This bit will be set to a one when the byte available at the D0 to D7 bits from the Receive FIFO is the first byte of a HDLC packet.

Bit 9 / Closing Byte (CBYTE). This bit will be set to a one when the byte available at the D0 to D7 bits from the Receive FIFO is the last byte of a HDLC packet whether the packet is valid or not. The Host can use the PS0 and PS1 bits to determine if the packet is valid or not.

Bits 10 and 11 / Packet Status Bits 0 and 1 (PS0 and PS1). These bits are only valid when the CBYTE bit is set to a one. These bits inform the Host of the validity of the incoming packet and the cause of the problem if the packet was received in error.

PS1	PS0	Packet Status	Reason for Invalid Reception of the Packet
0	0	Valid	
0	1	Invalid	corrupt CRC
1	0	Invalid	incoming packet was either too short (3 or less bytes including the CRC) or did not contain an integral number of octets
1	1	Invalid	abort sequence detected

Bit 15 / Receive FIFO Empty (REMPTY). This real time bit will be set to a one when the Receive FIFO is empty and hence the D0 to D7 bits contain no valid information.

Register Name: **THDLC**
Register Description: **Transmit HDLC FIFO**
Register Address: **84h**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	TMEND
Default	-	-	-	-	-	-	-	0

Note: When the CPU bus is operated in the 8-bit mode (CMS = 1), the Host should always write to the lower byte (bits 0 to 7) first followed by the upper byte (bits 8 to 15).
Note: The THDLC is a write only register.
Note: The Transmit FIFO can be filled to a maximum capacity of 256 bytes. When the Transmit FIFO is full, it will not accept any additional data.

Bits 0 to 7 / Transmit FIFO Data (D0 to D7). Data for the Transmit FIFO can be written to these bits. D0 is the LSB and is transmitted first while D7 is the MSB and is transmitted last.

Bit 8 / Transmit Message End (TMEND). This bit is used to delineate multiple messages in the Transmit FIFO. It should be set to a one when the last byte of a packet is written to the Transmit FIFO. The setting of this bit indicates to the HDLC controller that the message is complete and that it should calculate and add in the CRC checksum and at least two flags. This bit should be set to zero for all other data written to the FIFO. All HDLC messages must be at least two bytes in length.

9.3 HDLC STATUS AND INTERRUPT REGISTER DESCRIPTION

Register Name: **HSR**
Register Description: **HDLC Status Register**
Register Address: **86h**

Bit #	7	6	5	4	3	2	1	0
Name	TUDR	RPE	RPS	RHWM	n/a	TLWM	n/a	TEND
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	RABT	n/a	ROVR	TEMPTY	TFL3	TFL2	TFL1	TFL0
Default	-	-	-	-	-	-	-	-

Note: See Figure 9.3A for details on the signal flow for the status bits in the HSR register.
Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Transmit Packet End (TEND). This latched read only event status bit will be set to a one each time the transmit HDLC controller reads a transmit FIFO byte with the corresponding TMEND bit set or if a FIFO underrun occurs. This bit will be cleared when read and will not be set again until another message end is detected. The setting of this bit can cause a hardware interrupt to occur if the TEND bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 2 / Transmit FIFO Low Water Mark (TLWM). This read only real time status bit will be set to a one when the transmit FIFO contains less than the number of bytes configured by the Transmit Low Water Mark Setting control bits (TLWMS0 to TLWMS2) in the HDLC Control Register (HCR). This bit will be cleared when the FIFO fills beyond the Low Water Mark. The setting of this bit can cause a hardware interrupt to occur if the TLWM bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one.

Bit 4 / Receive FIFO High Water Mark (RHWM). This read only real time status bit will be set to a one when the receive FIFO contains more than the number of bytes configured by the Receive High Water Mark Setting control bits (RHWMS0 to RHWMS2) in the HDLC Control Register (HCR). This bit will be cleared when the FIFO empties below the High Water Mark. The setting of this bit can cause a hardware interrupt to occur if the RHWM bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one.

Bit 5 / Receive Packet Start (RPS). This latched read only event status bit will be set to a one each time the HDLC controller detects an opening byte of an HDLC packet. This bit will be cleared when read and will not be set again until another message is detected. The setting of this bit can cause a hardware interrupt to occur if the RPS bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 6 / Receive Packet End (RPE). This latched read only event status bit will be set to a one each time the HDLC controller detects the finish of a message whether the packet is valid (CRC correct) or not (bad CRC, abort sequence detected, packet too small, not an integral number of octets, or an overrun occurred). This bit will be cleared when read and will not be set again until another message end is detected. The setting of this bit can cause a hardware interrupt to occur if the RPE bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 7 / Transmit FIFO Underrun (TUDR). This latched read only event status bit will be set to a one each time the transmit FIFO underruns and an abort is automatically sent. This bit will be cleared when read and will not be set again until another underrun occurs (i.e. the FIFO has been written to and then allowed to empty again). The setting of this bit can cause a hardware interrupt to occur if the TUDR bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bits 8 to 11 / Transmit FIFO Level Bits 0 to 3 (TFL0 to TFL3). These read only real time status bits indicate the current depth of the transmit FIFO with a 16 byte resolution. These status bits cannot cause a hardware interrupt.

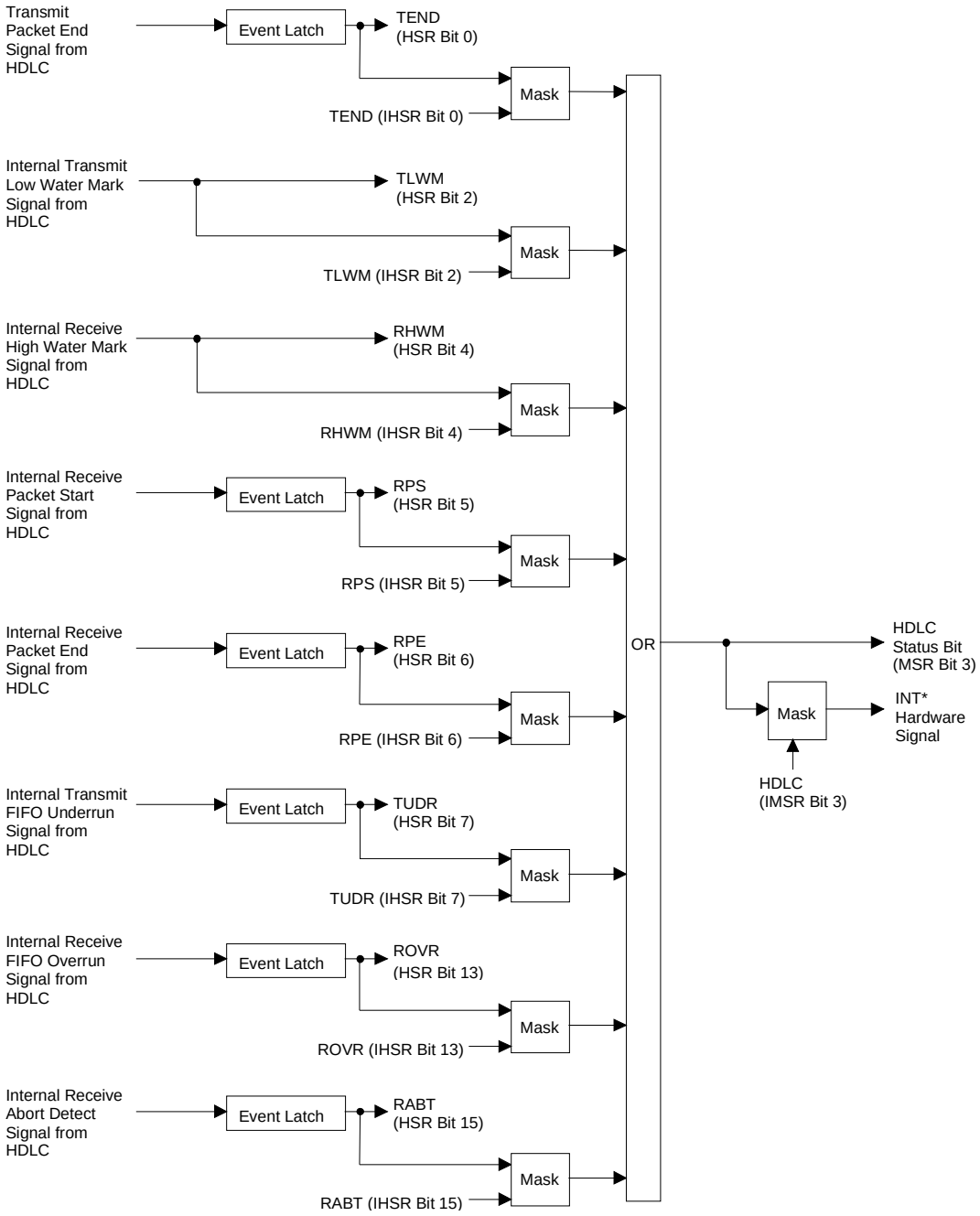
TFL3	TFL2	TFL1	TFL0	Transmit FIFO Level
0	0	0	0	empty to 15 bytes
0	0	0	1	16 to 31 bytes
0	0	1	0	32 to 47 bytes
0	0	1	1	48 to 63 bytes
0	1	0	0	64 to 79 bytes
0	1	0	1	80 to 95 bytes
0	1	1	0	96 to 111 bytes
0	1	1	1	112 to 127 bytes
1	0	0	0	128 to 143 bytes
1	0	0	1	144 to 159 bytes
1	0	1	0	160 to 175 bytes
1	0	1	1	176 to 191 bytes
1	1	0	0	192 to 207 bytes
1	1	0	1	208 to 223 bytes
1	1	1	0	224 to 239 bytes
1	1	1	1	240 to 256 bytes

Bit 12 / Transmit FIFO Empty (TEMPTY). This read only real time status bit will be set to a one when the transmit FIFO is empty. It will be cleared when the transmit FIFO contains one or more bytes. This status bit cannot cause a hardware interrupt.

Bit 13 / Receive FIFO Overrun (ROVR). This latched read only event status bit will be set to a one each time the receive FIFO overruns. This bit will be cleared when read and will not be set again until another overrun occurs (i.e. the FIFO has been read from and then allowed to fill up again). The setting of this bit can cause a hardware interrupt to occur if the ROVR bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bit 15 / Receive Abort Sequence Detected (RABT). This latched read only event status bit will be set to a one each time the receive HDLC controller detects 7 or more ones in a row during packet reception. If the receive HDLC is not currently receiving a packet, then 7 or more ones in a row will not trigger this status bit. This bit will be cleared when read and will not be set again until another abort is detected (at least one valid flag must be detected before another abort can be detected). The setting of this bit can cause a hardware interrupt to occur if the RABT bit in the Interrupt Mask for HSR (IHSR) register is set to a one and the HDLC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

HSR Status Bit Flow Figure 4.3E



Note: All event latches above are cleared when the HSR register is read.

Register Name: **IHSR**
Register Description: **Interrupt Mask for HDLC Status Register**
Register Address: **88h**

Bit #	7	6	5	4	3	2	1	0
Name	TUDR	RPE	RPS	RHWM	n/a	TLWM	n/a	TEND
Default	0	0	0	0	-	0	-	0

Bit #	15	14	13	12	11	10	9	8
Name	RABT	n/a	ROVR	n/a	n/a	n/a	n/a	n/a
Default	0	-	0	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Transmit Packet End (TEND).
0 = interrupt masked
1 = interrupt unmasked

Bit 2 / Transmit FIFO Low Water Mark (TLWM).
0 = interrupt masked
1 = interrupt unmasked

Bit 4 / Receive FIFO High Water Mark (RHWM).
0 = interrupt masked
1 = interrupt unmasked

Bit 5 / Receive Packet Start (RPS).
0 = interrupt masked
1 = interrupt unmasked

Bit 6 / Receive Packet End (RPE).
0 = interrupt masked
1 = interrupt unmasked

Bit 7 / Transmit FIFO Underrun (TUDR).
0 = interrupt masked
1 = interrupt unmasked

Bit 13 / Receive FIFO Overrun (ROVR).
0 = interrupt masked
1 = interrupt unmasked

Bit 15 / Receive Abort Sequence Detected (RABT).
0 = interrupt masked
1 = interrupt unmasked

SECTION 10: FEAC CONTROLLER

10.1 GENERAL DESCRIPTION

The DS3112 contains an onboard FEAC controller. When the device is operated in the T3 Mode, the FEAC controller is only active in the C-Bit Parity Mode. When the device is operated in the E3 mode, the user has the option to connect the FEAC controller to the Sn bit position. On the receive side, the FEAC controller is always connected to the receive E3 framer. If the Host does not wish to use the FEAC controller for the Sn bit, then the status updates provided by the FEAC controller are ignored. On the transmit side, the Host selects the source of the Sn via the E3SnC0 and E3SnC1 controls bits in the T3/E3 Control Register (see Section 5.2 for details).

The DS3112 can both detect and generate Far End Alarm Codewords (FEAC). The FEAC codeword is a repeating 16 bit pattern of the form ...0xxxxxx011111111... where the rightmost bit is transmitted first. The FEAC codeword must be transmitted at least 10 times. When no FEAC codeword is being transmitted, the data pattern should be forced to all ones.

The receive FEAC detector does a bit by bit search for a data pattern of the form of a FEAC codeword. Once found, the receive FEAC detector validates incoming codewords by checking to see that the same codeword is found in three consecutive opportunities. Once validated, a codeword is considered no longer present when it is received incorrectly twice in a row. Once a codeword is validated, the Receive FEAC Codeword Detect (RFCD) status bit is set and the codeword is written into the Receive FEAC FIFO for the Host to read. The Host can use the RFCD status to know when to read the Receive FEAC FIFO. The Receive FEAC FIFO is four codewords deep. If the FIFO is full when the receive FEAC detector attempts to write a new incoming codeword, the latest incoming codeword(s) will be discarded and the Receive FEAC FIFO Overflow (RFFO) status bit will be set.

The DS3112 can transmit two different FEAC codewords. This is useful if the Host wishes to generate a Loopback Command which is made up of 10 FEAC codewords that indicate the type of loopback followed by 10 FEAC codewords that indicate which line is to be looped back.

10.2 FEAC CONTROL REGISTER DESCRIPTION

Register Name: **FCR**
Register Description: **FEAC Control Register**
Register Address: **90h**

Bit #	7	6	5	4	3	2	1	0
Name	TFS1	TFS0	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
Default	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	RFR	n/a	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
Default	0	-	0	0	0	0	0	0

Note: Bits that are underlined are read only; all other bits are read-write.

Bits 0 to 5 / Transmit FEAC Codeword A Data (TFCA0 to TFCA5). The FEAC codeword is of the form ...0xxxxxx011111111... where the rightmost bit is transmitted first. These six bits are the middle six bits of the second byte of the FEAC codeword (i.e. the six "x" bits). The device can generate two different codewords and these six bits represent what will be transmitted for codeword A. TFCA0 is the LSB and is transmitted first while TFCA5 is the MSB and is transmitted last. The TFS0 and TFS1 control bits determine if this codeword is to be generated. These bits should only be changed when the transmit FEAC controller is in the idle state (TFS0 = 0 and TFS1 = 0).

Bits 6 and 7 / Transmit FEAC Codeword Select Bits 0 and 1 (TFS0 and TFS1). These two bits control which of the two available codewords are to be generated. Both TFS0 and TFS1 are edge triggered. To change the action, the Host must go back to the null state (TFS0 = TFS1 = 0) before proceeding to the desired action.

TFS1	TFS0	Action
0	0	idle state; do not generate a FEAC codeword (send all ones)
0	1	send 10 of codeword A followed by all ones
1	0	send 10 of codeword A followed by 10 of codeword B followed by all ones
1	1	send codeword A continuously (will be sent for at least 10 times)

Bits 8 to 13 / Transmit FEAC Codeword B Data (TFCB0 to TFCB5). The FEAC codeword is of the form ...0xxxxxx011111111... where the rightmost bit is transmitted first. These six bits are the middle six bits of the second byte of the FEAC codeword (i.e. the six "x" bits). The device can generate two different codewords and these six bits represent what will be transmitted for codeword B. TFCB0 is the LSB and is transmitted first while TFCB5 is the MSB and is transmitted last. The TFS0 and TFS1 control bits determine if this codeword is to be generated. These bits should only be changed when the transmit FEAC controller is in the idle state (TFS0 = 0 and TFS1 = 0).

Bit 15 / Receive FEAC Controller Reset (RFR). A 0 to 1 transition will reset the receive FEAC controller and flush the Receive FEAC FIFO. This bit must be cleared and set again for a subsequent reset.

10.3 FEAC STATUS REGISTER DESCRIPTION

Register Name: **FSR**
Register Description: **FEAC Status Register**
Register Address: **92h**

Bit #	7	6	5	4	3	2	1	0
Name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	RFCD
Default	-	-	-	-	-	-	-	-

Bit #	15	14	13	12	11	10	9	8
Name	RFFO	RFFE	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
Default	-	-	-	-	-	-	-	-

Note: Bits that are underlined are read only; all other bits are read-write.

Bit 0 / Receive FEAC Codeword Detected (RFCD). This latched read only event status bit will be set to a one each time the FEAC controller has detected and validated a new FEAC codeword. This bit will be cleared when read and will not be set again until another new codeword is detected. The setting of this bit can cause a hardware interrupt to occur if the FEAC bit in the Interrupt Mask for MSR (IMSR) register is set to a one. The interrupt will be allowed to clear when this bit is read.

Bits 8 to 13 / Receive FEAC FIFO Data (RFF0 to RFF5). Data from the Receive FEAC FIFO can be read from these bits. The FEAC codeword is of the form ...0xxxxxx011111111... where the rightmost bit is received first. These six bits are the debounced and integrated middle six bits of the second byte of the FEAC codeword (i.e. the six "x" bits). RFF0 is the LSB and is received first while RFF5 is the MSB and is received last.

Bit 14 / Receive FEAC FIFO Empty (RFFE). This read only real time status bit will be set to a one when the Receive FEAC FIFO is empty and hence the RFF0 to RFF5 bits contain no valid information.

Bit 15 / Receive FEAC FIFO Overflow (RFFO). This latched read only event status bit will be set to a one when the receive FEAC controller has attempted to write to an already full Receive FEAC FIFO and current incoming FEAC codeword is lost. This bit will be cleared when read and will not be set again until another FIFO overflow occurs (i.e. the Receive FEAC FIFO has been read and then fills beyond capacity).

SECTION 11: JTAG

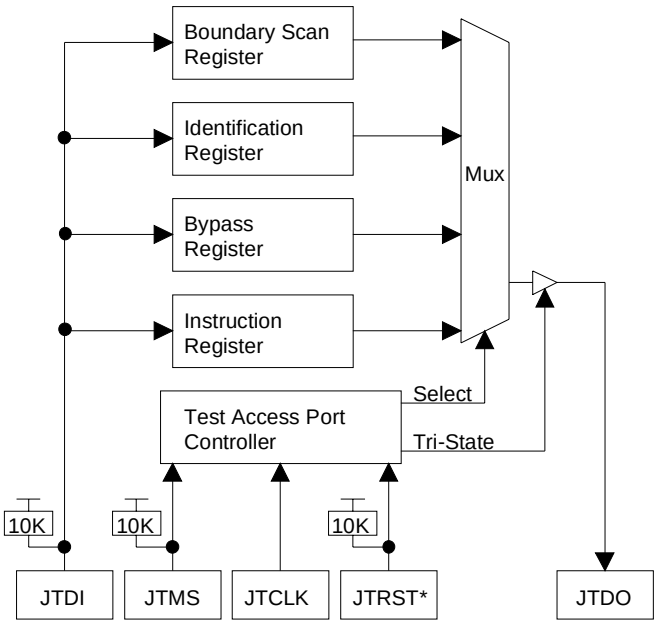
11.1 JTAG DESCRIPTION

The DS3112 device supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, IDCODE. See Figure 11.1A for a Block Diagram. The DS3112 contains the following items which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)
TAP Controller
Instruction Register
Bypass Register
Boundary Scan Register
Device Identification Register.

The Test Access Port has the necessary interface pins, namely JTCLK, JTRST*, JTDI, JTDO, and JTMS. Details on these pins can be found in Section 2.9. Details on the Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

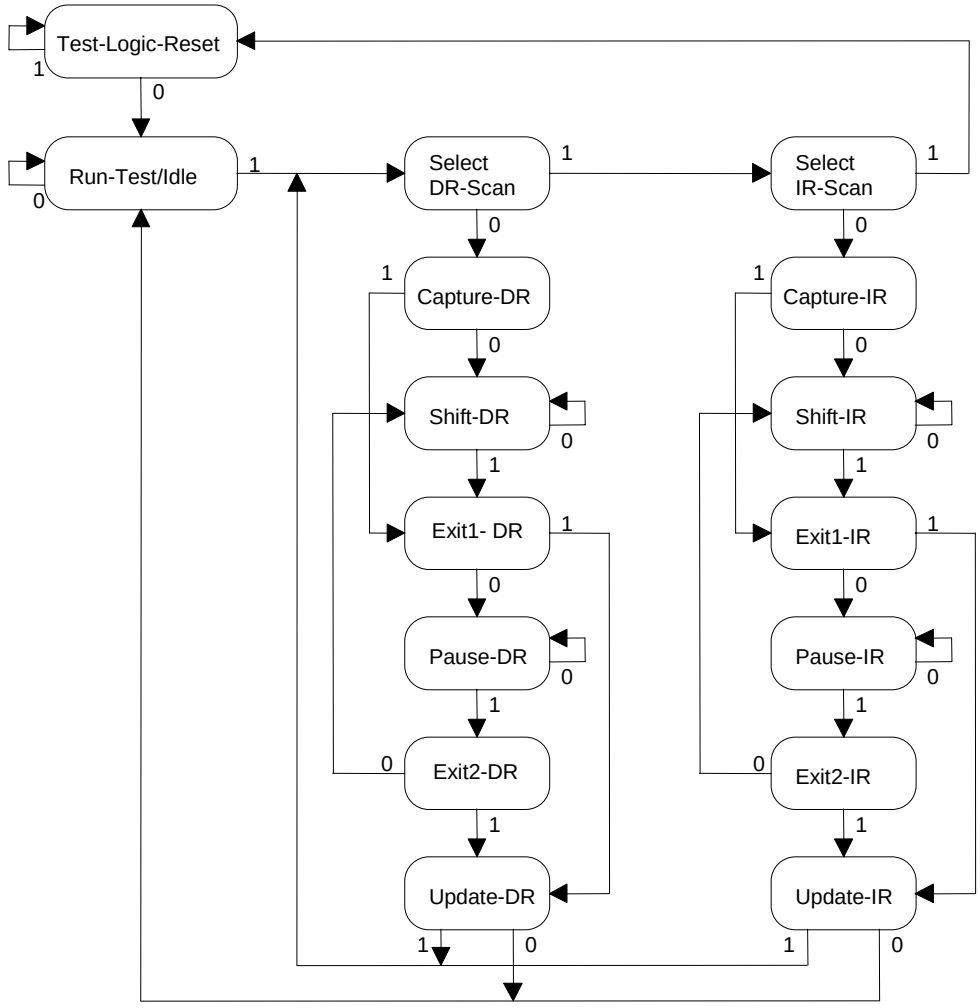
JTAG Block Diagram Figure 11.1A



11.2 TAP CONTROLLER STATE MACHINE DESCRIPTION

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. Please See Figure 11.2A for details on each of the states described below. The TAP controller is a finite state machine which responds to the logic level at JTMS on the rising edge of JTCLK.

TAP Controller State Machine Figure 11.2A



Test-Logic-Reset

Upon power-up of the DS3112, the TAP controller will be in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic on the DS3112 will operate normally.

Run-Test-Idle

Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and Test register will remain idle.

Select-DR-Scan

All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR

Data may be parallel loaded into the Test Data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is low or it will go to the Exit1-DR state if JTMS is high.

Shift-DR

The Test Data register selected by the current instruction will be connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a Test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

Exit1-DR

While in this state, a rising edge on JTCLK with JTMS high will put the controller in the Update-DR state which terminates the scanning process. A rising edge on JTCLK with JTMS low will put the controller in the Pause-DR state.

Pause-DR

Shifting of the Test registers is halted while in this state. All Test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is low. A rising edge on JTCLK with JTMS high will put the controller in the Exit2-DR state.

Exit2-DR

While in this state, a rising edge on JTCLK with JTMS high will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS low will enter the Shift-DR state.

Update-DR

A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low, will put the controller in the Run-Test-Idle state. With JTMS high, the controller will enter the Select-DR-Scan state.

Select-IR-Scan

All Test registers retain their previous state. The Instruction register will remain unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR

The Capture-IR state is used to load the shift register in the Instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller will enter the Shift-IR state.

Shift-IR

In this state, the shift register in the Instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all Test registers remain at their previous states. A rising edge on JTCLK with JTMS high will move the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low will keep the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR

A rising edge on JTCLK with JTMS low will put the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

Pause-IR

Shifting of the Instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR

A rising edge on JTCLK with JTMS high will put the controller in the Update-IR state. The controller will loop back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR

The instruction shifted into the Instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low, will put the controller in the Run-Test-Idle state. With JTMS high, the controller will enter the Select-DR-Scan state.

11.3 INSTRUCTION REGISTER AND INSTRUCTIONS

The Instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register will be connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low will shift data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS3112 and their respective operational binary codes are shown in Table 11.3A.

Instruction Codes Table 11.3A

Instructions	Selected Register	Instruction Codes
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD

A mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the DS3112 can be sampled at the Boundary Scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the DS3112 to shift data into the Boundary Scan register via JTDI using the Shift-DR state.

EXTEST

EXTEST allows testing of all interconnections to the DS3112. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The Boundary Scan register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the Boundary Scan register.

BYPASS

When the BYPASS instruction is latched into the parallel Instruction register, JTDI connects to JTDO through the one-bit Bypass Test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

IDCODE

When the IDCODE instruction is latched into the parallel Instruction register, the Identification Test register is selected. The device identification code will be loaded into the Identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The device ID code will always have a one in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. The device ID code for the DS3112 is **0000B143h**.

HIGHZ

All digital outputs will be placed into a high impedance state. The Bypass Register will be connected between JTDI and JTDO.

CLAMP

All digital outputs will output data from the boundary scan parallel output while connecting the Bypass Register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

11.4 TEST REGISTERS

IEEE 1149.1 requires a minimum of two Test registers; the Bypass register and the Boundary Scan register. An optional Test register has been included in the DS3112 design. This Test register is the Identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions which provides a short path between JTDI and JTDO.

Identification Register

The Identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 196 bits in length. Table 11.4A shows all of the cell bit locations and definitions.

Boundary Scan Control Bits Table 11.4A

Bit	Symbol	Lead	I/O or Control Bit Description
0	OUT_ENB	control bit	0 = outputs are active 1 = outputs are 3-state (“z”)
1	TEST	C3	I
2	CINT_ENB_N	control bit	0 = CINT* is a zero (“0”) 1 = CINT* is 3-state (“z”)
3	CINT_OUT	A2	O (open drain)
4	CINT_IN	A2	I
5	CMS	B2	I
6	CIM	B3	I
7	CCS*	C4	I
8	CRD*	D5	I
9	CWR*	A3	I
10	T3E3MS	B4	I
11	RST*	C5	I
12	G747E	B6	I
13	CALE	C7	I
14	FRMECU	A7	I
15	FRLOF	C8	O
16	FRLOS	B8	O
17	FRSOF	A8	O
18	FRDEN	C9	O
19	FRD	B9	O
20	FRCLK	A9	O
21	FTDEN	C10	O
22	FTD	B10	I
23	FTCLK	A10	I
24	FTSOF_ENB_N	control bit	1 = FTSOF is an input 0 = FTSOF is an output
25	FTSOF_OUT	A11	O
26	FTSOF_IN	A11	I
27	FTMEI	C11	I
28	HRNEG	C12	I
29	HRCLK	A13	I
30	HRPOS	B13	I
31	HTNEG	A14	O
32	HTCLK	B14	O

Bit	Symbol	Lead	I/O or Control Bit Description
33	HTPOS	C14	O
34	LTCCLK	G19	I
35	LRCCLK	G20	I
36	LTCLK28	H18	I
37	LTDAT28	H19	I
38	LRCLK28	H20	O
39	LRDAT28	J18	O
40	LTCLK27	J19	I
41	LTDAT27	J20	I
42	LRCLK27	K18	O
43	LRDAT27	K19	O
44	LTCLK26	K20	I
45	LTDAT26	L20	I
46	LRCLK26	L18	O
47	LRDAT26	L19	O
48	LTCLK25	M20	I
49	LTDAT25	M19	I
50	LRCLK25	M18	O
51	LRDAT25	M17	O
52	LTCLK24	N20	I
53	LTDAT24	N19	I
54	LRCLK24	N18	O
55	LRDAT24	P20	O
56	LTCLK23	P19	I
57	LTDAT23	P18	I
58	LRCLK23	R20	O
59	LRDAT23	R19	O
60	LTCLK22	P17	I
61	LTDAT22	R18	I
62	LRCLK22	T20	O
63	LRDAT22	T19	O
64	LTCLK21	T18	I
65	LTDAT21	U20	I
66	LRCLK21	V20	O
67	LRDAT21	T17	O
68	LTCLK20	U18	I
69	LTDAT20	U19	I
70	LRCLK20	V19	O
71	LRDAT20	W20	O
72	LTCLK19	Y20	I
73	LTDAT19	W19	I
74	LRCLK19	V18	O
75	LRDAT19	Y19	O
76	LTCLK18	W18	I
77	LTDAT18	V17	I
78	LRCLK18	U16	O
79	LRDAT18	Y18	O

Bit	Symbol	Lead	I/O or Control Bit Description
80	LTCLK17	W17	I
81	LTDAT17	V16	I
82	LRCLK17	Y17	O
83	LRDAT17	W16	O
84	LTCLK16	V15	I
85	LTDAT16	U14	I
86	LRCLK16	Y16	O
87	LRDAT16	W15	O
88	LTCLK15	V14	I
89	LTDAT15	Y15	I
90	LRCLK15	W14	O
91	LRDAT15	Y14	O
92	LTCLK14	V13	I
93	LTDAT14	W13	I
94	LRCLK14	Y13	O
95	LRDAT14	V12	O
96	LTCLK13	W12	I
97	LTDAT13	Y12	I
98	LRCLK13	V11	O
99	LRDAT13	W11	O
100	LTCLK12	Y11	I
101	LTDAT12	Y10	I
102	LRCLK12	V10	O
103	LRDAT12	W10	O
104	LTCLK11	Y9	I
105	LTDAT11	W9	I
106	LRCLK11	V9	O
107	LRDAT11	U9	O
108	LTCLK10	Y8	I
109	LTDAT10	W8	I
110	LRCLK10	V8	O
111	LRDAT10	Y7	O
112	LTCLK9	W7	I
113	LTDAT9	V7	I
114	LRCLK9	Y6	O
115	LRDAT9	W6	O
116	LTCLK8	U7	I
117	LTDAT8	V6	I
118	LRCLK8	Y5	O
119	LRDAT8	W5	O
120	LTCLK7	V5	I
121	LTDAT7	Y4	I
122	LRCLK7	Y3	O
123	LRDAT7	U5	O
124	LTCLK6	V4	I
125	LTDAT6	W4	I
126	LRCLK6	Y2	O

Bit	Symbol	Lead	I/O or Control Bit Description
127	LRDAT6	W3	O
128	LTCLK5	V3	I
129	LTDAT5	W1	I
130	LRCLK5	V2	O
131	LRDAT5	U3	O
132	LTCLK4	T4	I
133	LTDAT4	V1	I
134	LRCLK4	U2	O
135	LRDAT4	T3	O
136	LTCLK3	U1	I
137	LTDAT3	T2	I
138	LRCLK3	R3	O
139	LRDAT3	P4	O
140	LTCLK2	R2	I
141	LTDAT2	P3	I
142	LRCLK2	R1	O
143	LRDAT2	P2	O
144	LTCLK1	P1	I
145	LTDAT1	N3	I
146	LRCLK1	N2	O
147	LRDAT1	N1	O
148	LTCLKB	M3	I
149	LTDATB	M2	I
150	LRCLKB	M1	O
151	LRDATB	L3	O
152	LTCLKA	L2	I
153	LTDATA	L1	I
154	LRCLKA	K1	O
155	LRDATA	K3	O
156	CA7	K2	I
157	CA6	J1	I
158	CA5	J2	I
159	CA4	J3	I
160	CA3	J4	I
161	CA2	H1	I
162	CA1	H2	I
163	CA0	H3	I
164	CD15_OUT	G1	O
165	CD15_IN	G1	I
166	CD14_OUT	G2	O
167	CD14_IN	G2	I
168	CD13_OUT	G3	O
169	CD13_IN	G3	I
170	CD12_OUT	F1	O
171	CD12_IN	F1	I
172	CD11_OUT	F2	O
173	CD11_IN	F2	I

Bit	Symbol	Lead	I/O or Control Bit Description
174	CD10_OUT	G4	O
175	CD10_IN	G4	I
176	CD9_OUT	F3	O
177	CD9_IN	F3	I
178	CD8_OUT	E1	O
179	CD8_IN	E1	I
180	CD7_OUT	E2	O
181	CD7_IN	E2	I
182	CD6_OUT	E3	O
183	CD6_IN	E3	I
184	CD5_OUT	D1	O
185	CD5_IN	D1	I
186	CD4_OUT	C1	O
187	CD4_IN	C1	I
188	CD3_OUT	E4	O
189	CD3_IN	E4	I
190	CD2_OUT	D3	O
191	CD2_IN	D3	I
192	CD1_OUT	D2	O
193	CD1_IN	D2	I
194	CD0_OUT	C2	O
195	CD0_IN	C2	I
196	CD_ENB_N	control bit	1 = CD is an input 0 = CD is an output

SECTION 12: ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Lead with Respect to VSS (except VDD)	-0.3V to 5.5V
Supply Voltage (V_{DD}) with Respect to VSS	-0.3V to 3.63V
Operating Temperature	0C to +70C
Storage Temperature	-55C to +125C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note: The typical values listed below are not production tested.

RECOMMEND DC OPERATING CONDITIONS (0°C to +70°C for DS3112; -40° to +85°C for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	-0.3		0.8	V	
Supply (V_{DD})	V_{DD}	3.135		3.465	V	

DC CHARACTERISTICS (0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112; -40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Current @ V_{DD} = 3.465V	I_{DD}		150		mA	1
Lead Capacitance	C_{IO}		7		pF	
Input Leakage	I_{IL}	-10		+10	uA	2
Input Leakage (w/ pull-ups)	I_{ILP}	-500		+500	uA	2
Output Leakage	I_{LO}	-10		+10	uA	3
Output Current (2.4V)	I_{OH}	-4.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. FTCLK = HRCLK = 44.736 MHz and LTCLK1 to LTCLK28 = 1.544 MHz; other inputs at V_{DD} or grounded; other outputs left open circuited
2. $0V < V_{IN} < V_{DD}$
3. Outputs in Tri-State

AC CHARACTERISTICS – LOW SPEED (T1 and E1) PORTS

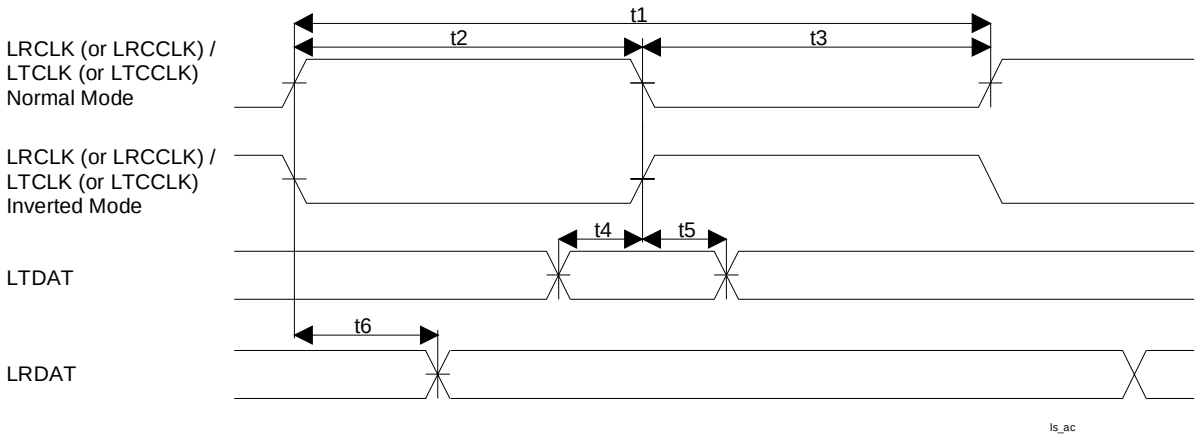
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
LRCLK / LRCCLK / LTCLK / LTCCLK Clock Period	t1 t1		648 488		ns ns	1 2
LRCLK Clock High Time	t2 t2	294 204	324 244	354 284	ns ns	1 2
LTCLK / LTCCLK / LRCCLK Clock High Time	t2	100			ns	
LRCLK Clock Low Time	t3 t3	294 204	324 244	354 284	ns ns	1 2
LTCLK / LTCCLK / LRCCLK Clock Low Time	t3	100			ns	
LTDAT Set Up Time to the Falling Edge or Rising Edge of LTCLK / LTCCLK	t4	50			ns	
LTDAT Hold Time from the Falling Edge or Rising Edge of LTCLK / LTCCLK	t5	50			ns	
Delay from the Rising Edge or Falling Edge of LRCLK to Data Valid on LRDAT	t6			25	ns	
Delay from the Rising Edge or Falling Edge of LRCCLK to Data Valid on LRDAT	t6			100	ns	5

NOTES:

1. T3 Mode
2. E3 Mode
3. In Normal Mode, LTDAT is sampled on the falling edge of LTCLK / LTCCLK and LRDAT is updated on the rising edge of LRCLK / LRCCLK
4. In Inverted Mode, LTDAT is sampled on the rising edge of LTCLK / LTCCLK and LRDAT is updated on the falling edge of LRCLK / LRCCLK
5. LRCCLK is enabled (see Section 4.2 and Figures 1A and 1B and 1C for details)

LOW SPEED (T1 and E1) PORT AC TIMING DIAGRAM Figure 12A



AC CHARACTERISTICS – HIGH SPEED (T3 and E3) PORTS

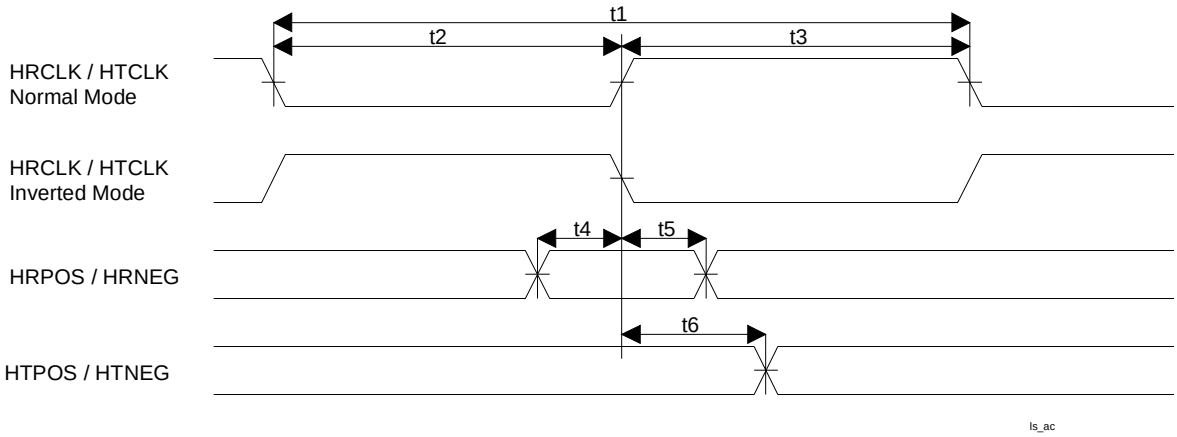
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
HRCLK / HTCLK Clock Period	t1 t1		22.4 29.1		ns ns	1, 3 2, 3
HRCLK Clock Low Time	t2	9			ns	
HRCLK Clock High Time	t3	9			ns	
HRPOS/HRNEG Set Up Time to the Rising Edge or Falling Edge of HRCLK	t4	3			ns	
HRPOS/HRNEG Hold Time from the Rising Edge or Falling Edge of HRCLK	t5	3			ns	
Delay from the Rising Edge or Falling Edge of HTCLK to Data Valid on HTPOS/HTNEG	t6			5	ns	

NOTES:

1. T3 Mode
2. E3 Mode
3. HTCLK is a buffered version of either FTCLK or HRCLK and as such, the duty cycle of HTCLK is determined by the source clock
4. In Normal Mode, HRPOS and HRNEG are sampled on the rising edge of HRCLK and HTPOS and HTNEG are updated on the rising edge of HTCLK
5. In Inverted Mode, HRPOS and HRNEG are sampled on the falling edge of HRCLK and HTPOS and HTNEG are updated on the falling edge of HTCLK

HIGH SPEED (T3 and E3) PORT AC TIMING DIAGRAM Figure 12B



AC CHARACTERISTICS – FRAMER (T3 and E3) PORTS

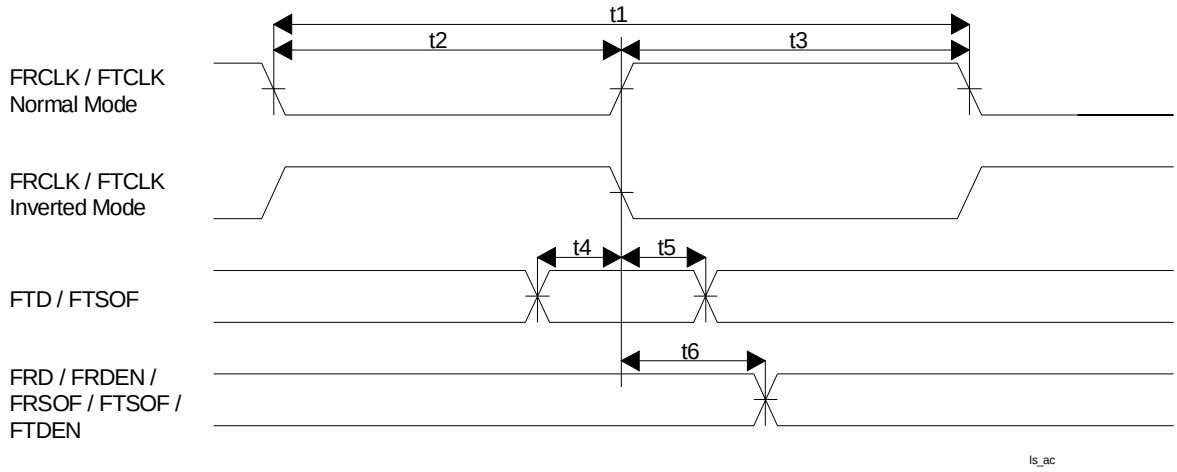
(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
FRCLK / FTCLK Clock Period	t1		22.4		ns	1, 3
	t1		29.1		ns	2, 3
FTCLK Clock Low Time	t2	9			ns	
FTCLK Clock High Time	t3	9			ns	
FTD/FTSOF Set Up Time to the Rising Edge or Falling Edge of FTCLK	t4	3			ns	4
FTD/FTSOF Hold Time from the Rising Edge or Falling Edge of FTCLK	t5	3			ns	4
Delay from the Rising Edge or Falling Edge of FRCLK/FTCLK to Data Valid on FRDEN/FRD/FRSOF/ FTDEN/FTSOF	t6			5	ns	5

NOTES:

1. T3 Mode
2. E3 Mode
3. FRCLK is a buffered version of either FTCLK or HRCLK and as such, the duty cycle of FRCLK is determined by the source clock
4. FTSOF is configured to be an input
5. FTSOF is configured to be an output
6. In Normal Mode, FTD (and FTSOF if it is configured as an input) is sampled on the rising edge of FTCLK and FRDEN, FRD, FRSOF, FTDEN (and FTSOF if it is configured as an output) are updated on the rising edge of FRCLK or FTCLK
7. In Inverted Mode, FTD (and FTSOF if it is configured as an input) is sampled on the falling edge of FTCLK and FRDEN, FRD, FRSOF, FTDEN (and FTSOF if it is configured as an output) are updated on the falling edge of FRCLK or FTCLK

FRAMER (T3 and E3) PORT AC TIMING DIAGRAM Figure 12C



AC CHARACTERISTICS – CPU BUS

(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Set Up Time for CA[7:0] Valid to CCS* Active	t1	0			ns	
Set Up Time for CCS* Active to CRD*, CWR*, or CDS* Active	t2	0			ns	
Delay Time from CRD* or CDS* Active to CD[15:0] Valid	t3			65	ns	
Hold Time from CRD* or CWR* or CDS* Inactive to CCS* Inactive	t4	0			ns	
Hold Time from CCS* or CRD* or CDS* Inactive to CD[15:0] Tri-State	t5	5		20	ns	
Wait Time from CWR* or CDS* Active to Latch CD[15:0]	t6	65			ns	
CD[15:0] Set Up Time to CWR* or CDS* Inactive	t7	10			ns	
CD[15:0] Hold Time from CWR* or CDS* Inactive	t8	2			ns	
CA[7:0] Hold from CWR* or CRD* or CDS* Inactive	t9	5			ns	

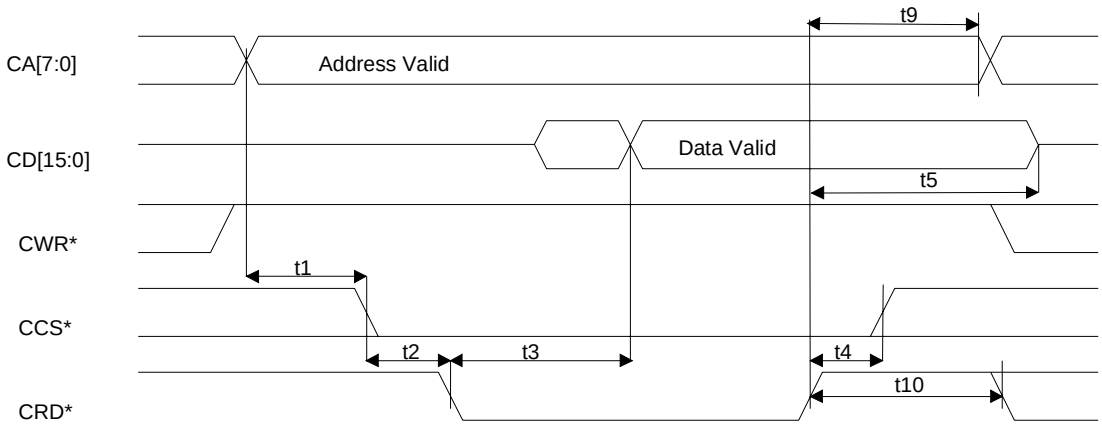
Parameter	Symbol	Min	Typ	Max	Units	Notes
CRD*, CWR* or CDS* Inactive Time	t10	75			ns	
Muxed Address Valid to CALE Falling	t11	10			ns	2
Muxed Address Hold Time	t12	10			ns	2
CALE Pulse Width	t13	30			ns	2
Setup time for CALE high or muxed address valid to CCS* active	t14	0			ns	2

NOTES:

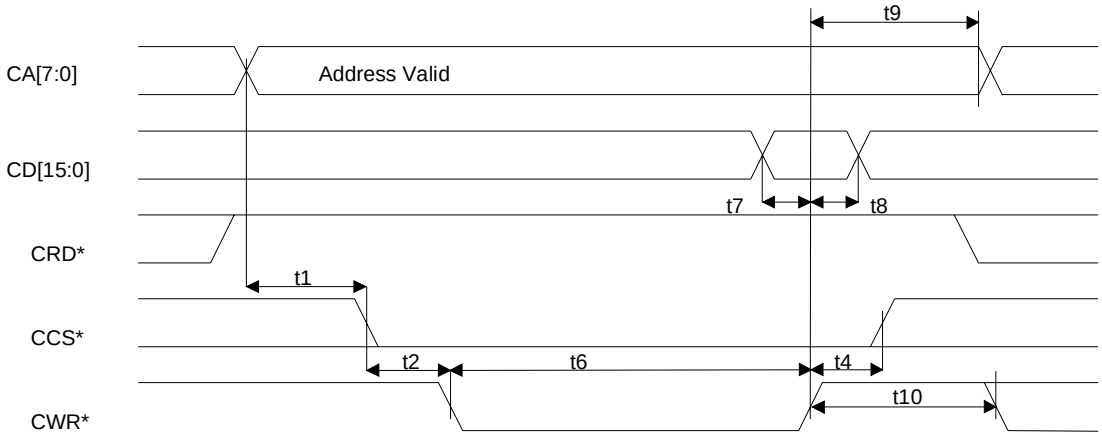
1. In non-multiplexed bus applications (see Figure 12D), CALE should be tied high.
2. In multiplexed bus applications (see Figure 12E), CA[7:0] should be tied to CD[7:0] and the falling edge of CALE will latch the address.

CPU BUS AC TIMING DIAGRAM (non-multiplexed) Figure 12D

Intel Read Cycle



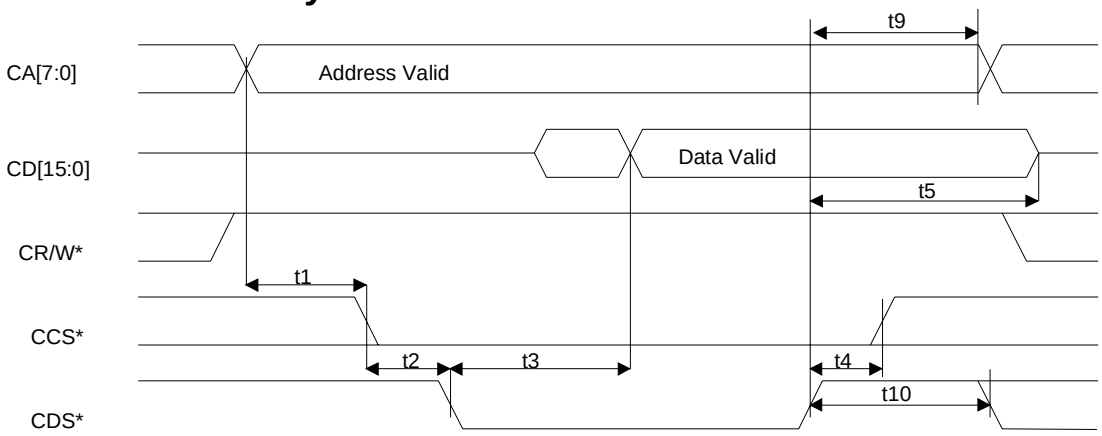
Intel Write Cycle



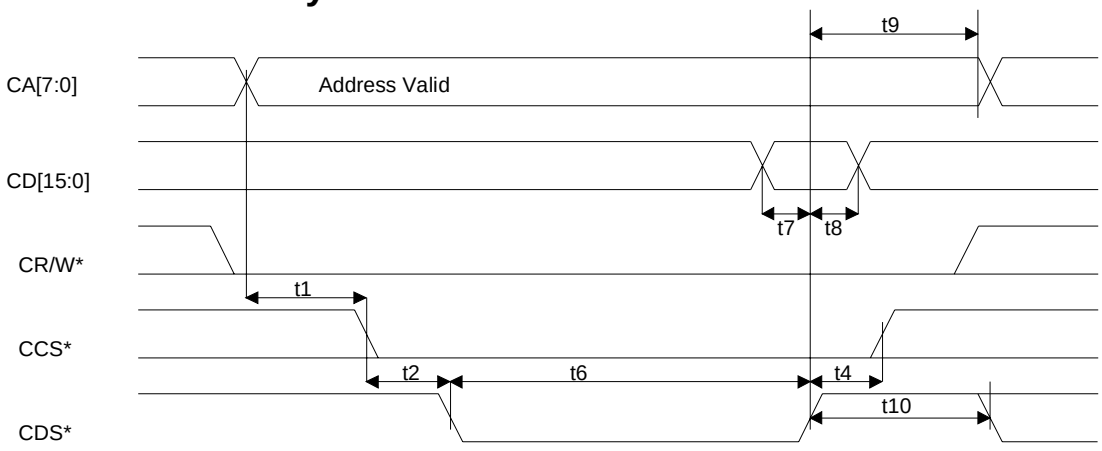
cpu_ac

CPU BUS AC TIMING DIAGRAM (non-multiplexed) Figure 12D Continued

Motorola Read Cycle



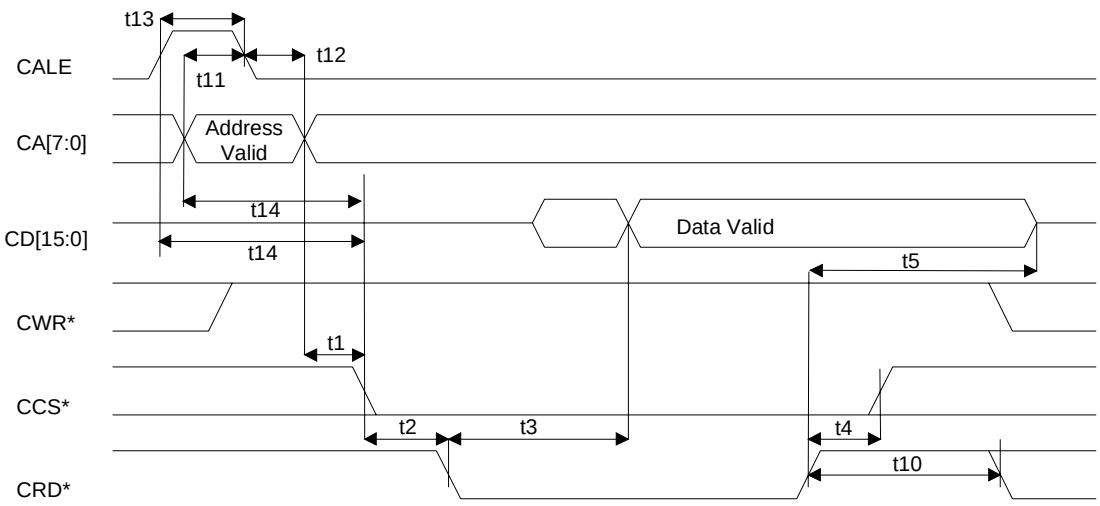
Motorola Write Cycle



cpu_ac

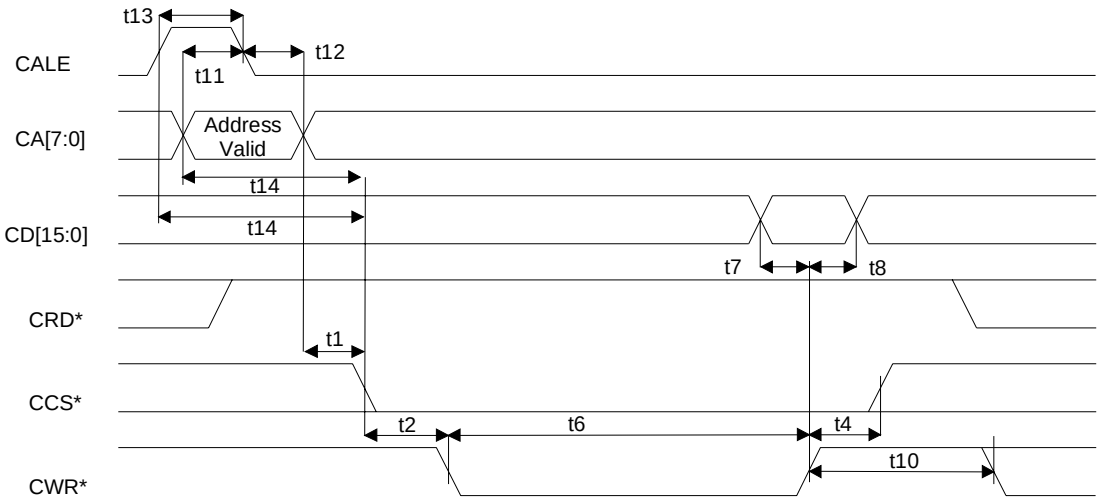
CPU BUS AC TIMING DIAGRAM (multiplexed) Figure 12E

Intel Read Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

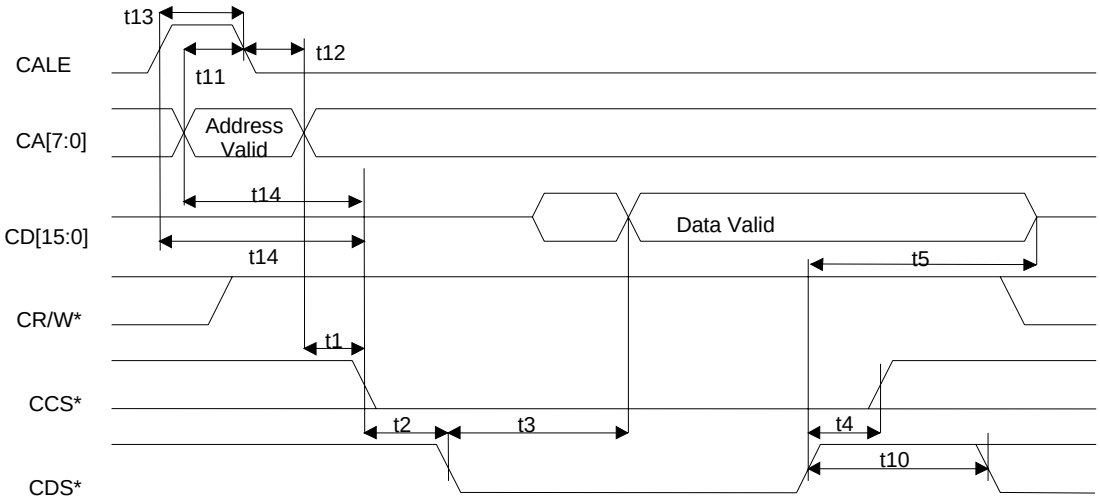
Intel Write Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

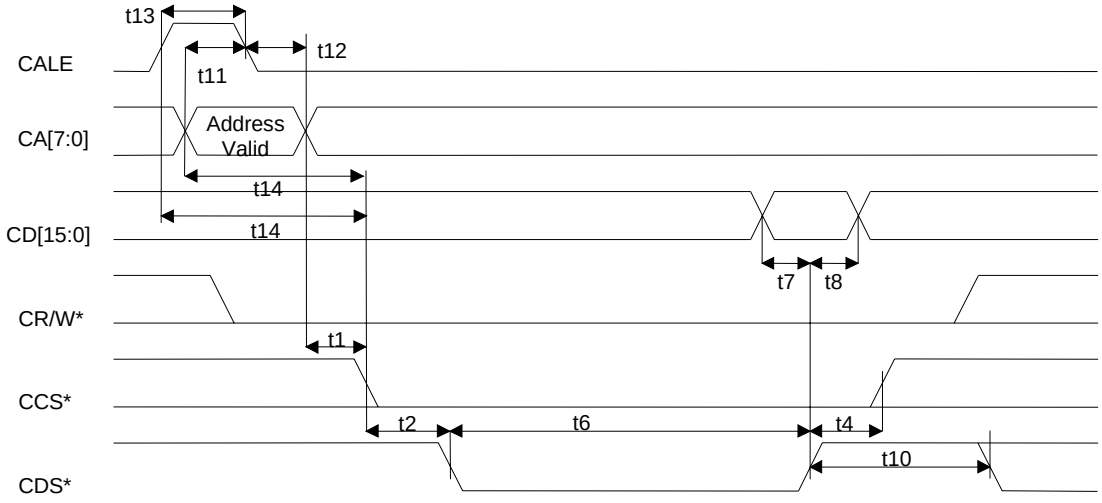
CPU BUS AC TIMING DIAGRAM (multiplexed) Figure 12E Continued

Motorola Read Cycle



Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

Motorola Write Cycle



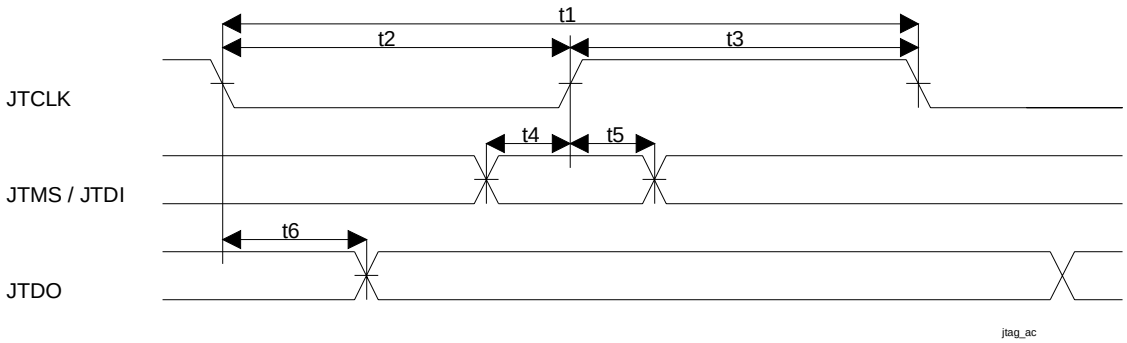
Note: t14 starts on the occurrence of either the rising edge of CALE or a valid address, whichever occurs first.

AC CHARACTERISTICS – JTAG TEST PORT INTERFACE

(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

Parameter	Symbol	Min	Typ	Max	Units	Notes
JTCLK Clock Period	t1	1000			ns	
JTCLK Clock Low Time	t2	400			ns	
JTCLK Clock High Time	t3	400			ns	
JTMS / JTDI Set Up Time to the Rising Edge of JTCLK	t4	50			ns	
JTMS / JTDI Hold Time from the Rising Edge of JTCLK	t5	50			ns	
Delay Time from the Falling Edge of JTCLK to Data Valid on JTDO	t6	2		50	ns	

JTAG TEST PORT INTERFACE AC TIMING DIAGRAM Figure 12F



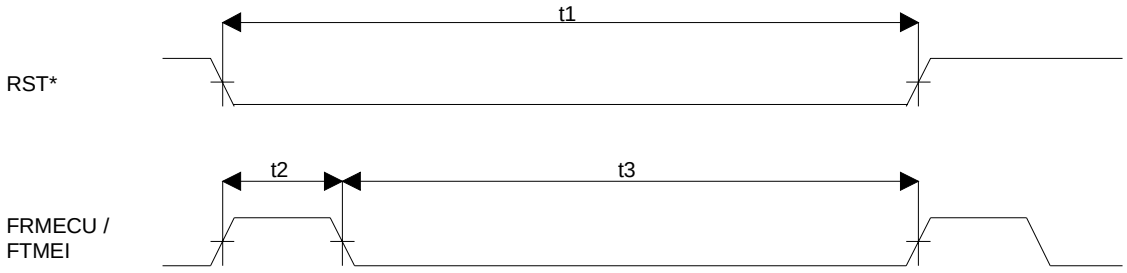
AC CHARACTERISTICS – RESET AND MANUAL ERROR COUNTER / INSERT SIGNALS

(0°C to 70°C; V_{DD} = 3.3V ± 5% for DS3112;
-40°C to +85°C; V_{DD} = 3.3V ± 5% for DS3112N)

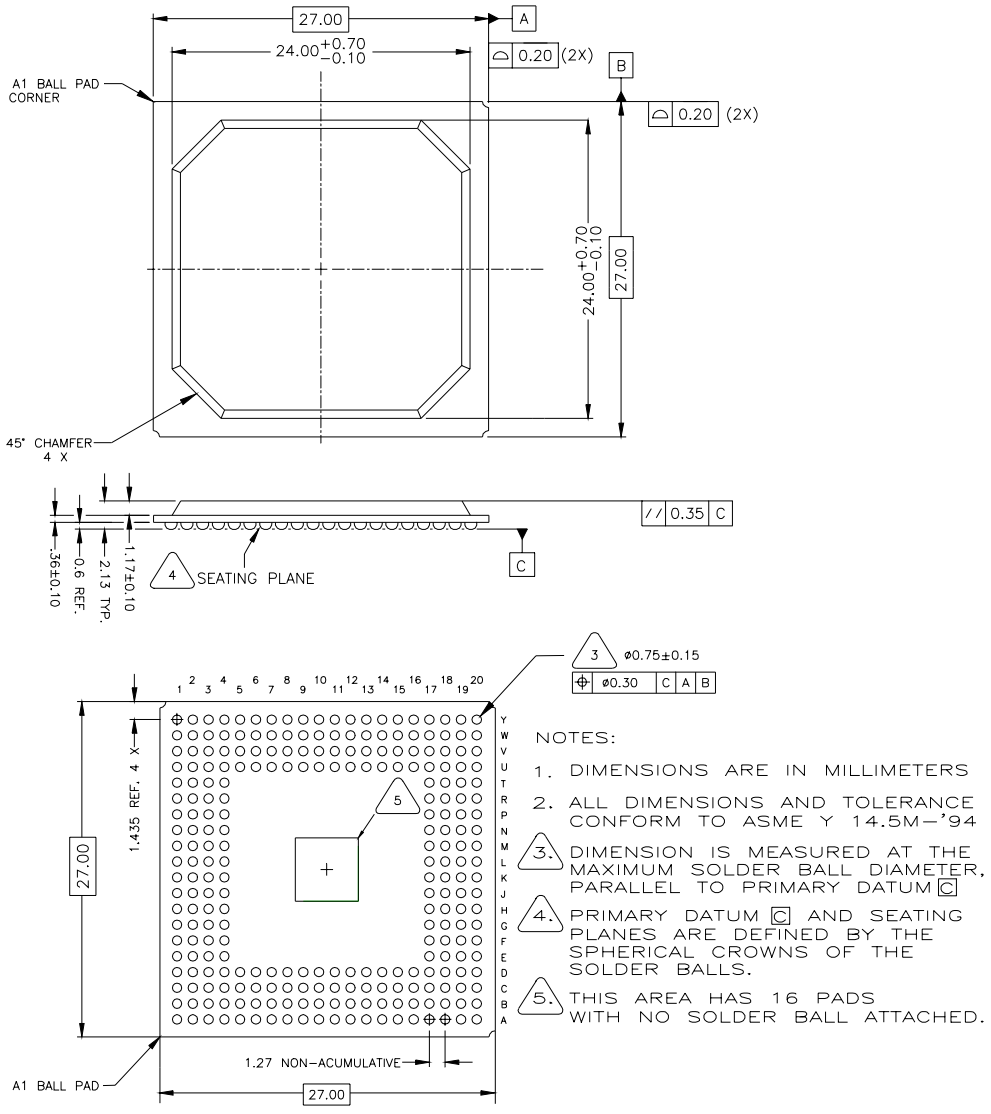
Parameter	Symbol	Min	Typ	Max	Units	Notes
RST* Low Time	t1	1000			ns	
FRMECU / FTMEI High Time	t2	50			ns	
FRMECU / FTMEI Low Time	t3	1000			ns	

RESET AND MANUAL ERROR COUNTER / INSERT AC TIMING DIAGRAM

Figure 12G



SECTION 13: MECHANICAL DIMENSIONS

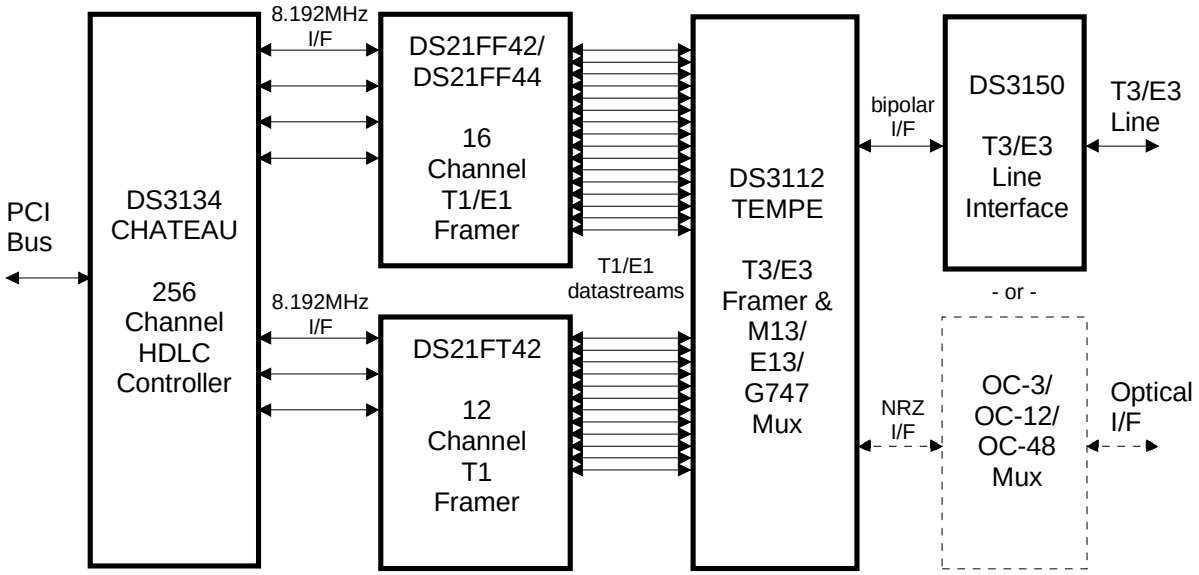


SECTION 14: APPLICATIONS AND STANDARDS OVERVIEW

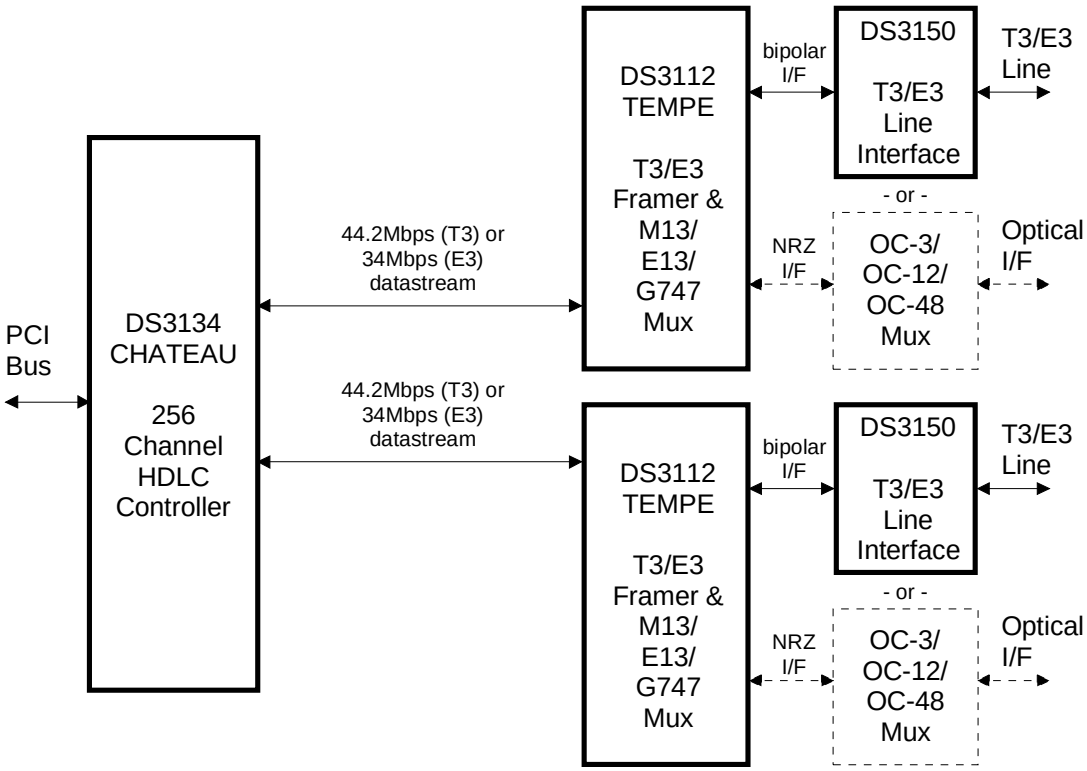
14.1 APPLICATION EXAMPLES

Figures 14.1A and 14.1B detail two possible applications of the DS3112. Figure 14.1A shows an example of a channelized T3/E3 application. It shows the DS3112 being used to multiplex and demultiplex a T3/E3 datastream into either 28 T1 datastreams or 16 E1 datastreams. The demultiplexed T1/E1 datastreams are fed into the DS21FF42/44 16 Channel T1/E1 Framer and the DS21FT42 12 Channel T1 Framer devices. The T1/E1 framers locate the frame boundaries and concatenate four T1/E1 datastreams into one 8.192 MHz datastream which is feed into the DS3134 HDLC controller. Figure 14.1B shows an example of a dual unchannelized T3/E3 application. In this application, the multiplexing capability of the DS3112 is disabled and it is only used as a T3/E3 framer.

Channelized T3/E3 Application Figure 14.1A



Unchannelized Dual T3/E3 Application Figure 14.1B



14.2 M13 BASICS

M13 multiplexing is the process of merging 28 T1 lines into a single T3 line. This is a two step process. First, four of the T1 lines are merged into a single T2 rate and then seven T2 rates are merged to form the T3. The first step of this process is called a M12 function since it is merging T1 lines into T2. The second step of this process is called a M23 function since it is merging T2 lines into a T3. The term M13 implies that both M12 and M23 are being performed to map 28 T1 lines into the T3. These two steps are independent and will be discussed separately.

T Carrier Rates Table 14.2A

T Carrier Level	Nominal Data Rate
T1 / DS1	1.544 Mbps
T2 / DS2	6.312 Mbps
T3 / DS3	44.736 Mbps

T2 Framing Structure

To understand the M12 function requires an understanding of T2 framing. The T2 frame structure is made up of four subframes called M subframes. See Figure 14.2A. The four M subframes are transmitted one after another (...M1/M2/M3/M4/M1/M2...) to make up the complete T2 M frame data structure. Each M subframe is made up of six blocks and each block is made up of 49 bits. The first bit of each block is dedicated to overhead and the next 48 bits are the information bits where the T1 data will be placed for transport. The definition of the overhead bits is shown in Table 14.2B and the placement of the overhead bits is shown in Figure 14.2A.

T2 Overhead Bit Assignments Table 14.2B

Overhead Bit	Description
M Bits (M1/M2/M3)	The M bits provide the frame alignment pattern for the four M subframes. Like all framing patterns, the M bits are fixed to a certain state (M1 = 0 / M2 = 1 / M3 = 1).
F Bits (F1/F2)	The F bits provide the frame alignment pattern for the M frame. Like all framing patterns, the F bits are fixed to a certain state (F1 = 0 / F2 = 1).
C Bits (C1/C2/C3)	In the M12 application, the C bits are used to indicate when stuffing occurs. If all three C Bits within a subframe are set to 1, then stuffing has occurred in the stuff block of that subframe. If all three C Bits are set to zero, then no stuffing has occurred. When the three C bits are not equal, a majority vote is used to determine the true state. The exception to this rule is when the C3 bit is the inverse of C1 and C2. When this occurs, it indicates that the T1 signal should be looped back.
X Bit	The X bit is used as a Remote Alarm Indication (RAI). It will be set to a zero (X = 0) when the T2 framer cannot synchronize. It will be set to a one (X = 1) otherwise.

M12 Multiplexing

The M12 function multiplexes four T1 lines into a single T2 line. Since there are four M subframes in the T2 framing structure, it might be concluded that each M subframe supports one T1 line but this is not the case. The four T1 lines are bit interleaved into the T2 framing structure. A bit from T1 line #1 is placed immediately after the overhead bit, followed by a bit from T1 line #2, which is followed by a bit from T1 line #3, which is followed by a bit from T1 line #4, and then the process repeats. Since there are 48 information bits in each block, there are 12 bits from each T1 line in a block. The second and fourth T1 lines are logically inverted before the bit interleaving occurs.

The four T1 lines are mapped asynchronously into the T2 data stream. This implies that there is no T1 framing information passed to the T2 level. The four T1 lines can have independent timing sources and they do not need to be timing locked to the T2 clock. To account for differences in timing, bit stuffing is used. The last block of each M subframe is the stuff block. See Figure 14.2A. In each stuff block there is an associated stuff bit (see Figure 14.2B) that will be either an information bit (if the three C bits are decoded to be a zero) or a stuff bit (if the three C bits are decoded to be a one). As shown in Figure 14.2B the position of the stuff bit varies depending on the M subframe. This is done to allow a stuffing opportunity to occur on each T1 line in every T2 M frame. For example, if the C Bits in M Subframe 2 were all set to one, then the second bit after the F2 overhead bit in the last block would be a stuff bit instead of an information bit.

T2 M-Frame Structure Figure 14.2A

M1 Subframe Stuff Block

M1 (0)	48 Info Bits	C1	48 Info Bits	F1 (0)	48 Info Bits	C2	48 Info Bits	C3	48 Info Bits	F2 (1)	48 Info Bits

M2 Subframe Stuff Block

M2 (1)	48 Info Bits	C1	48 Info Bits	F1 (0)	48 Info Bits	C2	48 Info Bits	C3	48 Info Bits	F2 (1)	48 Info Bits

M3 Subframe Stuff Block

M3 (1)	48 Info Bits	C1	48 Info Bits	F1 (0)	48 Info Bits	C2	48 Info Bits	C3	48 Info Bits	F2 (1)	48 Info Bits

M4 Subframe Stuff Block

X	48 Info Bits	C1	48 Info Bits	F1 (0)	48 Info Bits	C2	48 Info Bits	C3	48 Info Bits	F2 (1)	48 Info Bits

Note: M1 is transmitted and received first.

T2 Stuff Block Structure Figure 14.2B

M1 Subframe	F2	Stuff Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	.....	Info Bit 48
M2 Subframe	F2	Info Bit 1	Stuff Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	.....	Info Bit 48
M3 Subframe	F2	Info Bit 1	Info Bit 2	Stuff Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	.....	Info Bit 48
M4 Subframe	F2	Info Bit 1	Info Bit 2	Info Bit 3	Stuff Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	.....	Info Bit 48

T3 Framing Structure

As with M12, to understand the M23 function requires an understanding of T3 framing. The T3 frame structure is very similar to the T2 frame structure however it is made up of seven M subframes. See Figure 14.2C. The seven M subframes are transmitted one after another (...M1/M2/M3/.../ M6/M7M1/M2...) to make up the complete T3 M frame structure. Each M subframe is made up of eight blocks and each block is made up of 85 bits. The first bit of each block is dedicated to overhead and the next 84 bits are the information bits where the T2 data will be placed for transport. The definition of the overhead bits is shown in Table 14.2C and the placement of the overhead bits is shown in Figure 14.2C.

T3 Overhead Bit Assignments Table 14.2C

Overhead Bit	Description
M Bits (M1/M2/M3)	The M bits provide the frame alignment pattern for the seven M subframes. Like all framing patterns, the M bits are fixed to a certain state (M1 = 0 / M2 = 1 / M3 = 0).
F Bits (F1/F2/F3/F4)	The F bits provide the frame alignment pattern for the M frame. Like all framing patterns, the F bits are fixed to a certain state (F1 = 1 / F2 = 0 / F3 = 0 / F4 = 1).
C Bits (C1/C2/C3)	In the M23 application, the C bits are used to indicate when stuffing occurs. If all three C Bits within a subframe are set to 1, then stuffing has occurred in the stuff block of that subframe. If all three C Bits are set to zero, then no stuffing has occurred. When the three C bits are not equal, a majority vote is used to determine the true state. In the C-Bit Parity application, the C bits are defined as shown in Table 14.2D.
P Bits (P1/P2)	The P bits provide parity information for the preceding M frame (not including the M, F, X, and C overhead bits). P1 and P2 are always the same value (if they are not the same value, this implies a parity error).
X Bits (X1/X2)	The X bit is used as a Remote Alarm Indication (RAI). It will be set to a zero (X1 = X2 = 0) when the T3 framer cannot synchronize or detects AIS. It will be set to a one (X1 = X2 = 1) otherwise. The value of the X bits should not change more than once per second. X1 and X2 are always the same value.

M23 Multiplexing

The M23 function multiplexes seven T2 data streams into a single T3 data stream. The seven T2 data streams are bit interleaved into the T3 framing structure. A bit from T2 line #1 is placed immediately after the overhead bit in the information bit field, followed by a bit from T2 line #2, and so on. Since there are 84 information bits in each block, there are 12 bits from each T2 line in a block.

The seven T2 lines are mapped asynchronously into the T3 data stream. This implies that there is no T2 framing information passed to the T3 level. The seven T2 lines can have independent timing sources and they do not need to be timing locked to the T3 clock. To account for differences in timing, bit stuffing is used. The last block of each M subframe is the stuff block. See Figure 14.2C. In each stuff block there is an associated stuff bit (see Figure 14.2D) that will be either an information bit (if the three C bits are decoded to be zero) or a stuff bit (if the three C bits are decoded to be a one). As shown in Figure 14.2D, the position of the stuff bit varies depending on the M subframe. This is done to allow a stuffing opportunity to occur on each T2 line in every T3 frame. For example, if the C Bits in M Subframe 5 were all set to one, then the fifth bit after the F4 overhead bit in the last block would be a stuff bit instead of an information bit.

C-Bit Parity Mode

Unlike the M23 application which uses the C bits for stuffing, the C-bit Parity Mode assumes that a stuff bit should be placed at every opportunity and hence the C bits can be used for other purposes. See Table 14.2D for a list of how the C bits are redefined in the C-Bit Parity Mode.

C Bit Assignment for C-Bit Parity Mode Table 14.2D

M Subframe Number	C Bit Number	Function	Description
1	1	**Application ID**	This bit (which is fixed to a value of 1) identifies the T3 data stream as operating in C-Bit Parity Mode.
	2	**Reserved**	Must be set to one (1).
	3	**Far End Alarm and Control (FEAC)**	A serial communications channel that contains a repeating 16-bit codeword that indicates the state of the far-end and can control the near-end by invoking loopbacks both on the T3 and T1 lines. If no codewords are being sent, the channel contains all ones.
2	1 2 3	**Unused** **Unused** **Unused**	All unused bits are set to a one (1).
3	1 2 3	**C-Bit Parity (CP)** **C-Bit Parity (CP)** **C-Bit Parity (CP)**	All three CP bits are set to the same value as the two P bits. If the three CP bits are not equal, a majority vote is used to decode the true value.
4	1 2 3	**FEBE** **FEBE** **FEBE**	All three Far End Block Error (FEBE) bits shall be set to one (111) if the local T3 framer did not incur an error in either the M bits or F bits nor has it detected a CP parity error. The FEBE bits are set to any value except 111 when an error is detected in the M bits or F bits or if a CP parity error is detected. During an LOF event, these bits are set to 000.
5	1 2 3	**Data Link** **Data Link** **Data Link**	These three C bits make up a 28.2 kbps HDLC (LAPD) maintenance data link over which three 76 octet messages are sent from the local end to the remote end once a second.
6	1 2 3	**Unused** **Unused** **Unused**	Must be set to 1. Must be set to 1. Must be set to 1.
7	1 2 3	**Unused** **Unused** **Unused**	Must be set to 1. Must be set to 1. Must be set to 1.

T3 M-Frame Structure Figure 14.2C

M1 Subframe **Stuff Block**

X1	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M2 Subframe **Stuff Block**

X2	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M3 Subframe **Stuff Block**

P1	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M4 Subframe **Stuff Block**

P2	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M5 Subframe **Stuff Block**

M1 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M6 Subframe **Stuff Block**

M2 (1)	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

M7 Subframe **Stuff Block**

M3 (0)	84 Info Bits	F1 (1)	84 Info Bits	C1	84 Info Bits	F2 (0)	84 Info Bits	C2	84 Info Bits	F3 (0)	84 Info Bits	C3	84 Info Bits	F4 (1)	84 Info Bits

Note: X1 is transmitted and received first.

T3 Stuff Block Structure Figure 14.2D

M1 Subframe	F4	**Stuff Bit 1**	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	..... Info Bit 84
M2 Subframe	F4	Info Bit 1	**Stuff Bit 2**	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	..... Info Bit 84
M3 Subframe	F4	Info Bit 1	Info Bit 2	**Stuff Bit 3**	Info Bit 4	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	..... Info Bit 84
M4 Subframe	F4	Info Bit 1	Info Bit 2	Info Bit 3	**Stuff Bit 4**	Info Bit 5	Info Bit 6	Info Bit 7	Info Bit 8	..... Info Bit 84
M5 Subframe	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	**Stuff Bit 5**	Info Bit 6	Info Bit 7	Info Bit 8	..... Info Bit 84
M6 Subframe	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	**Stuff Bit 6**	Info Bit 7	Info Bit 8	..... Info Bit 84
M7 Subframe	F4	Info Bit 1	Info Bit 2	Info Bit 3	Info Bit 4	Info Bit 5	Info Bit 6	**Stuff Bit 7**	Info Bit 8	..... Info Bit 84

14.3 E13 BASICS

E13 multiplexing is the process of merging 16 E1 lines into a single E3 line. This is a two step process. First, four of the E1 lines are merged into a single E2 rate and then four E2 rates are merged to form the E3. The first step of this process is called a E12 function since it is merging E1 lines into E2. The second step of this process is called a E23 function since it is merging E2 lines into a E3. The term E13 implies that both E12 and E23 are being performed to map 16 E1 lines into the E3. These two steps are independent and will be discussed separately.

E Carrier Rates Table 14.3A

E Carrier Level	Nominal Data Rate
E1	2.048 Mbps
E2	8.448 Mbps
E3	34.368 Mbps

E2 Framing Structure and E12 Multiplexing

The E2 frame structure is made up of four 212 bit Sets. See Figure 14.3A. The four Sets are transmitted one after another (...Set1/Set2/Set3/Set4/Set1...) to make up the complete E2 frame structure. The Frame Alignment Signal (FAS) is placed in the first 10 bits of Set 1 and is followed by the Remote Alarm Indication (RAI) bit and a National Bit (Sn). The remainder of Set 1 is filled with bits from the four tributaries. The four tributaries are bit interleaved starting with a bit from Tributary 1 immediately after the Sn bit. The first four bits of Sets 2, 3, and 4 are the Justification Control Bits. Bits 5 to 8 of Set 4 are the Stuffing Bits. The Justification Control bits control when data will be stuffed into the Stuffing Bit

positions. When a majority of the three Justification Control Bits from a particular tributary is set to zero, the Stuffing Bit position will be used for tributary data. When the Justification Control Bits are majority decoded to be one, the Stuffing Bit will not be used for tributary data.

E3 Framing Structure and E23 Multiplexing

The E3 frame structure and the E23 multiplexing scheme is almost identical to the E2 framing structure and the E12 multiplexing scheme. The E3 frame structure is made up of four 384 bit Sets. See Figure 14.3B. The four Sets are transmitted one after another (...Set1/Set2/Set3/Set4/Set1...) to make up the complete E3 frame structure. The Frame Alignment Signal (FAS) is placed in the first 10 bits of Set 1 and is followed by the Remote Alarm Indication (RAI) bit and a National Bit (Sn). The remainder of Set 1 is filled with bits from the four tributaries. The four tributaries are bit interleaved starting with a bit from Tributary 1 immediately after the Sn bit. The first four bits of Sets 2, 3, and 4 are the Justification Control Bits. Bits 5 to 8 of Set 4 are the Stuffing Bits. The Justification Control bits control when data will be stuffed into the Stuffing Bit positions. When a majority of the three Justification Control Bits from a particular tributary is set to zero, the Stuffing Bit position will be used for tributary data. When the Justification Control Bits are majority decoded to be one, the Stuffing Bit will not be used for tributary data.

E2 Frame Structure Figure 14.3A

Set 1

Bit 1 Bit 212

FAS (1111010000)	RAI	Sn	b_{11}	b_{21}	b_{31}	b_{41}	b_{12}	...bits from the tributaries...

Set 2

Bit 1 Bit 212

c_{11}	c_{21}	c_{31}	c_{41}	...bits from the tributaries...

Set 3

Bit 1 Bit 212

c_{12}	c_{22}	c_{32}	c_{42}	...bits from the tributaries...

Set 4

Bit 1 Bit 212

c_{13}	c_{23}	c_{33}	c_{43}	s_1	s_2	s_3	s_4	...bits from the tributaries...

Notes:

1. bit 1 of set 1 is transmitted first
2. bji tributary bits j = tributary number i = bit number
3. cji justification control bits j = tributary number i = control bit number
4. sj stuffing bits j = tributary number

E3 Frame Structure Figure 14.3B

Set 1

Bit 1 Bit 384

FAS (1111010000)	RAI	Sn	b_{11}	b_{21}	b_{31}	b_{41}	b_{12}	...bits from the tributaries...

Set 2

Bit 1 Bit 384

c_{11}	c_{21}	c_{31}	c_{41}	...bits from the tributaries...

Set 3

Bit 1 Bit 384

c_{12}	c_{22}	c_{32}	c_{42}	...bits from the tributaries...

Set 4

Bit 1 Bit 384

c_{12}	c_{22}	c_{32}	c_{42}	s_1	s_2	s_3	s_4	...bits from the tributaries...

Notes:

1. bit 1 of set 1 is transmitted first
2. bji tributary bits j = tributary number i = bit number
3. cji justification control bits j = tributary number i = control stuffing bit number
4. sj stuffing bits j = tributary number

14.4 G.747 BASICS

G.747 multiplexing is a mixture of T3 and E1. It is the process of merging 21 E1 lines into a single T3 line. This is a two step process. First, three of the E1 lines are merged into a single T2 rate and then seven T2 rates are merged to form the T3 just like the normal T2 to T3 multiplexing scheme. Once the three E1 lines have been multiplexed together, the resultant 6.312 Mbps data stream is treated just like a T2 data stream that contains four T1 lines. We will only discuss the G.747 multiplexing scheme in this Section. See Section 14.2 for details on the T2 to T3 multiplexing scheme (i.e. M23) and the T3 framing structure.

G.747 Carrier Rates Table 14.4A

T or E Carrier Level	Nominal Data Rate
E1	2.048 Mbps
T2	6.312 Mbps
T3	44.736 Mbps

G.747 Framing Structure and E12 Multiplexing

The G.747 frame structure is made up of five 168 bit Sets. See Figure 14.4A. The five Sets are transmitted one after another (...Set1/Set2/Set3/Set4/Set5/Set1...) to make up the complete G.747 frame structure. The Frame Alignment Signal (FAS) is placed in the first 9 bits of Set 1. Set 2 contains the Remote Alarm Indication (RAI) bit and a Parity Bit (PAR) as well as a reserved bit which is fixed to a one. The PAR bit will be set to a one when there are odd number of ones from the tributaries in the preceding frame and it will be set to a zero when there are an even number of ones. The parity calculation does not include the FAS, RAI, reserved bit, or Justification Control Bits. The three tributaries are bit interleaved starting with a bit from Tributary 1 immediately after the FAS in Set 1. The first three bits of Sets 3, 4, and 5 are the Justification Control Bits. Bits 4 to 6 of Set 5 are the Stuffing Bits. The Justification Control bits control when data will be stuffed into the Stuffing Bit positions. When a majority of the three Justification Control Bits from a particular tributary is set to zero, the Stuffing Bit position will be used for tributary data. When the Justification Control Bits are majority decoded to be one, the Stuffing Bit will not be used for tributary data.

G.747 Frame Structure Figure 14.4A

Set 1

Bit 1 Bit 168

FAS (111010000)	b_{11}	b_{21}	b_{31}	b_{12}	b_{22}	b_{32}	b_{13}	...bits from the tributaries...

Set 2

Bit 1 Bit 168

RAI	PAR	1	...bits from the tributaries...

Set 3

Bit 1 Bit 168

c_{11}	c_{21}	c_{31}	...bits from the tributaries...

Set 4

Bit 1 Bit 168

c_{12}	c_{22}	c_{32}	...bits from the tributaries...

Set 5

Bit 1 Bit 168

c_{13}	c_{23}	c_{33}	s_1	s_2	s_3	...bits from the tributaries...

Notes:

1. bit 1 of set 1 is transmitted first
2. bji tributary bits j = tributary number i = bit number
3. cji justification control bits j = tributary number i = control stuffing bit number
4. sj stuffing bits j = tributary number