VP310

Satellite Channel Demodulator

Preliminary Information

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Ordering Information
VP310 CG GQ1N

The VP310 is a QPSK/BPSK 1 to 45 MBaud demodulator and channel decoder for digital satellite television transmissions to the European Broadcast Union ETS 300 421 specification. It receives analog I and Q signals from the tuner, digitises and digitally demodulates the signals, and implements the complete DVB/DSS FEC (Forward Error Correction), and de-scrambling function. The output is in the form of MPEG2 or DSS transport stream data packets. The VP310 also provides automatic gain control to the RF front-end devices.

The VP310 has a serial I^2C port interface to the control microprocessor. Minimal software is required to control the VP310 because of the built in automatic search and decode control functions.

Applications

- DVB 1 to 45 MBaud compliant satellite receivers
- DSS 20 MBaud compliant satellite receivers
- SCPC receivers (Single Channel Per Carrier)
- SMATV trans-modulators (Single Master Antenna TV)
- LMDS (Local Multipoint Distribution Service)
- Satellite PC applications

Key Features

- Conforms to EBU specification for DVB-S and DirecTV specification for DSS
- On-chip digital filtering supports 1 to 45 MBaud Symbol rates
- On-chip 6-bit 60 or 90 MHz dual-ADC
- High speed scanning mode for blind symbol rate and code rate acquisition
- Up to ± 15 MHz LNB frequency tracking
- Fully digital timing and phase recovery loops
- High level software interface for minimum development time
- DiSEqC™ v1.1: control outputs for full control of LNB and dish

Additional Features

- I^2C bus microprocessor interface
- All digital clock and carrier recovery
- On-chip PLL clock generation using low cost 10 to 15 MHz crystal
- 3.3V operation
- 80 pin MQFP package
- Low external component count
- Commercial temperature range 0 to 70°C

Demodulator

- BPSK or QPSK programmable

Viterbi

- Programmable decoder rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8
- Constraint length k=7
- Trace back depth 128
- Extensive SNR and BER monitors

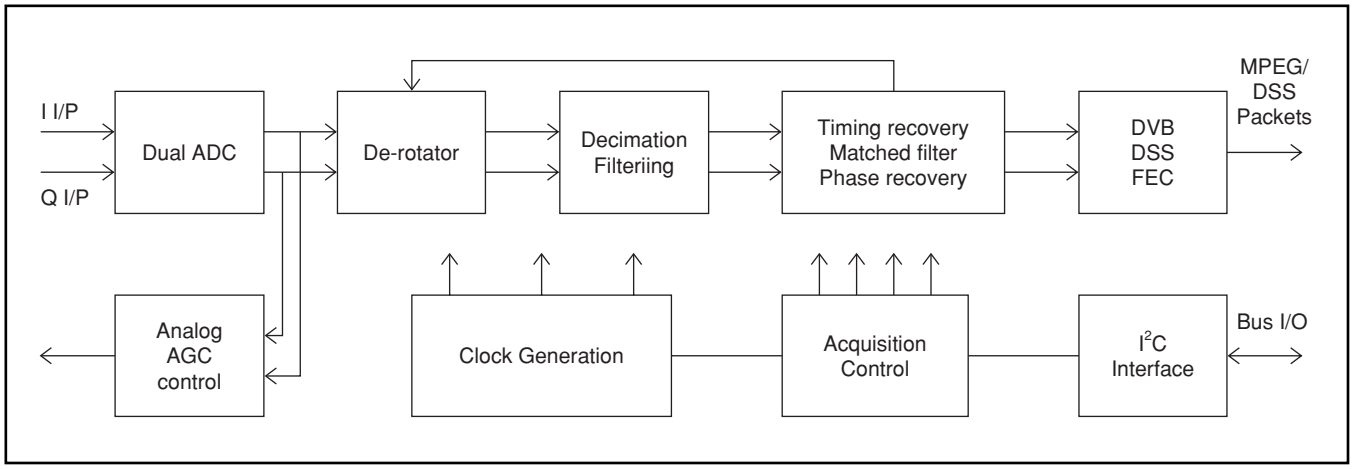

Figure 1 - VP310 Functional Block Diagram

Additional Features (continued)

De-Interleaver
- Compliant with DVB and DSS standards

Reed Solomon
- (204, 188) for DVB and (146,130) for DSS
- Reed Solomon Bit-error-rate monitor to indicate Viterbi performance

De-Scrambler
- EBU specification De-scrambler for DVB mode

Outputs
- MPEG transport parallel & serial output
- Integrated MPEG2 TEI bit processing for DVB only

Application Support
- Channel decoder system evaluation board
- I^2C interface board to PC
- Windows based evaluation software
- ANSI C generic software
- Application support help desk via email/ telephone

Digital Video Broadcasting

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www.zarlink.com