SP8855E

2.8GHz Parallel Load Professional Synthesiser

Advance Information

DS4239 ISSUE 3.0 March 1999

The SP8855E is one of a family of parallel load synthesisers containing all the elements apart from the loop amplifier to fabricate a PLL synthesis loop. Other devices in the series are the SP8852E which is a fully programmable device requiring two 16 bit words to set the RF and reference counters, and the SP8854E which has hard wired reference counter programming and requires a single bit word to program the RF divider. The SP8855E replaces the existing SP8855D.

The SP8855E is intended for applications where a fixed synthesiser frequency is required although it can also be used where frequency selection is set by switches. In general the device will be programmed by connecting the programming pins to either V_{CC} or ground. Additional hard wired inputs can be used to control the F_{pd} and F_{ref} outputs set the control direction of the loop and select the phase detector gain. Another input may be used to disable the phase detector output.

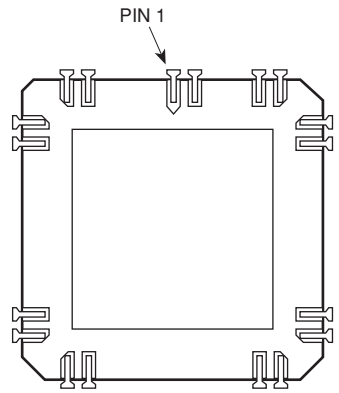
The device is available in both plastic (HP) and ceramic (HC) J-leaded 44-lead chip carrier. Ambient temperature ranges available are shown in the ordering information.

Features

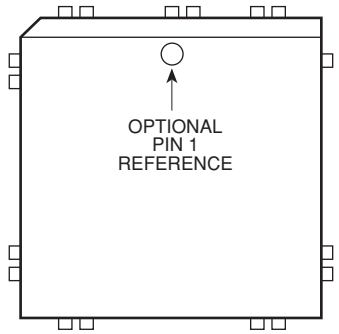
- 2.8GHz Operating Frequency (IG GRADE)
- Single 5V Supply Operation
- High Comparison Frequency 50MHz
- High Gain Phase Detector 1mA/rad
- Programmable Phase Detector Gain
- Zero "Dead Band" Phase Detector
- Wide range of RF and Reference Divide Ratios
- Programming by Hard Wired Inputs
- Low cost plastic package option
- GPS HI-REL level a screened option

Absolute Maximum Ratings

Supply voltage	-0.3V to 6V
Storage temperature	-65 °C to +150°C
Operating temperature	-55°C to +100°C
Prescaler & reference Input Voltage	2.5V p-p
Data Inputs	V_{CC} +0.3V
	V_{EE} -0.3V
Junction temperature	+ 175°C (HC package)
	+ 150°C (HP package)



HC44



HP44

Pin	Description	Pin	Description
1	Input bus bit 10	23	Control Direction
2	Input bus bit 9	24	F_{pd*}
3	Input bus bit 8	25	F_{ref*}
4	Input bus bit 7	26	+5V
5	Input bus bit 6	27	Ref. osc capacitor
6	Input bus bit 5	28	Ref in/XTAL
7	Input bus bit 4	29	Reference bit 9
8	Input bus bit 3	30	Reference bit 8
9	Input bus bit 2	31	Reference bit 7
10	Input bus bit 1	32	Reference bit 6
11	Input bus bit 0	33	Reference bit 5
12	0V (prescaler)	34	Reference bit 4
13	RF input	35	Reference bit 3
14	RF input	36	Reference bit 2
15	V_{CC} + 5V (prescaler)	37	Reference bit 1
16	V_{EE} 0V	38	Reference bit 0
17	Lock detect output	39	Phase Detect Enable
18	C-lock detect	40	Phase Detect Gain 1
19	Rset	41	Phase Detect Gain 0
20	Charge pump output	42	Input bus bit 13
21	Charge pump ref.	43	Input bus bit 12
22	F_{ref}/F_{pd} enable	44	Input bus bit 11

*Fpd and Fref outputs are reversed using the Control Direction input. The table above is correct when pin 23 is high.

Figure 1 - Pin connections - top view

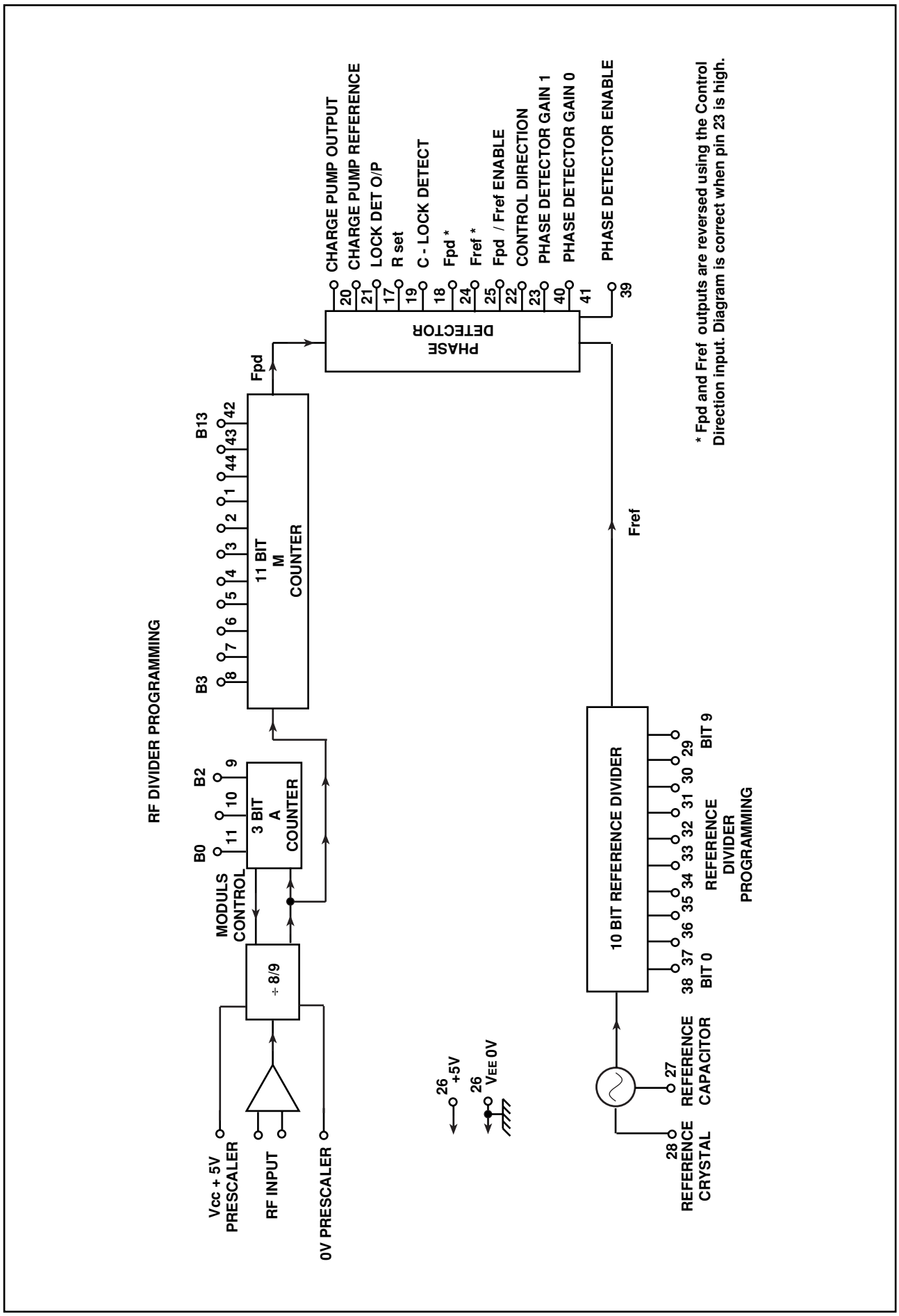


Figure 2 - SP8855E block diagram

PIN Description

PIN	Description
1,2,3,4,5,6,7,8,9,10,11,42,43,44	These pins are the data inputs used to set the RF divider ratio (M.N+A). Open circuit = 1 (high) on these pins. Inputs are transparent into the data buffers.
13, 14 (RF INPUT)	Balanced inputs to the RF pre-amplifier. For single ended operation the signal is AC coupled into pin 13 with pin 14 AC decoupled to ground (or vice -versa). Pins 13 and 14 are internally DC biased.
17 (LOCK DETECT INPUT)	A current sink into this pin is enabled when the lock detect circuit indicates lock. Used to give an external indication of phase lock.
18 (C-LOCK DETECT)	A capacitor connected to this point determines the lock detect integrator time constant and can be used to vary the sensitivity of the phase lock indicator.
19 (Rset)	An external resistor from Pin 19 to V_{CC} sets the charge pump output current
20 (CP OUTPUT)	The phase detector output is a single ended charge pump sourcing or sinking current to the inverting input of an external loop filter.
21 (CP REF)	Connected to the non-inverting input of the loop filter to set the optimum DC bias.
22 (F_{ref}/F_{pd} ENABLE	Part of the data input bus. When this pin is logic HI the F_{ref} and F_{pd} outputs are enabled. Open circuit = HI
23 (CONTROL DIRECTION)	This pin controls charge pump output direction. For Pin 23 HI the output sinks current when $F_{pd} > F_{ref}$ or when the RF phase leads Ref phase. For Pin 23 LO the relationship is reversed. (see table 2). Changing the state of pin 23 reverses the pins on which Fref and Fpd output occur. See pin 24 and Pin 25 below for details. Open circuit = HI.
24 = F_{pd} if Pin 23 is HI = F_{ref} if Pin 23 is LO	RF divider output pulses. Fpd = RF input frequency /(M.N+A). Pulse width = 8 RF input cycles (1 cycle of the divide by 8 prescaler output).
25 = F_{ref} if Pin 223 is HI	Reference divider output pulses. Fref = Reference input frequency/R. Pulse width = high period of Ref input.
27 (Reference Oscillator Capacitor)	Leave open circuit if an external reference is used. See fig. 5 for typical connection for use as an onboard crystal oscillator.
28 (Ref IN/XTAL)	This pin is the input buffer amplifier for an external reference signal. This amplifier provides the active element if an onboard crystal oscillator is used.
29,30,31,32,33,34,35,36,37,38	These pins set the Reference divider ratio R. Open circuit = HI.
39 (Phase Detector ENABLE)	When this pin is HI the phase detector output is enable. Open circuit = HI.
40, 41 (PD Gain)	These pins set the charge pump current multiplication factor (see table 1). Open circuit = HI.

Electrical Characteristics

Guaranteed over the full temperature and supply voltage range (unless otherwise stated)
Temperature T_{amb} for KG parts -55°C and +100°C, Temperature T_{amb} for IG parts -40°C and +85°, Temperature T_{case} for MA part -55°C and +125°C Supply Voltage = 4.75V and 5.25V

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current15, 26		180	240	mA		
RF input sensitivity	13, 14	-5.0		+7.0	dBm	100MHz to 2.8/2.7GHz See Fig. 3
RF division ratio	13,14,24	56		16383		
Reference division ratio	28, 25	1		1023		
Comparison frequency	28,24,25			50	MHz	
Reference input frequency	28	10		100	MHz	Reference division ratio ≥ 2 at frequencies >50MHz also see Note 1.
Reference input voltage	28	630	1200	2000	mV p-p	Sine Wave 10-100MHz
F_{ref}/F_{pd} output voltage high	24, 25		- 0.8		Vwrt V_{CC}	2.2K to 0V
F_{red}/F_{pd} output voltage low	24, 25		- 1.4		Vwrt V_{CC}	2.2K to 0V
Lock detect output voltage	17		300	500	mV	I_{OUT} = 3mA
Charge pump current at multiplication factor = 1	19,20,21	±1.4	±1.5	±1.7	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 1.5	19,20,21	±2.0	±2.3	±2.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 2.5	19,20,21	±3.4	±3.8	±4.6	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 4.0	19,20,21	±5.4	±6.1	±6.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Input bus high logic level	1-11, 22 23, 29-44	3.5			V	
Input bus low logic level	1-11, 22 23,29-44			1	V	
Input bus current source	1-11,22 23,29-44	-200			µA	V_{IN} = 0V
Input bys current sink	1-11, 22 23,29-44			10	µA	$V_{IN} = V_{CC}$
Up down current matching	20			±5	%	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump reference voltage	21			V_{CC}-0.5	V	$I_{pin\ 19}$ =1.6mA current multiplication factor = 1
Charge pump reference voltage	21	V_{CC}-1.6			V	$I_{pin\ 19}$ =1.6mA current multiplication factor = 4
R_{set} current	19	0.5		2	mA	See Note 2
R_{set} Voltage 19		1.6		V		$I_{pin\ 19}$ = 1.6mA

Notes: 1. Lower reference frequencies may be used if slew rates are maintained.
2. Pin 19 current x multiplication factor must be less than 5mA if charge pump accuracy is to be maintained.

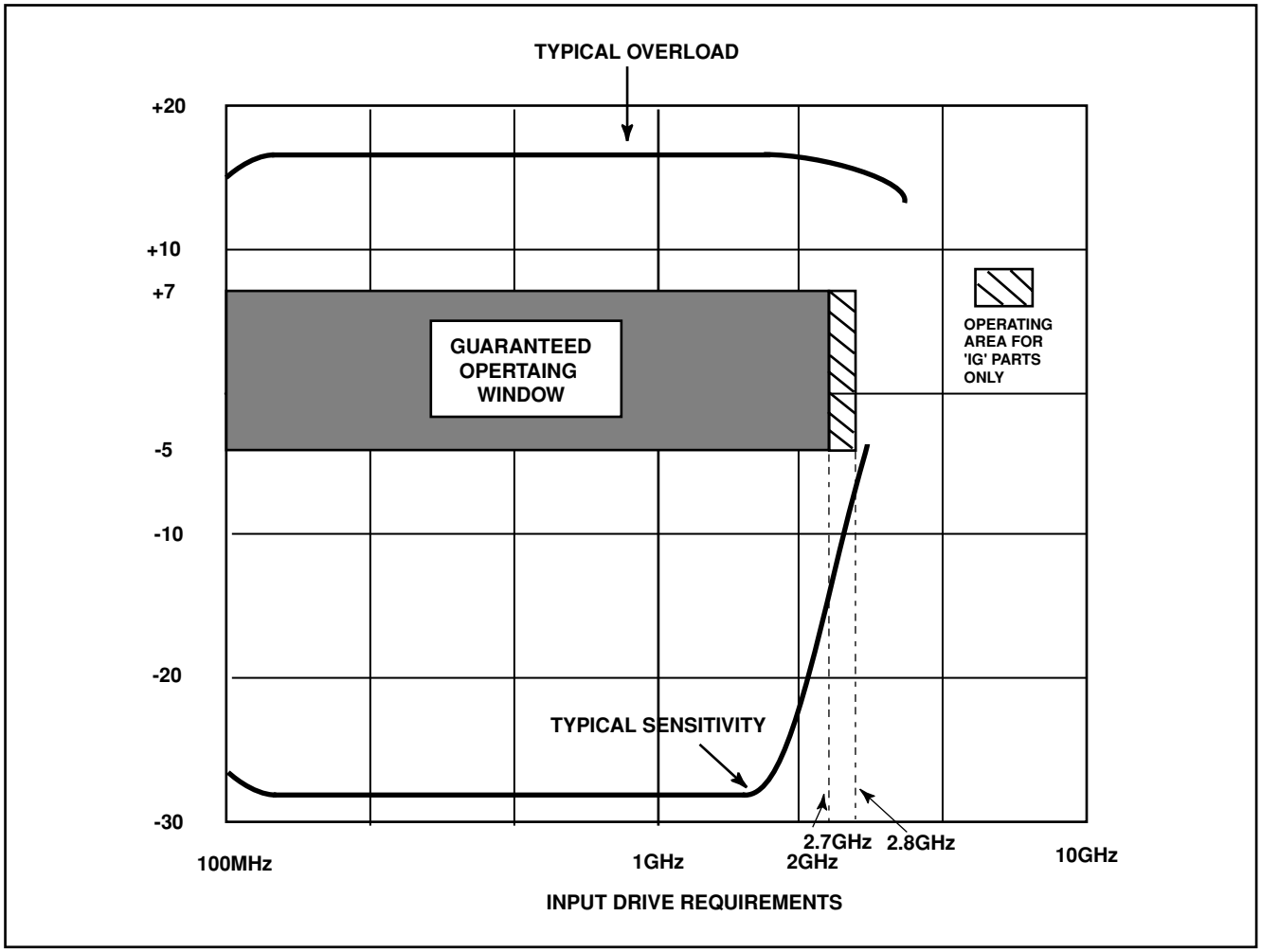


Figure 3 - SP8855E

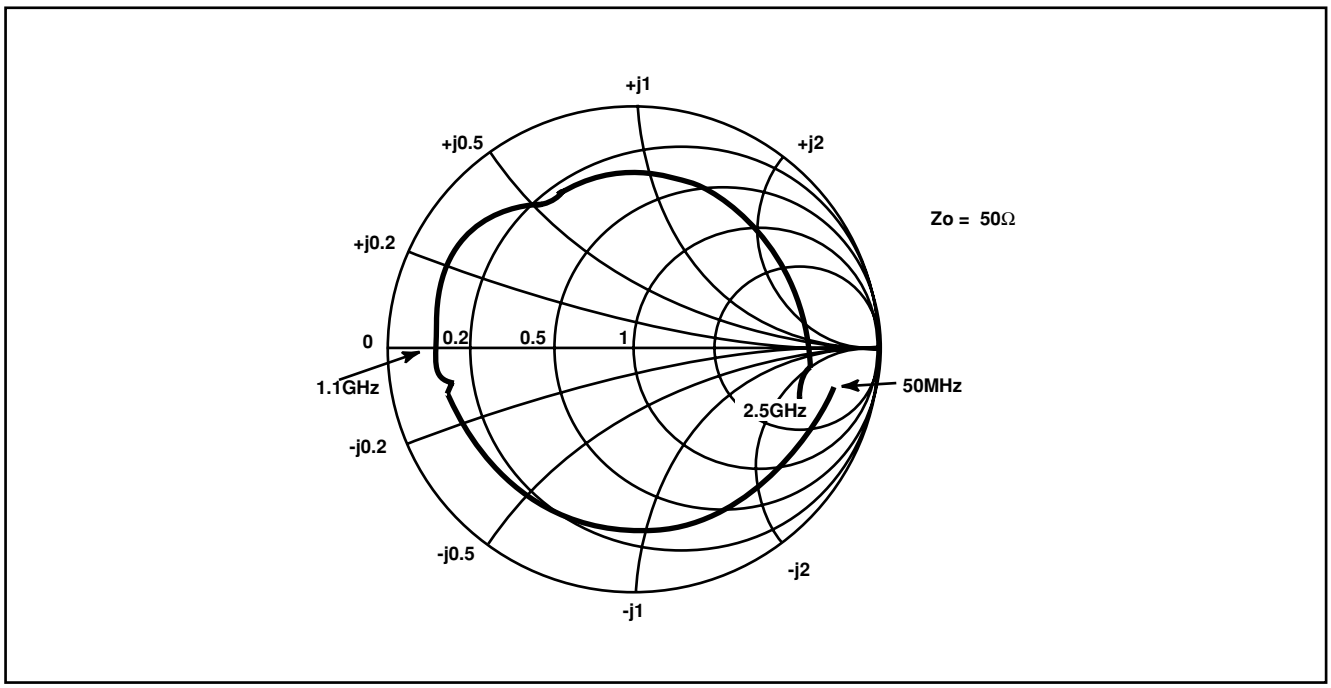


Figure 4 - R.F. input impedance

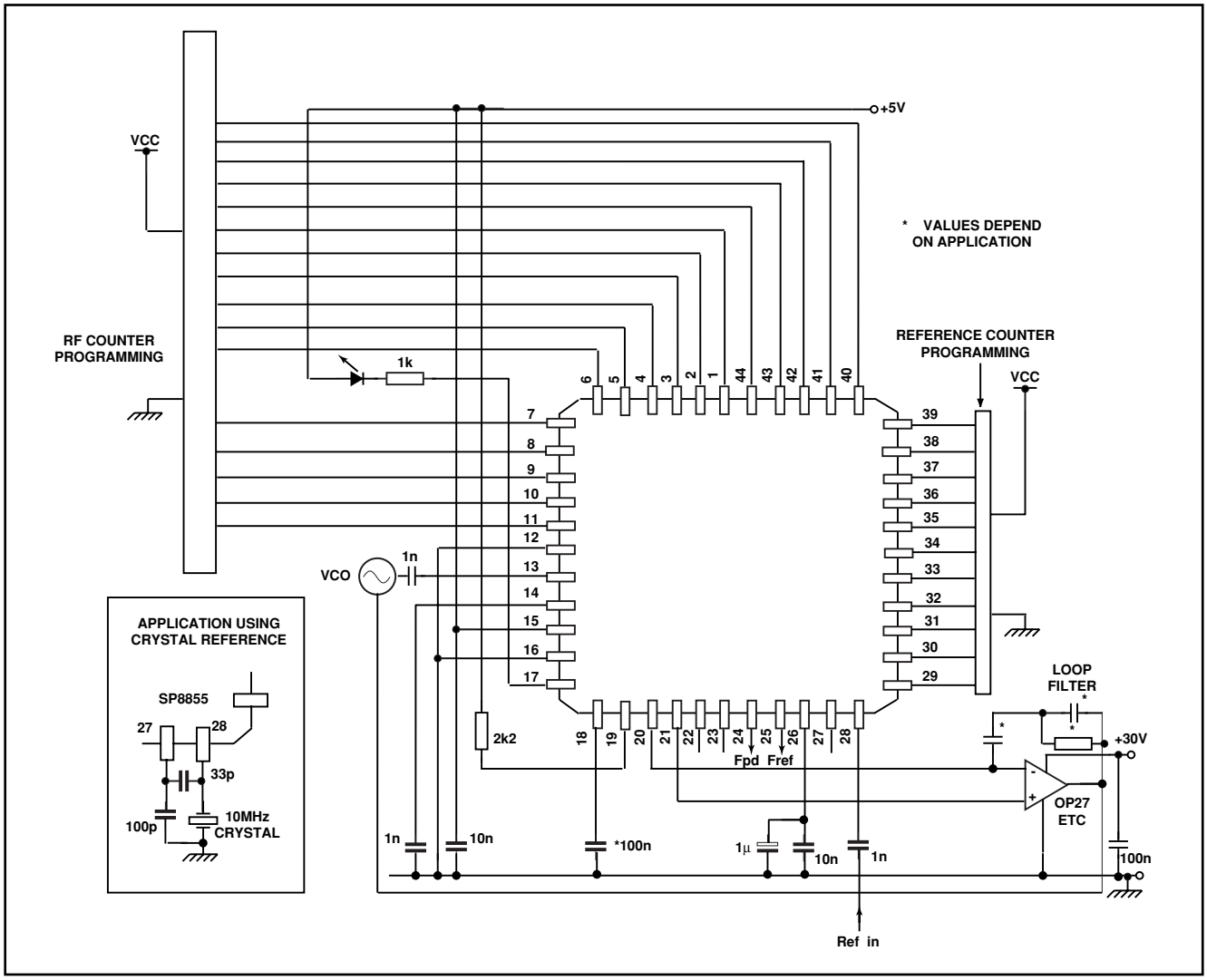


Figure 5 - Typical application diagram

Description

Prescaler and AM counter

The programmable divider chain is of AM counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN+A and a minimum integer steppable division ratio of N(N-1), where N is the prescaler ratio.

Programming

The device is programmed by connecting the programming pins to either V_{CC} or ground. The programming inputs will go high if left open circuit but for best noise immunity a wired connection to V_{CC} is preferable. The programming inputs can be driven from TTL or CMOS logic levels if required.

Reference input

The reference source can be either driven from an external sine or square wave source of up to 100MHz or a crystal can be connected as shown in Fig. 5.

Phase Comparator and Charge pump

The SP8855E has a digital phase/frequency comparator driving a charge pump with programmable current output. The charge pump current level at the minimum gain setting is approximately equal to the current fed into the R_{set} input pin 19 and can be increased by programming pins 40 and 41 according to Table 1 by up to 4 times.

Pin 40	Pin 41	Current Multiplication Factor
0	0	1.0
0	1	1.5
1	0	2.5
1	1	4.0

Table 1

$$\text{Pin 19 current} \;.\; \frac{V_{CC} - 1.6V}{R_{set}}$$

$$\text{Phase detector gain} = \frac{I_{pin\ 19}\,(mA) \times \text{multiplication factor}}{2\pi}\ mA/radian$$

To allow for control direction changes introduced by the design of the PLL, pin 23 can be programmed to reverse the control direction of the loop by transposing the F_{pd} and F_{ref} connections. In order that any external phase detector will also be reversed by this function, the F_{pd} and F_{ref} outputs are also interchanged as shown in Table 2.

Output for RF Phase Lag	
Control direction pin 23	pin 20
1	Current Source
0	Current Sink

Table 2

The Fpd and Fref signals to the phase detector are available on pin 24 and 25 and may be used to monitor the frequency input to the phase detector or used in conjunction with an external phase detector. When the Fpd/Fref outputs are to be used at high frequencies, an external pull down resistor of minimum value 330Ω may be used connected to ground to reduce the fall time of the output pulse.

The charge pump connections to the loop amplifier consist of the charge pump output and the charge pump reference. The matching of the charge pump up and down currents will only be maintained if the charge pumps output is held at a voltage equal to the charge pump reference using an operational amplifier to produce a virtual earth condition at pin 20.

The lock detect circuit can drive an LED to give visual indication of phase lock or provide an indication to the control system if a pull-up resistor is used in place of the LED. A small capacitor connected from the C-lock detector pin to ground may be used to delay lock detect indication and remove glitches produced by momentary phase coincidence during lock up. The phase detector can be disabled by pulling pin 39 to logic low.

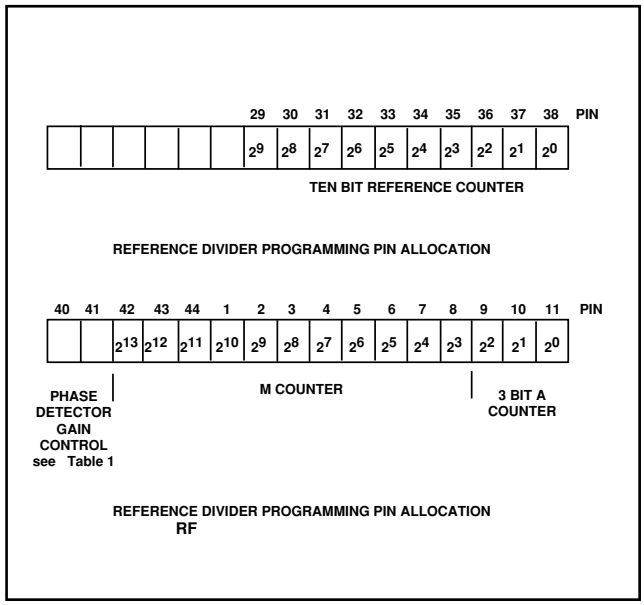


Figure 6 - Programming data format

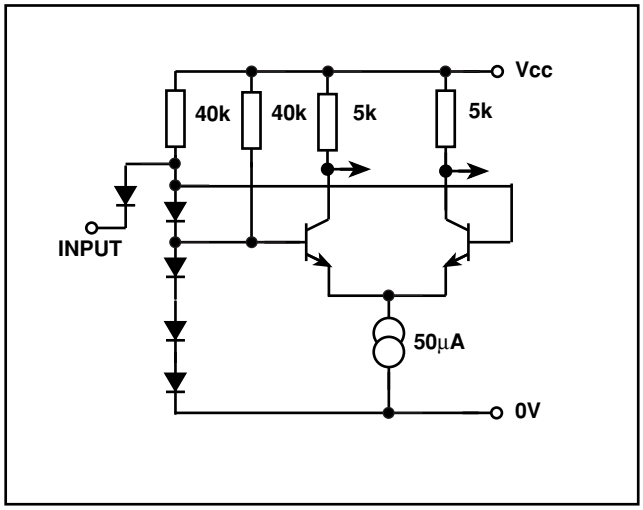


Figure 7a - RF and reference divider programming bits, F_{pd}/F_{ref} enable, control direction and phase detector gain control inputs

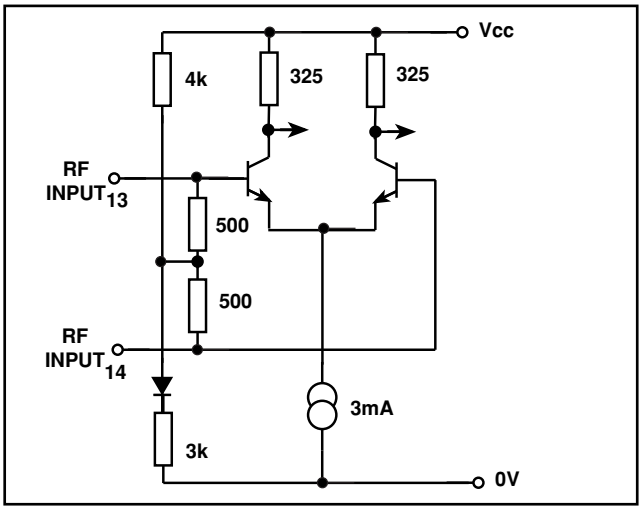


Figure 7b - RF inputs

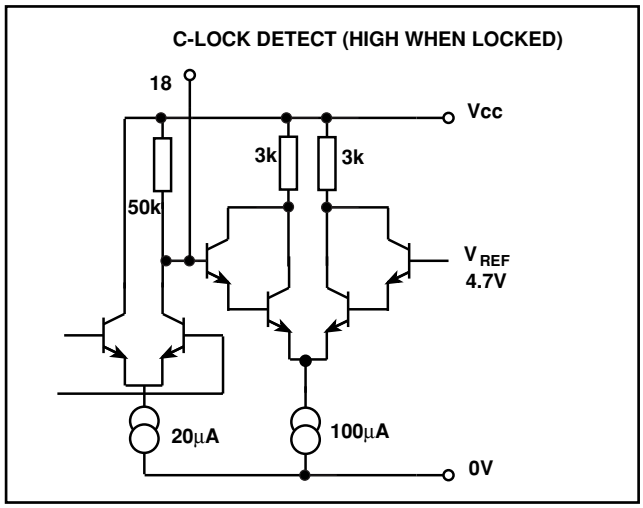


Figure 7c - Lock detect decouple

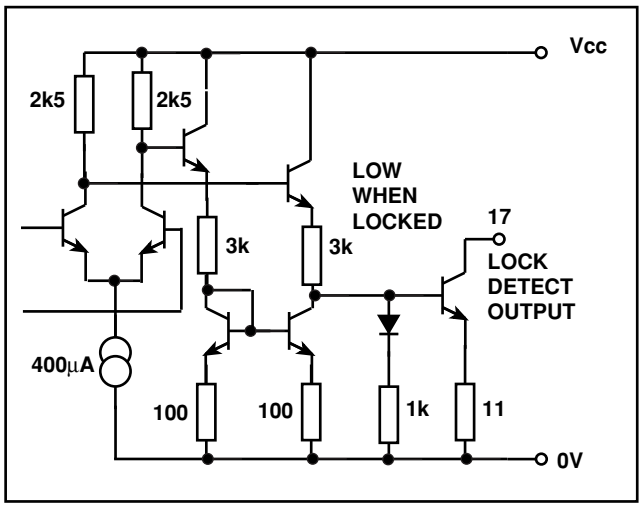


Figure 7d - Lock detect output

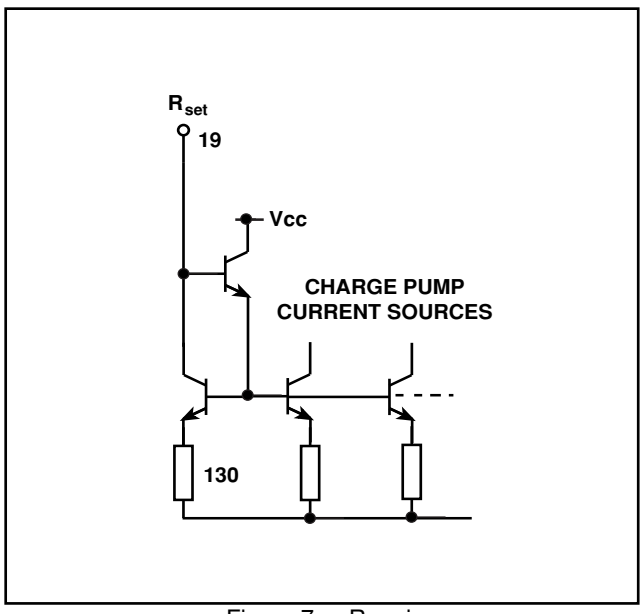


Figure 7e - R_{set} pin

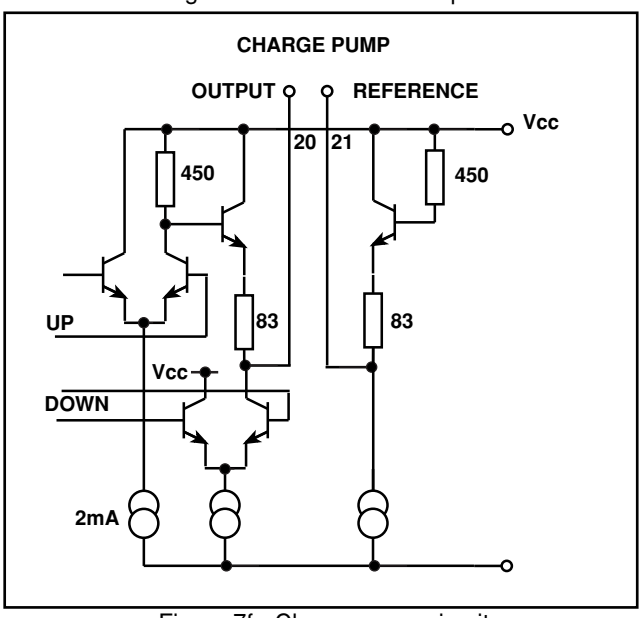


Figure 7f - Charge pump circuit

Figure 7 - Interface circuit diagrams

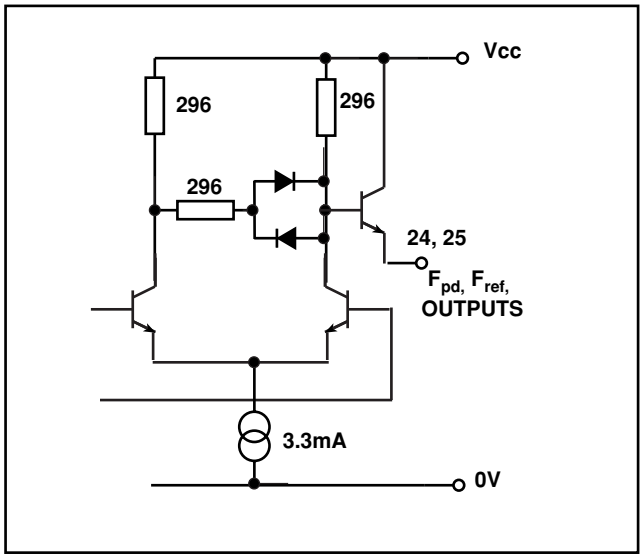


Figure 7g - F_{pd}, and F_{ref} outputs

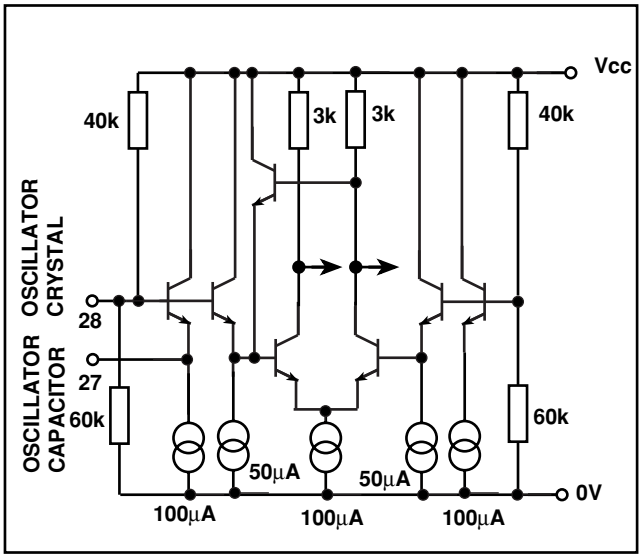


Figure 7h - Reference oscillator

Applications

RF Layout

The SP8855E can operate with input frequencies up to 2.8GHz but to obtain optimum performance, good RF layout practices should be used. A suitable layout technique is to use double sided printed circuit board with through plated holes. Wherever possible the top surface on which the SP8855E is mounted should be left as a continuous sheet of copper to form a low impedance earth plane. The ground pins 12 and 16 should be connected directly to the earth plane. Pins such as V_{cc} and the unused RF input should be decoupled with chip capacitors mounted as close to the device pin as possible with a direct connection to the earth plane, suitable values are 10nF for the power supplies and <1nF for the RF input pin. (a lower value should be used sufficient to give good decoupling at the RF frequency of operation). A larger decoupling capacitor mounted as close as possible to pin 26 should be used to prevent modulation of V_{CC} by the charge pump pulses. The R_{set} resistor should also be mounted close to the R_{set} pin to prevent noise pick-up, and the capacitor connected from the charge pump output should be a chip component with short connections to the SP8855E.

When the reference is derived from a crystal connected to pins 27 and 28 as shown in Fig.5 the oscillator components are best mounted close to the SP8855E.

All signals such as the programming inputs, RF in reference in and the connections to the op-amp are best taken through the pc board adjacent to the SP8855E with through plated holes allowing connections to remote points without fragmenting the earth plane.

Programming inputs

The input pins are designed to be compatible with TTL or CMOS logic with a switching threshold set at about 2.4V by three forward biased base emitter diodes. The inputs will be taken high by an internal pull up resistor if left open circuit but for best noise immunity it is better to connect unused inputs directly to V_{CC} or ground.

RF inputs

The prescaler has a differential input amplifier to improve input sensitivity. Generally the input drive will be single ended and the RF signal should be AC coupled to either of the inputs using a chip capacitor. The remaining input should be decoupled to ground , again using a chip capacitor. The inputs can be driven differentially but the input circuit should not provide DC path between inputs or to ground.

Lock detect circuit

The lock detect circuit uses the up and down correction pulses from the phase detector to determine whether the loop is in or out of lock. When the loop is locked, both up and down pulses are very narrow compared to the reference frequency, but the pulse width in the out of lock condition continuously varies, depending on the phase difference between the outputs of the reference and RF counters. The logical AND of the up and down pulses is used to switch a 20µA current sink to pin 18 and a 50k resistor provides a load to V_{CC}. The circuit is shown in Fig.7c. When lock is established, the narrow pulses from the phase detector ensure that the current source is off for the majority of the time and so pin18 will be pulled high by the 50k resistor. A voltage comparator with a switching threshold at abount 4.7V monitors the voltage at pin 18 and switches pin 17 low when pin 18 is more positive than the 4.7V threshold. When the loop is unlocked, the frequency difference at the counter outputs will produce a cyclic change in pulse width from the phase detector outputs with a frequency equal to the difference in frequency at the reference and RF counter outputs. A small capacitor connected to pin 18 prevents the indication of a false phase lock conditions at pin 17 for momentaary phase coincidence. Because of the variable width pulse nature of the signal at pin 18 the calculation of a suitable capacitor value is complex, but if an indication with a delay amounting to several times the expected lock up time is acceptable, the delay will be approximately equal to the time constant of the capacitor on pin 18 and the internal 50k resistor.

If a faster indication is required, comparable with the loop lock up time, the capacitor will need to be 2-3 times smaller than the time constant calculation suggests. The time to respond to an out of lock conditions is 2-3 times less than that required to indicate lock.

Charge pump circuit

The charge pump circuit converts the variable width up and down pulses from the phase detector into adjustable current pulses which can be directly connected to the loop amplifier. The magnitude of the current and therefore the phase detector gain can be modified when new frequency data is entered to compensate for change in the VCO gain characteristics over its frequency band. The charge pump pulse current is determined by the current fed into pin 19 and is approximately equal to pin 19 current when the programmed multiplication ratio is one. The circuit diagram Fig. 7e shows the internal components on pin 19 which mirror the input current into the charge pump. The voltage at pin 19 will be approximately 1.6V above ground due to two V_{be} drops in the current mirror. This voltage will exhibit a negative temperature coefficient, causing the charge pump current to change with chip temperature by up to 10% over the full military temperature range if the current programming resistor is connected to V_{cc} as shown in the application diagram Fig. 5. In critical applications where this change in charge pump current would be too large the resistor to pin 19 could be increased in value and connected to a higher supply to reduce the effect of V_{be} variation on the current level. A suitable resistor connected to a 30V supply would reduce the variation in pin 19 current due to temperature to less than 1.5%. Alternatively a stable current source could be used to set pin 19 current.

The charge pump output on pin 20 will only produce symmetrical up and down currents if the voltage is equal to that on the voltage reference pin 21. In order to ensure that this voltage relationship is maintained, an operational amplifier must be used as shown in the typical application Fig. 5. Using this configuration pin 20 voltage will be forced to be equal to that pin 21 since the operational amplifier differential input voltage will be no more than a few millivolts (the input offset voltage of the amplifier). When the synthesiser is first switched on or when a frequency outside VCO range is programmed the amplifier output will limit, allowing pin 20 voltage to differ from that on pin 21. As soon as an achievable frequency value is programmed and the amplifier output starts to slew the correct voltage relationship between pin 20 and 21 will be restored. Because of the importance of voltage equality between the charge pump reference and output pins, a resistor should never be connected in series with the operational amplifier inverting input and pin 20 as is the case with a phase detector giving voltage outputs. Any current drawn from the charge pump reference pin should be limited to the few micro amps input current of a typical operational amplifier. A resistor between the charge pump reference and the non inverting input could be added to provide isolation but the value should not be so high that more than a few millivolts drop are produced by the amplifier input current.

When selecting a suitable amplifier for the loop filter, a number of parameters are important; input offset voltage in most designs is only a few millivolts and an offset of 5mV will produce a mismatch in the up and down currents of about 4% with the charge pump multiplication factor set at 1. The mismatch in up down currents caused by input offset voltage will be reduced in proportion to the charge pump multiplication factor in use. If the linearity of the phase detector about the normal phase locked operating point is critical, the input offset voltage of most amplifiers can be adjusted to near zero by means of a potentiometer.

The charge pump reference voltage on pin 21 is about 1.3V below the positive supply and will change with the temperature and with the programmed charge pump multiplication factor. In many cases it is convenient to operate the amplifier with the negative power supply pin connected to 0V as this removes the need for an additional power supply. The amplifier selected must have a common mode range to within 3.4V (minimum charge pump reference voltage) of the negative supply pin to operate correctly without a negative supply. Most popular amplifiers can be operated from a 30V positive supply to give a wide VCO voltage drive range and have adequate common mode range to operate with inputs at +3.4V with respect to the negative supply. Input bias and offset current levels to most operational amplifiers are unlikely to be high enough to significantly affect the accuracy of the charge pump circuit currents but the bias current can be important in reducing reference side bands and local oscillator drift during frequency changes. When the loop is locked, the charge pump produces only very narrow pulses of sufficient width to make up for any charge lost from the loop filter components during the reference cycle. The charge lost will be due to leakage from the charge pump output pin and to the amplifier input bias current the latter usually being more significant. The result of the lost charge is a sawtooth ripple on the VCO control line which frequency modulates the phase locked oscillator at the reference frequency and its harmonics.

It is possible to disable the charge pump by taking pin 39 low. In this case any leakage current will cause the oscillator to drift off frequency. This feature may be useful where having achieved lock an external phase detector of the user's choice can be employed to suit a specific application.

F_{pd} and F_{ref} outputs

These outputs provide access to the outputs from the RF and reference dividers and are provided for monitoring purposes during product development or test, and for connection of an external phase detector if required. The output circuit is of ECL type, the circuit diagram being shown in Fig. 7g. The outputs are enabled when pin 22 is high and disabled when pin22 is low, but are best left in the disabled state when not required as the fast edge speeds on the output can increase the level of reference sidebands on the synthesised oscillator.

The emitter follower outputs have no internal pull down resistor to save current and if the outputs are required an external pull down resistor should be fitted. The value should be kept as high as possible to reduce supply current, about 2.2k. being suitable for monitoring with a high impedance oscilloscope probe or for driving an AC coupled 50 Ohm load.

A minimum value for the pull down resistor is 330 Ohms. When the F_{pd} and F_{ref} outputs are disabled the output level will be at the logic low level of about 3.5V so that the additional supply current due to the load resistors will be present even when the outputs are disabled.

Reference input

The reference input circuit functions as an input amplifier or crystal oscillator. When an external reference signal is used this is simply AC coupled to pin 28, the base of the input emitter follower. When a low phase noise synthesiser is required the reference signal is critical since any noise present here will be multiplied by the loop. To obtain the lowest possible phase noise from the SP8855E it is best to use the highest possible reference input frequency and to divide this down internally to obtain the required frequency at the phase detector. The amplitude of the reference input is also important, and a level close to the maximum will give the lowest noise. When the use of a low reference input frequency say 4-10MHz is essential some advantage may be gained by using a limiting amplifier such as a CMOS gate to square up the reference input.

In cases where a suitable reference signal is not available, it may be more convenient to use the input buffer as a crystal oscillator in this case the emitter follower input transistor is connected as a Colpitts oscillator with the crystal connected from the base to ground and with the feedback necessary for oscillation provided by a capacitor tap at the emitter. The arrangement is shown inset in Fig. 5.

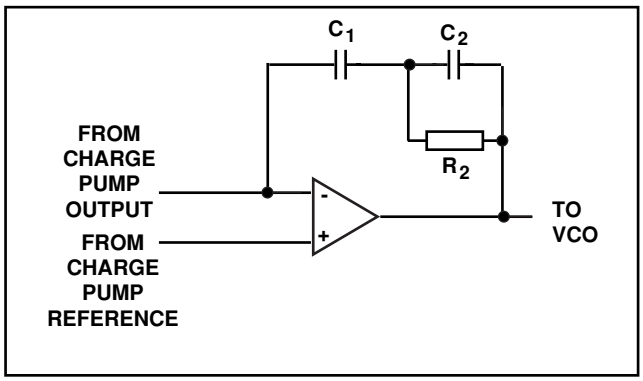


Figure 8 - third order loop filter circuit diagram

Loop Filter Design

Generally the third order filter configuration shown in Fig.8 gives better results than the more commonly used second order because the reference sidebands are reduced. Three equations are required to determine values for the three constants where;

$$\tau_1 = C_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

The equations are

$$1 \qquad \tau_1 = \frac{K_\phi K_0}{N\omega_n^2} \left[\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2} \right]^{1/2}$$

$$2 \qquad \tau_2 = \frac{1}{\omega_n^2 \tau_3}$$

$$3 \qquad \tau_3 = \frac{-\tan \phi_o + \frac{1}{\cos \phi_o}}{\omega_n}$$

Where;

- K_ϕ is the phase detector gain factor in mA/radian
- K_0 is theVCO gain factor in radian/second/Volt
- N is the total division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- ϕ_o is the phase margin normally set to 45°

Since the phase detector is linear over a range of 2π radian, K_ϕ can be calculated from

K_ϕ = Phase comparator current setting/2π mA/radian

These values can now be substituted in equation 1 to obtain a value for C_1 and equation 2 and 3 used to determine values for C_2 and R_2

EXAMPLE

Calculate values for a loop with the following parameters

Frequency to be synthesised:	1000MHz
Reference frequency	10MHz
Division ratio	1000MHz/10MHz = 100
ω_n natural loop frequency	100KHz
K_0 VCO gain factor	2π x 10MHz/Volt
ϕ_0 phase margin	45°
Phase comparator current	6.3mA

The phase detector gain factor K_ϕ
= 6.3mA /2π = 1mA/radian

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{100kHz \times 2\pi} = \frac{0.4142}{628319}$$

$$\tau_3 = 659 \times 10^{-9}$$

From equation 2:

$$\tau_2 = \frac{1}{(100kHz \times 2\pi)^2 \times 659 \times 10^{-9}}$$

$$\tau_2 = 3.844 \times 10^{-6}$$

Using these values in equation 1:

$$\tau_1 = \frac{1 \times 10^{-3} \times 2\pi \times 10MHz/V}{100 \times (2\pi \times 100kHz)^2} [A]^{1/2}$$

Where A is:

$$\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2} = \frac{1 + (2\pi \times 100kHz)^2 \times (3.844 \times 10^{-6})^2}{1 + (2\pi \times 100kHz)^2 \times (659 \times 10^{-9})^2}$$

$$\tau_1 = \frac{62832}{39.48 \times 10^{12}} \left[\frac{6.833}{1.1714}\right]^{1/2}$$

$$\tau_1 = 1.59 \times 10^{-9} \times 2.415$$

$$\tau_1 = 3.84 \times 10^{-9}$$

Now $\tau_1 = C1 \therefore C1 = 3.84nF$

$$\tau_2 = R_2 (C_1 + C_2)$$

$$\tau_3 = C_2 R_2$$

Substituting for C_2

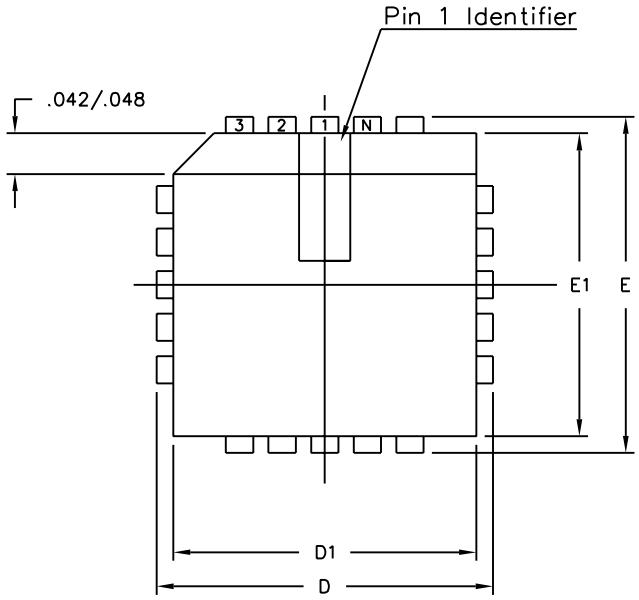
$$\tau_2 = R_2 \left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

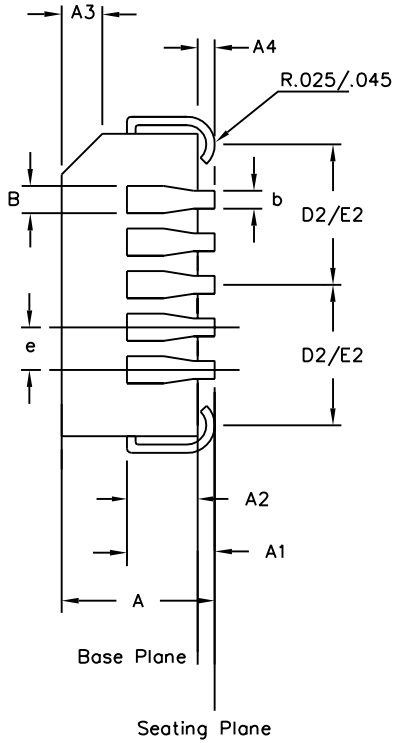
$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{3.844 \times 10^{-6} - 659 \times 10^{-9}}{9.61 \times 10^{-9}}$$

$$R_2 = 829.4\Omega$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{659 \times 10^{-9}}{829.4}$$

$$C_2 = 0.794nF$$





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 44 lead PLCC

GPD00003

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www.zarlink.com