A DIVISION OF CIRRUS LOGIC

CDB5181

Evaluation Board for the CS5181

Features

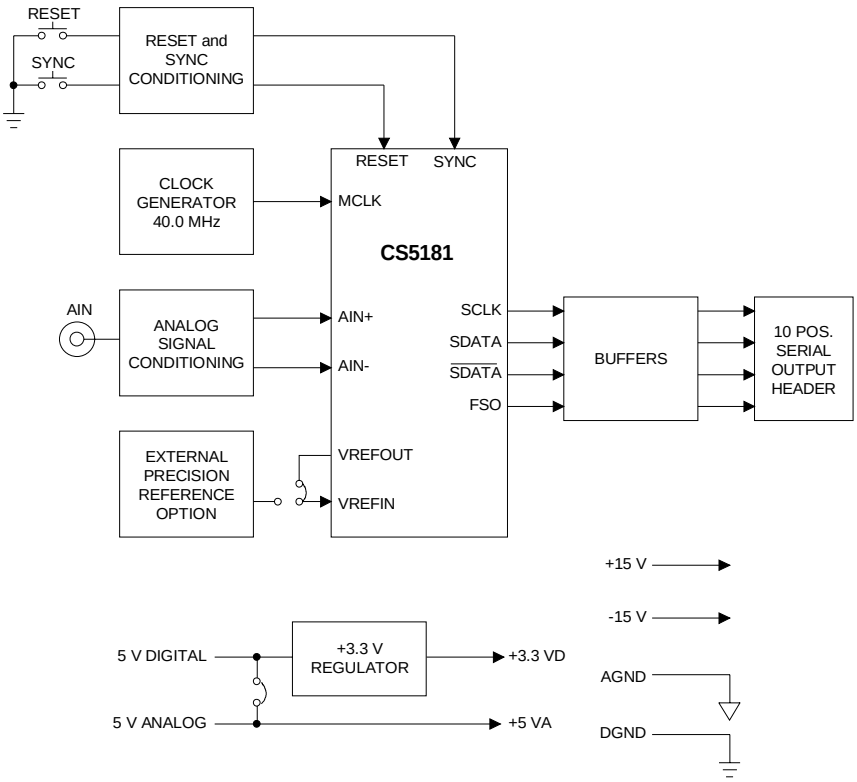
- Buffered Serial Data Output
- Input Signal Conditioning Amplifiers
- On-board 3.3 Volt regulator
- Analog/Digital Patch Areas
- Analog BNC Input Connector
- Provision for optional precision voltage reference
- Compatible with CDBCapture+ board
- Provision for evaluation of CS5181 with internal digital filter enabled or disabled (one-bit mode)

Description

The CDB5181 is an evaluation board that expedites the laboratory characterization of the CS5181 A/D converter. The CS5181 is a 16-bit high speed delta-sigma converter with a serial output having an output word rate of up to 625 kHz. The board accepts single-ended or differential input signals and buffers the serial output of the CS5181 before sending it to a header for off-board use. The output header signals on the evaluation board are designed to be compatible with the CDBCapture+ board. An on-board 3.3 Volt regulator allows the CS5181 to be evaluated with the recommended 3.3 Volts for the digital supplies. The converter can be operated with it's internal voltage reference although the layout makes provision for adding an external precision reference as a user-supplied option.

ORDERING INFORMATION

CDB5181 Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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POWER SUPPLIES AND VOLTAGE REFERENCE

Figure 1 illustrates the power supply and precision voltage reference circuits. The CDB5181 evaluation board has inputs for 4 regulated voltages, +5 Volts Digital, +5 Volts Analog, +15 Volts, and -15 Volts. As an option, one 5 Volt power supply may be used to power both the analog and digital portions of the converter. This is done by installing HDR17 and connecting the 5 Volt supply to post J7. The 5 Volts is applied to a 3.3 Volt regulator to allow the converter's digital circuitry to operate from the recommended 3.3 Volts. This regulator also powers the other digital circuitry on the board. The plus and minus 15 Volts are used to power the analog signal conditioning circuits external to the converter. The analog 5 Volt supply can be used to power a precision 2.5 Volt reference, an LT1019-2.5 or equivalent, which can be substituted for the converter's on-board reference to achieve lower drift. The board is supplied with the external reference and it's passive components depopulated. If it is desired to use an external reference, then the following steps must be completed.

1) Remove zero-ohm resistor R32 and install a zero-ohm resistor in the R33 position.
2) Install the following components: U10, C38, C56, R22, C59, and R25.
3) Set the reference voltage to the desired value by adjusting potentiometer R22.

The output of the internal reference is connected to the operational amplifiers through zero-ohm resistor R54. If it is desired to use the external reference to drive the signal conditioning circuits, then R54 must be removed and a zero-ohm resistor installed in position R55.

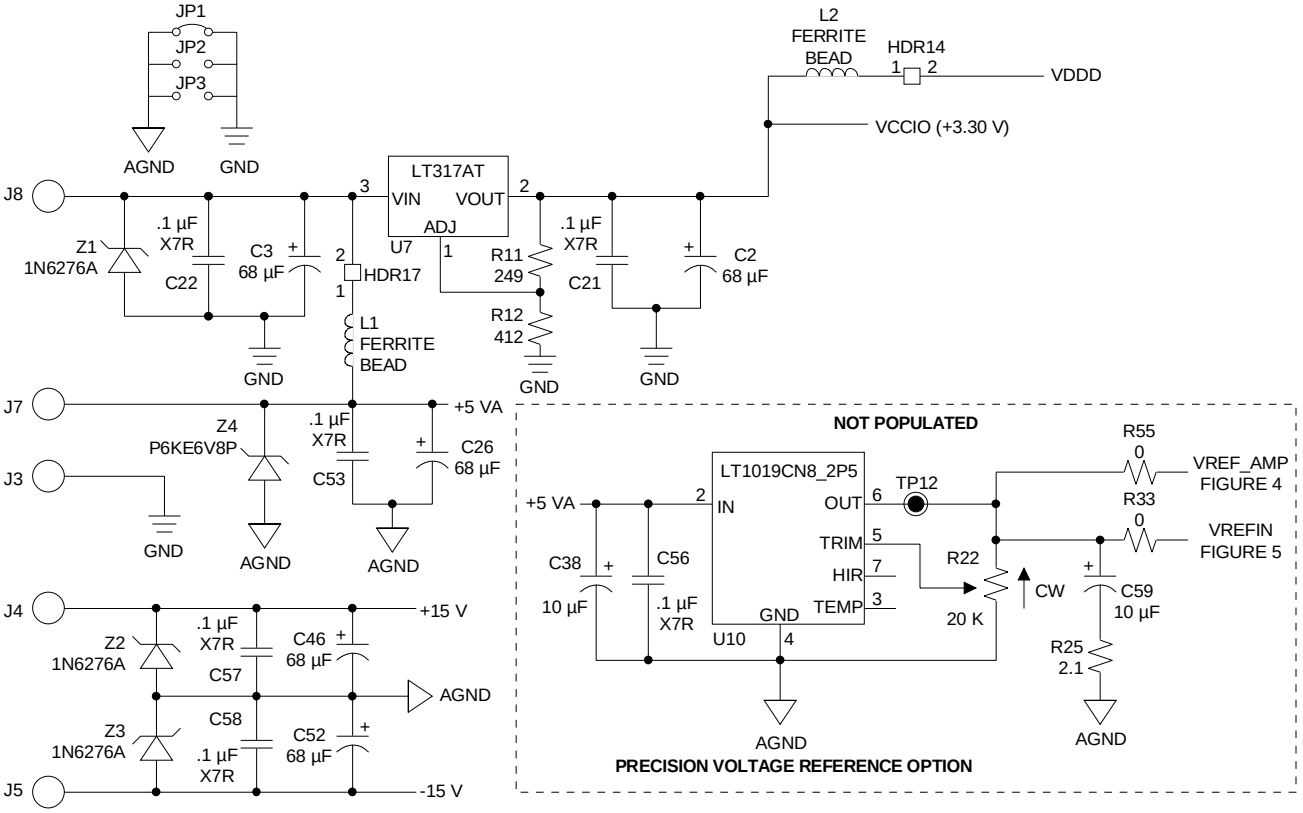

Figure 1. Power Supplies and Voltage Reference

CLOCK OSCILLATOR AND BUFFER

Figure 2 illustrates the circuitry used to generate the clock signal MCLK that drives the CS5181. The board contains a 40.0 MHz nominal oscillator as well as a BNC connector for use with an external clock source. The on-board oscillator is buffered and inverted to form a complementary clock signal, MCLKB, that is used in the SYNC and RESET circuits. Selection of internal clock or external clock is done by setting header HDR3 to either the OSC or BNC position. Using the on-board oscillator will result in an output word rate of 625.0 kHz. If an external clock is going to be used, care should be taken to insure that the peak amplitude of the clock signal does not exceed 3.3 Volts.

RESET AND SYNC CIRCUITS

Figure 3 illustrates the circuits used for generating the chip RESET and SYNC signals. Two manual pushbuttons are provided for generating the RESET and SYNC signals, which are synchronized to the falling edge of the master clock by means of a flip-flop before being sent to the CS5181. Header HDR2, not populated, is provided for connecting to external SYNC and RESET signals. To use the external signals, set headers HDR6 and HDR7 to the EXT position and apply the external signals at the HDR2 thru-holes.

INPUT SIGNAL CONDITIONING

Figure 4 illustrates the circuitry used to condition the analog input signal. A single-ended input is fed in via the BNC connector to a pair of operational amplifiers. The signal is buffered and also inverted to form differential signals. These signals are then fed to two more op-amps where the voltage reference is added to each of them to bring the common mode voltage up to the range required by the converter. Potentiometer R41 is available to adjust the offsets on the two op-amp outputs to be equal, so that with zero volts in at J2, the converter reads zero. The two signals are then passed through an attenuating resistor network before being input to the converter. A 1.0 Volt peak-peak signal input at the BNC connector will result in nominal 0.2849 Volt peak-peak fully differential signals being applied between the AIN+ and AIN- pins of the converter. If the external signal is not single ended but is already differential, it can be input through connector J6 where it is capacitively coupled in and offset to the proper common mode value before being applied to the converter. The settings of HDR8 and

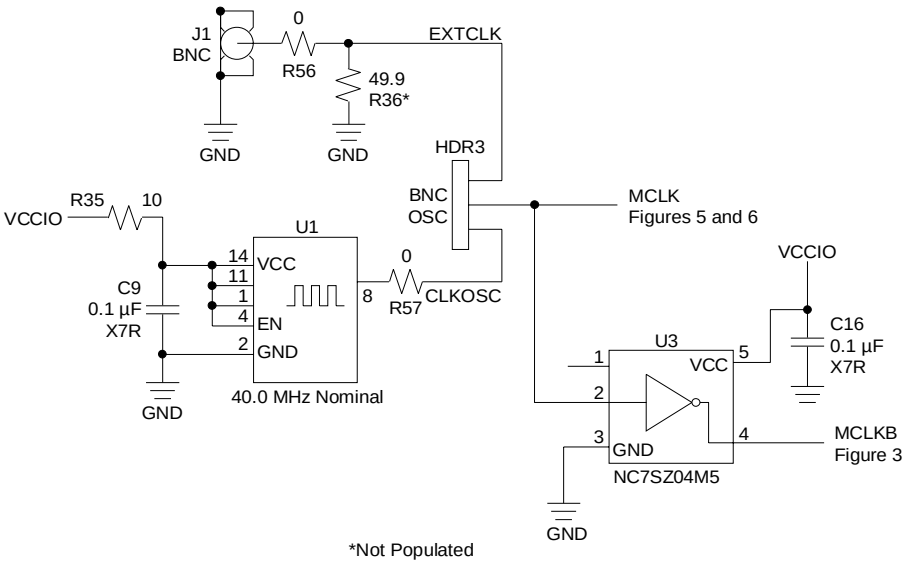

Figure 2. Clock Oscillator and Buffer

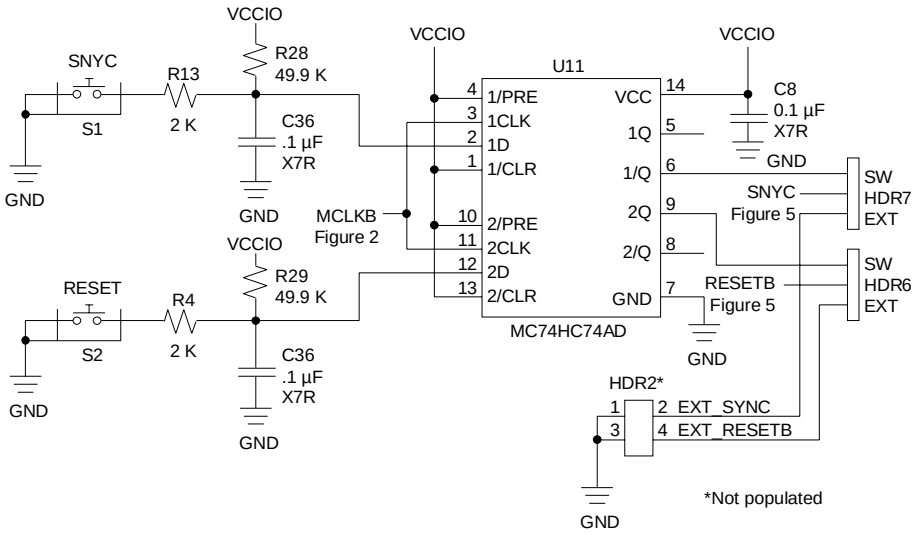

Figure 3. Reset and Sync Circuits

HDR9 select whether the input signal will be input through the BNC connector as a single-ended signal or through J6 as a differential signal. To use the DC-coupled signal from the BNC connector J2, set headers HDR8 and HDR9 to the BNC position. To feed a capacitively coupled signal from J6 to the CS5181, set HDR8 and HDR9 to the XLR position. Alternatively, the differential signals can be applied by feeding them into test points BAL+ and BAL-. Note that connector J6, R20, R21, C40, and C41 do not come installed on the board and must be obtained and soldered in by the user before a balanced signal can be applied to the board input. J6, R20, R21, C40, and C41 are not required when a single-ended signal is being applied to connector J2, since the op-amps will convert and apply a balanced signal to the CS5181.

CS5181 CONVERTER CIRCUITS

The connections to the CS5181 chip are illustrated in Figure 5. The analog and digital supply voltages are all decoupled with X7R ceramic capacitors close to the device. In addition to the 0.1 µF ceramic capacitors, there are 1 and 10 µF electrolytic caps on the voltage reference input and output lines to minimize noise on the references. An LED is connected to the MFLAG signal and when on, indicates that data from the converter may be invalid due to an input overload. Header plugs are provided to change the MODE pin, allowing for raw 1-bit modulator data to be output, and for placing the chip in the power-down mode. For normal operation, header HDR15 should not be installed. To use the CS5181 internal digital filter, the mode pin should be set high by removing header HDR16. If HDR16 is installed, the internal digital filter is disabled and the direct unfiltered modulator output will be presented on the serial data pin SDO. For this condition, header HDR12 should be set to the MCLK position.

OUTPUT BUFFERS AND HEADER CONNECTIONS

Figure 6 illustrates the circuitry for sending the output data off-board and the associated header connections. The CS5181 outputs data in a serial format only, along with the serial clock and the frame sync signal, FSO. These signals are buffered externally to the CS5181 and then made available on the 10-pin header HDR1. Header HDR12 can be used to select between sending the serial clock SCLK or the master clock, MCLK, to pin 8 of HDR1. If the evaluation board is being used with the CDBCapture+ board then the CS5181 should

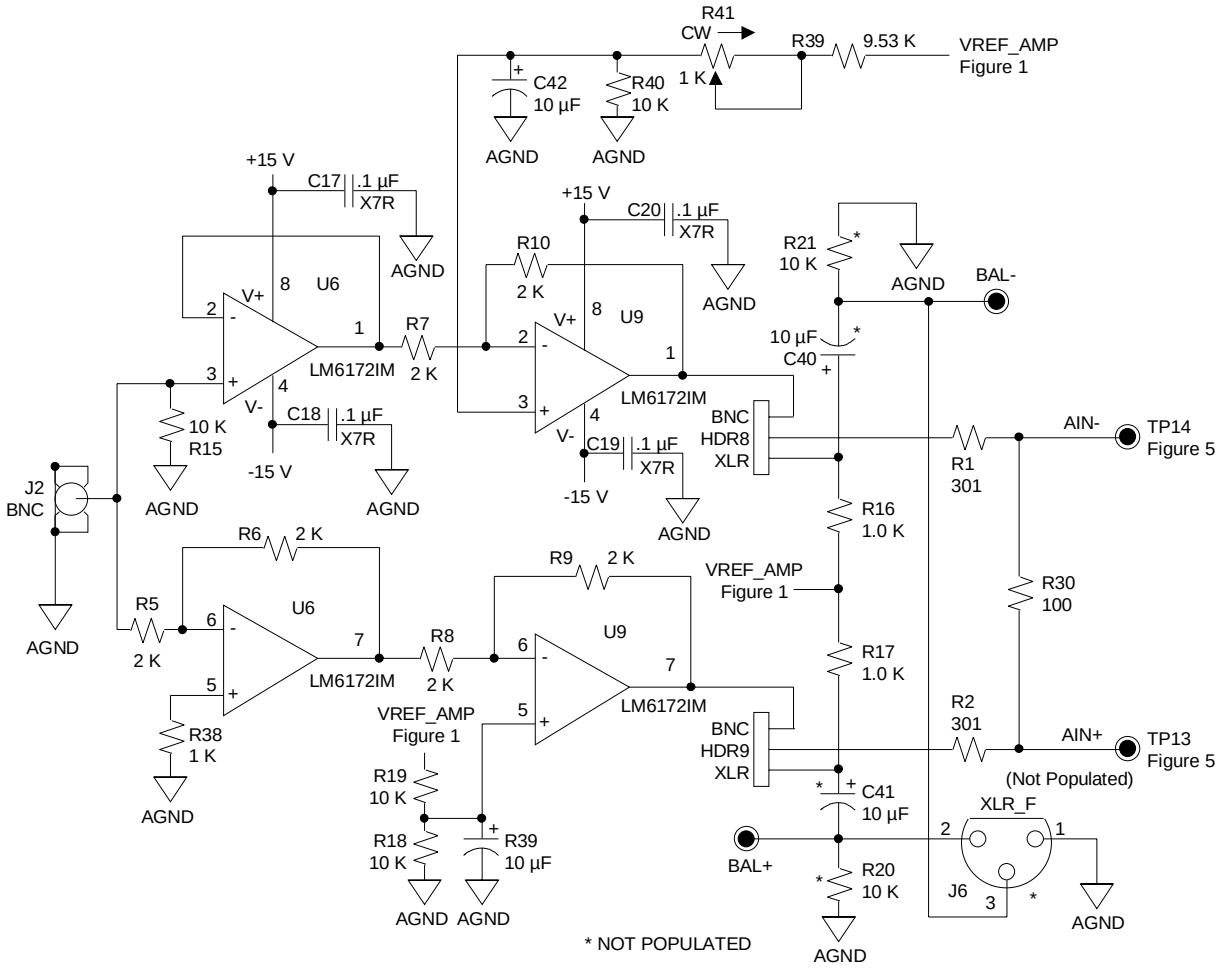

Figure 4. Input Signal Conditioning Circuitry

be operated in Mode 1 (internal digital filter enabled), and HDR12 should be set to the SCLK position, where SCLK is connected to HDR1. If the evaluation board is being used without the CDB-Capture+ board and the CS5181 is operating in Mode 0 (raw modulator output), then HDR12 should be set to the MCLK position, feeding the master clock signal to connector HDR1. Nor-gates U13 and U14 will automatically reconstruct the RTZ data from the modulator bitstream so that it can be sampled on the falling edge of MCLK.

USING THE EVALUATION BOARD

Although the evaluation board can be connected directly to a microprocessor that has a serial port and is fast enough to process up to 625K words/second, it can be more convenient to use the evaluation board in conjunction with the Crystal CDBCapture+ Board, which has been designed specifically to interface with high speed converters and has a 10-pin header that is compatible with the signals on header HDR1 of the evaluation board. Connect the appropriate power supply voltages to the binding posts of the board. Use high quality linear power supplies that are low in noise, ripple, and line frequency (50/60 Hz) interference. If both 5 V digital and 5 V analog supplies are to be used, make sure that HDR17 is removed to prevent contention between the supplies. Total 5 Volt current requirements are approximately 0.2 Amps. The load on the plus and minus 15 Volt supplies will be under 0.1 Ampere each. The Capture Plus board is then

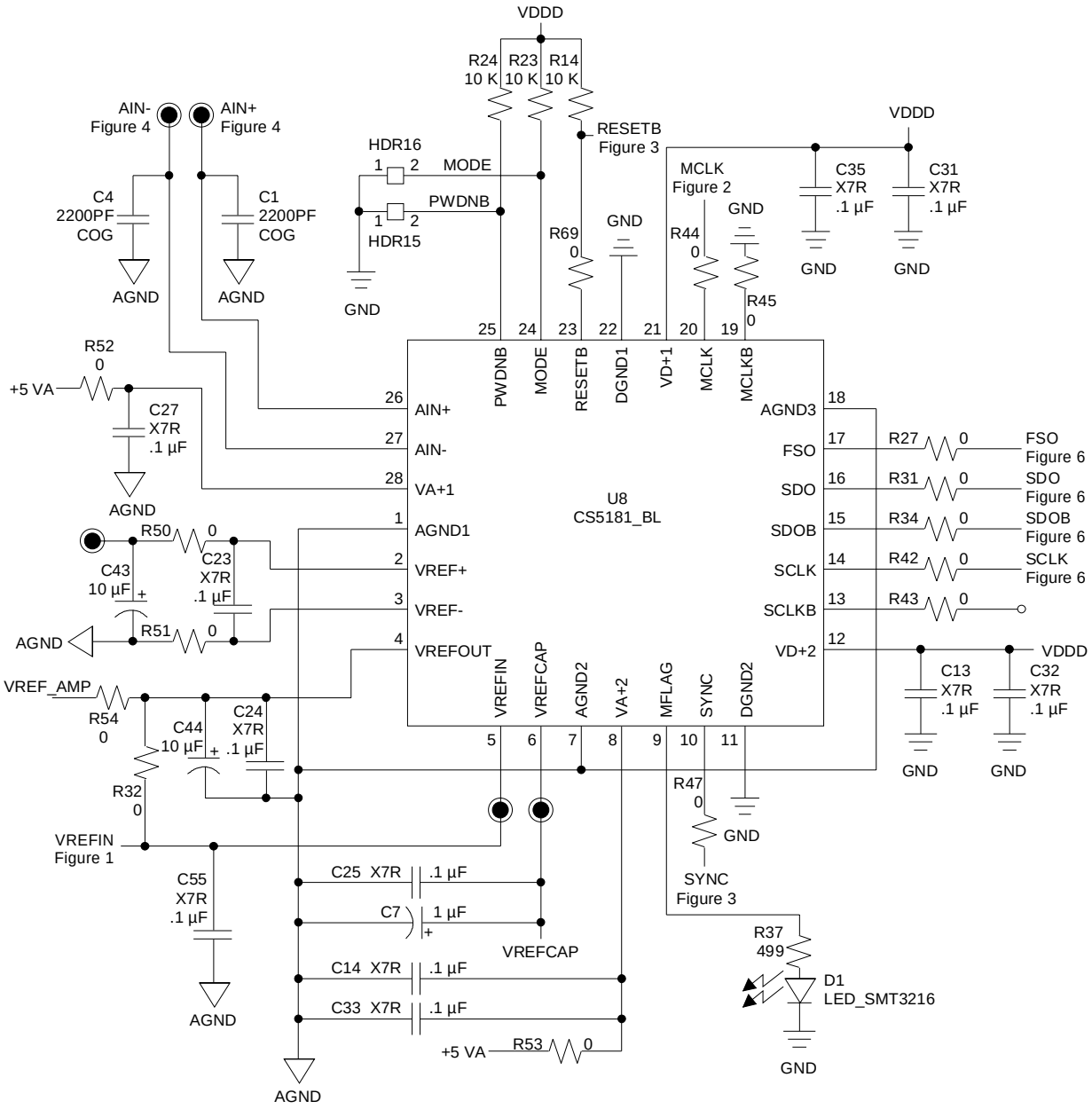

Figure 5. CS5181 Converter Circuit

connected to a PC and Crystal's software is used to configure the board and to capture data.

Connect a coaxial cable from the AIN BNC (J2) to a high quality signal source, such as the Krohn-Hite Model 4400A. Note that the performance of the CS5181 A/D converter can exceed the capability of many signal generators, especially with respect to noise and line frequency interference.

COMPONENT LAYOUT

Figures 7, 8, and 9 illustrate the component placement and layout of the CDB5181 evaluation board. Digital and analog patch areas have been provided for experimentation with new components. Note that all the power supply rails and their grounds are made available in the respective patch areas.

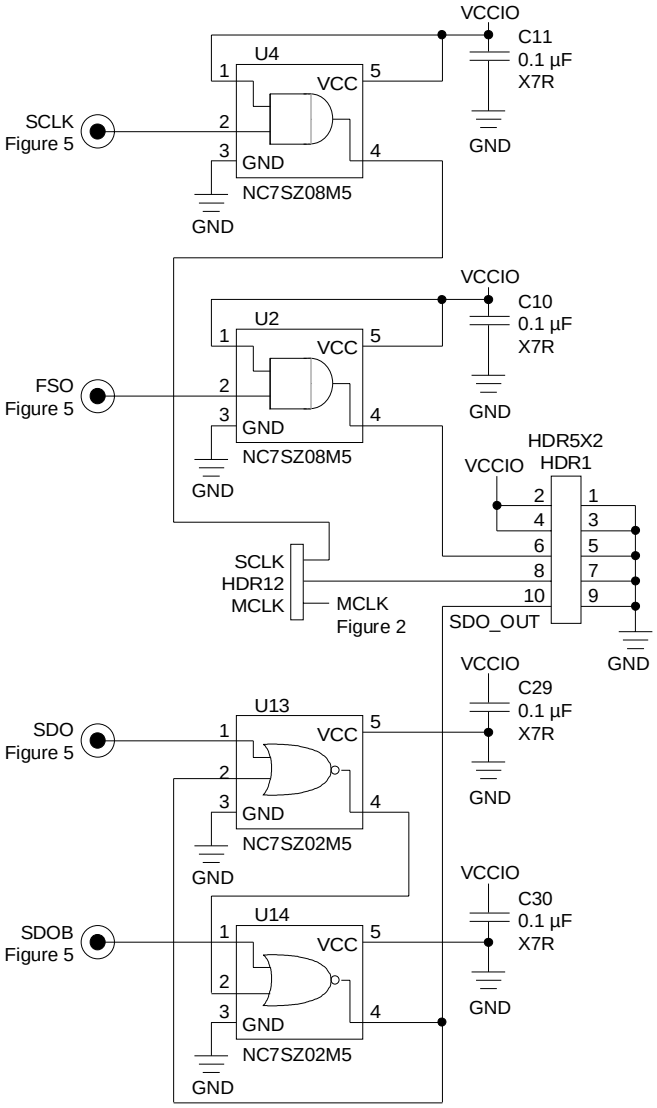

Figure 6. Output Buffers and Header Connections

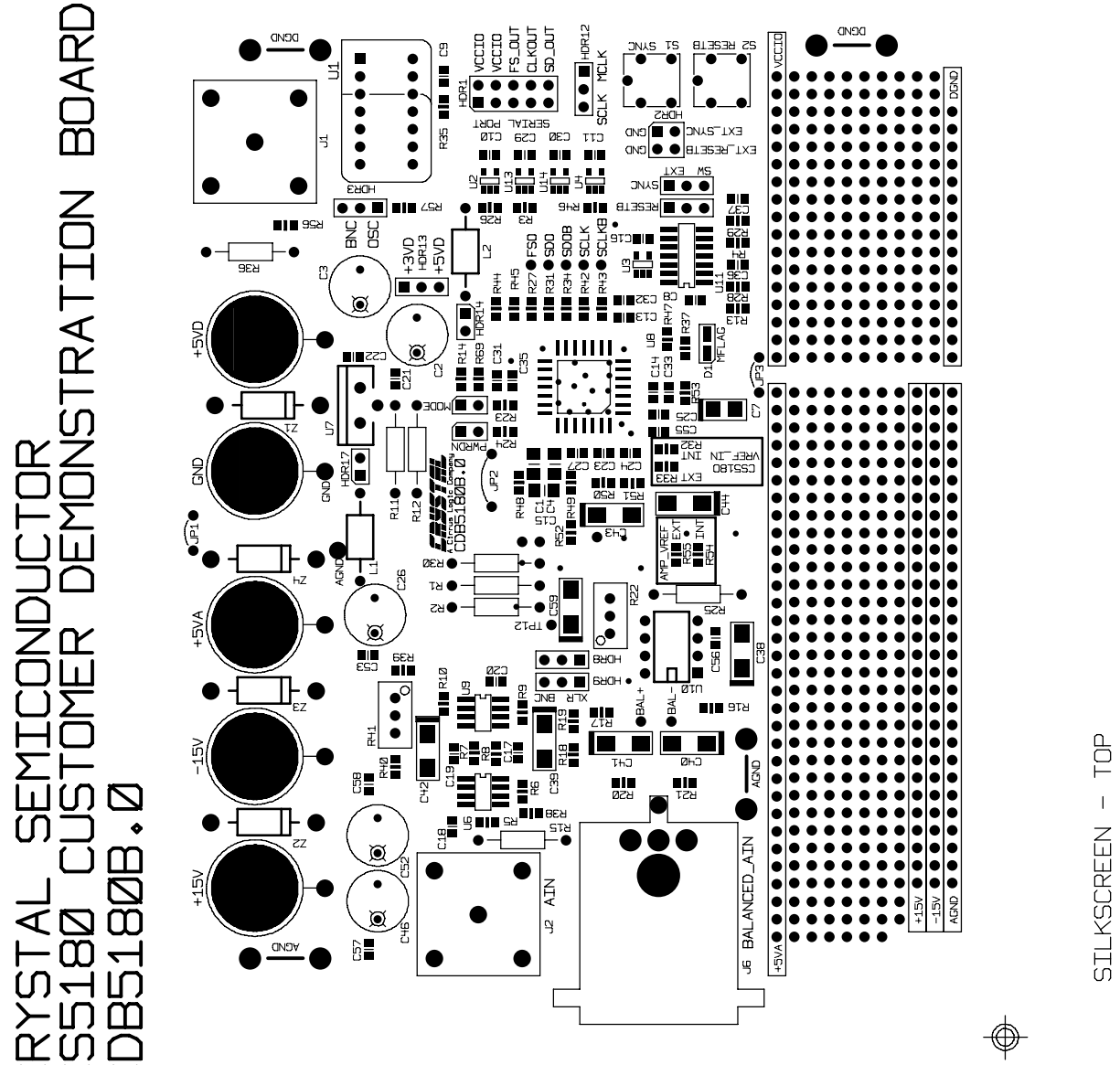

Figure 7. Component Top Side Layout Silkscreen

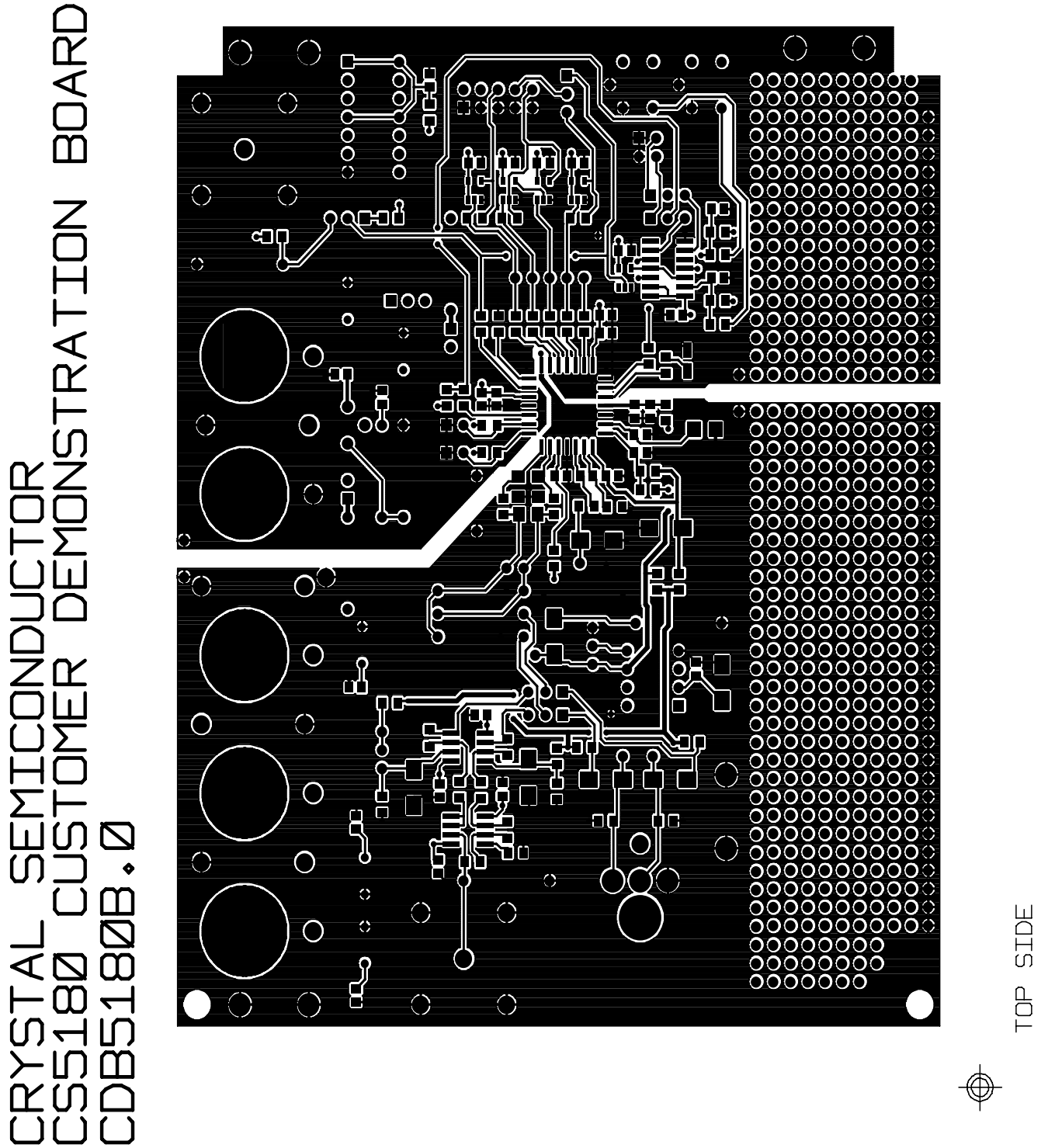

Figure 8. Top Side Traces and Groundplane

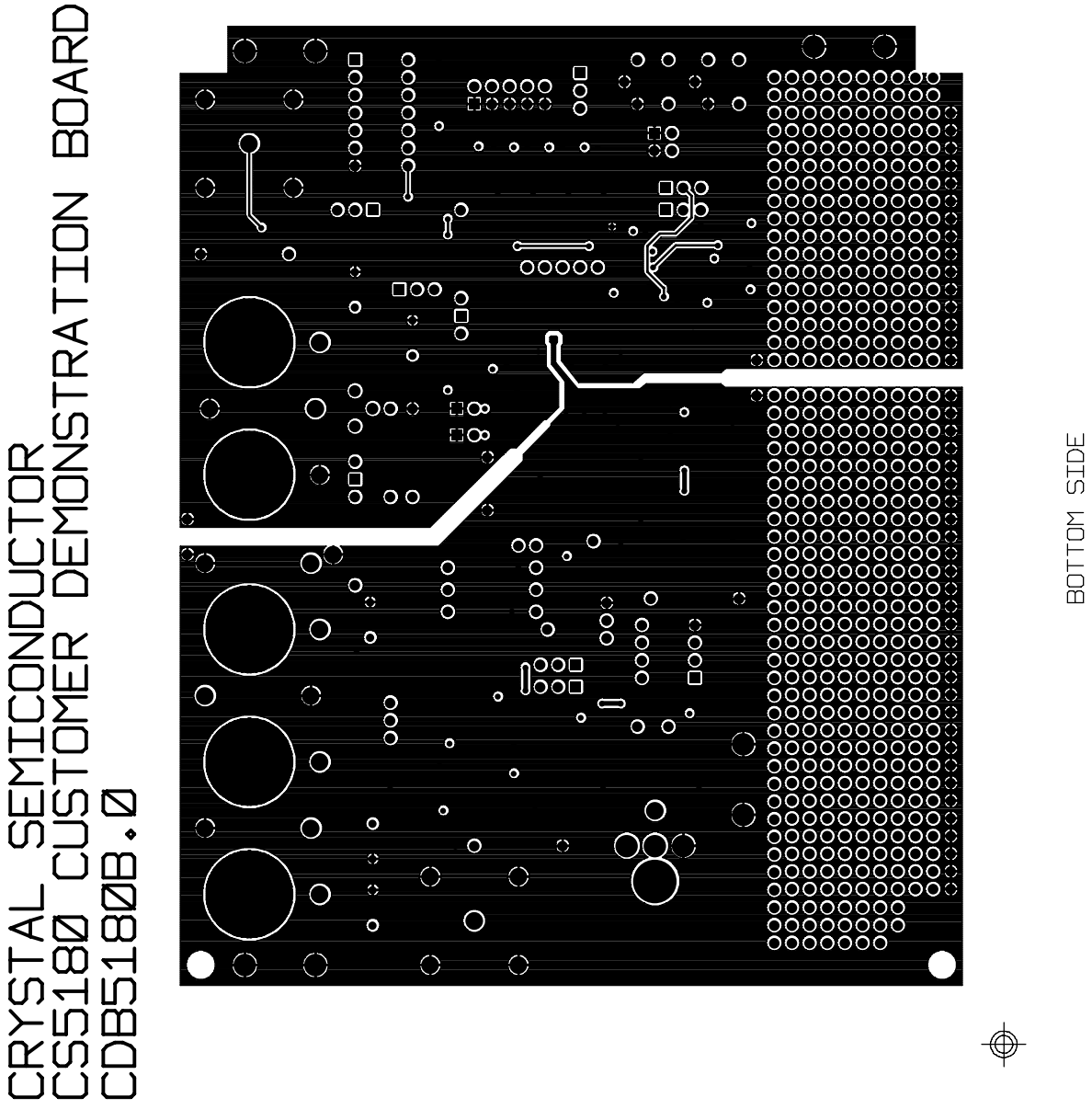

Figure 9. Bottom Side Traces and Groundplane

• Notes •

Contacting Cirrus Logic Support

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