HM51W16160A Series
HM51W18160A Series

1048576-word × 16-bit Dynamic Random Access Memory

HITACHI

ADE-203-217B (Z)
Rev. 2.0
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Description

The Hitachi HM51W16160A Series, HM51W18160A Series are CMOS dynamic RAMs organized as 1,048,576-word × 16-bit. They employ the most advanced CMOS technology for high performance and low power. The HM51W16160A Series, HM51W18160A Series offer Fast Page Mode as a high speed access mode. They have package variations of 42-pin plastic SOJ and 50-pin plastic TSOP II.

Features

- Single 3.3 V (±0.3 V)
- High speed
  - — Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode : 360 mW/324 mW/288 mW (max) (HM51W16160A Series)
    : 612 mW/540 mW/468 mW (max) (HM51W18160A Series)
  - — Standby mode : 7.2 mW (max)
    : 0.54 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - — 4096 refresh cycles : 64 ms (HM51W16160A Series)
    : 128 ms (L-version)
  - — 1024 refresh cycles : 16 ms (HM51W18160A Series)
    : 128 ms (L-version)

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

Hitachi semiconductor

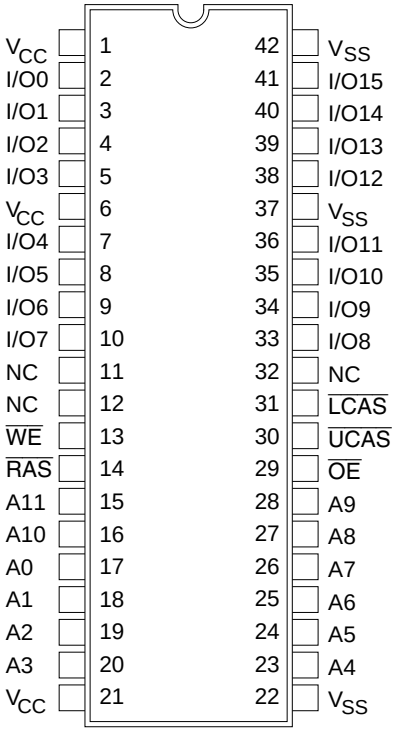
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM51W16160AJ-6	60 ns	400-mil 42-pin plastic SOJ (CP-42D)
HM51W16160AJ-7	70 ns	
HM51W16160AJ-8	80 ns	
HM51W16160ALJ-6	60 ns	
HM51W16160ALJ-7	70 ns	
HM51W16160ALJ-8	80 ns	
HM51W18160AJ-6	60 ns	
HM51W18160AJ-7	70 ns	
HM51W18160AJ-8	80 ns	
HM51W18160ALJ-6	60 ns	
HM51W18160ALJ-7	70 ns	
HM51W18160ALJ-8	80 ns	
HM51W16160ATT-6	60 ns	400-mil 50-pin plastic TSOP II (TTP-50/44DC)
HM51W16160ATT-7	70 ns	
HM51W16160ATT-8	80 ns	
HM51W16160ALTT-6	60 ns	
HM51W16160ALTT-7	70 ns	
HM51W16160ALTT-8	80 ns	
HM51W18160ATT-6	60 ns	
HM51W18160ATT-7	70 ns	
HM51W18160ATT-8	80 ns	
HM51W18160ALTT-6	60 ns	
HM51W18160ALTT-7	70 ns	
HM51W18160ALTT-8	80 ns	

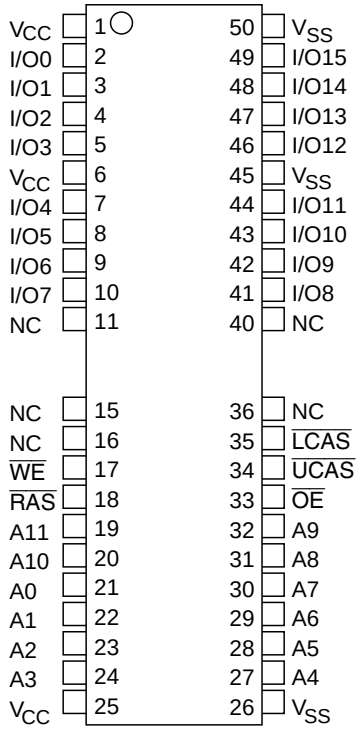
Pin Arrangement

HM51W16160AJ/ALJ Series



(Top view)

HM51W16160ATT/ALTT Series



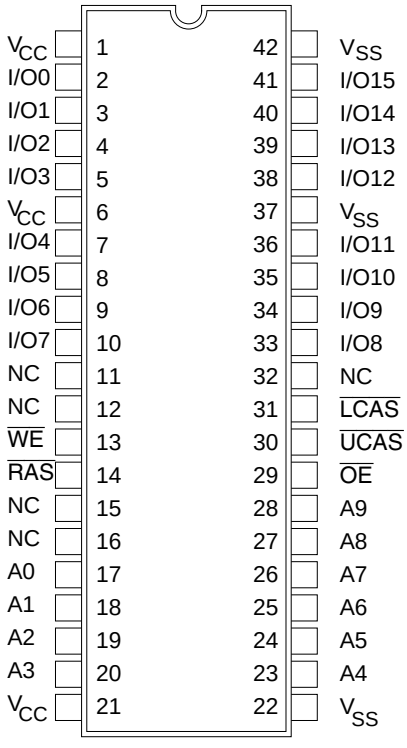
(Top view)

Pin Description

Pin name	Function	
A0 to A11	Address input — Row/Refresh address — Column address	 A0 to A11 A0 to A7
I/O0 to I/O15	Data input/Data output	
$\overline{RAS}$	Row address strobe	
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe	
$\overline{WE}$	Read/Write enable	
$\overline{OE}$	Output enable	
V_{CC}	Power supply	
V_{SS}	Ground	
NC	No connection	

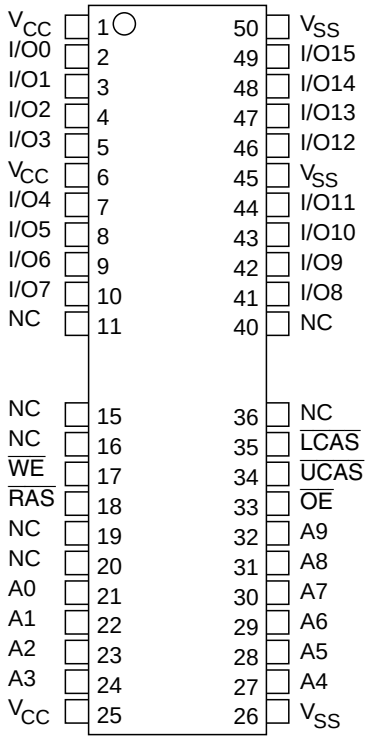
Pin Arrangement

HM51W18160AJ/ALJ Series



(Top view)

HM51W18160ATT/ALTT Series

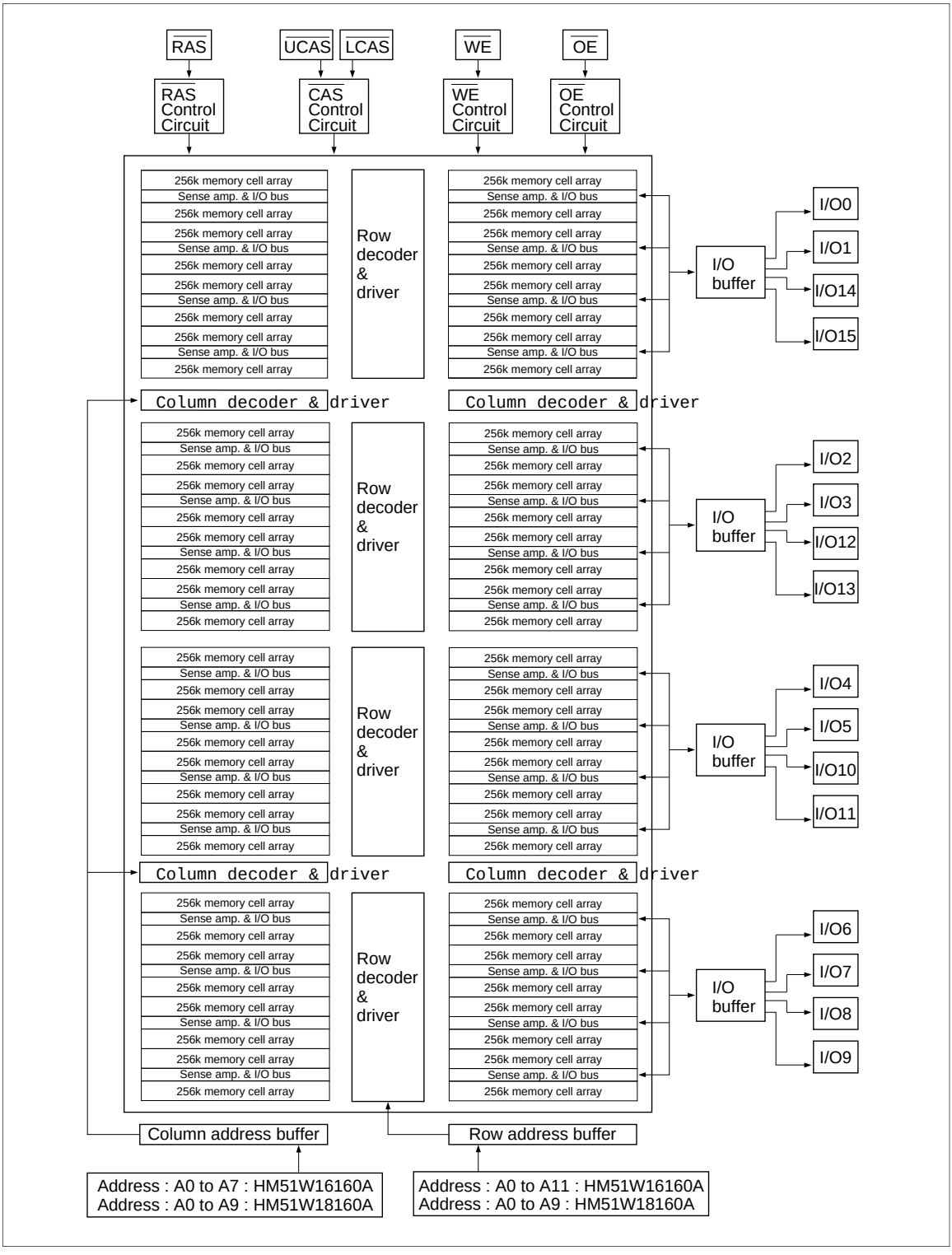


(Top view)

Pin Description

Pin name	Function	
A0 to A9	Address input	
	— Row/Refresh address	A0 to A9
	— Column address	A0 to A9
I/O0 to I/O15	Data input/Data output	
$\overline{RAS}$	Row address strobe	
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe	
$\overline{WE}$	Read/Write enable	
$\overline{OE}$	Output enable	
V_{CC}	Power supply	
V_{ss}	Ground	
NC	No connection	

Block Diagram



Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Output		Operation
H	D	D	D	D	Open		Standby
L	L	H	H	L	Valid	Lower byte	Read cycle
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L*[2]	D	Open	Lower byte	Early write cycle
L	H	L	L*[2]	D	Open	Upper byte	
L	L	L	L*[2]	D	Open	Word	
L	L	H	L*[2]	H	Undefined	Lower byte	Delayed write cycle
L	H	L	L*[2]	H	Undefined	Upper byte	
L	L	L	L*[2]	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
L	H	H	D	D	Open	Word	$\overline{RAS}$-only refresh cycle
H to L	H	L	D	D	Open	Word	$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or
H to L	L	H	D	D	Open	Word	Self refresh cycle (L-version)
H to L	L	L	D	D	Open	Word	
L	L	L	H	H	Open		Read cycle (Output disabled)

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{WCS} \geq 0$ ns Early write cycle

   $t_{WCS} < 0$ ns Delayed write cycle

3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.

   ex. if $\overline{RAS}$ = H to L, $\overline{UCAS}$ = H, $\overline{LCAS}$ = L, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 V (max))	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W16160A Series)

		HM51W16160A							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	100	—	90	—	80	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	100	—	90	—	80	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	100	—	90	—	80	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	100	—	90	—	80	mA	t_{PC} = min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	400	—	400	—	400	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 31.3 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	250	—	250	—	250	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W18160A Series)

		HM51W18160A							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current*1, *2	I_{CC1}	—	170	—	150	—	130	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	170	—	150	—	130	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	170	—	150	—	130	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	170	—	150	—	130	mA	t_{PC} = min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	400	—	400	—	400	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 125 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	250	—	250	—	250	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≤ 0.2 V Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH} to disable Dout.

AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *1, *2, *18, *19, *20

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	21
Column address hold time	t_{CAH}	10	—	15	—	15	—	ns	21
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	20	60	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	23
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	22
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	20	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7

Read Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	15	—	18	—	20	ns	9, 25
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	–	0	—	ns	12, 22
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	—	35	—	40	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	5

Write Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14, 21
Write command hold time	t_{WCH}	10	—	15	—	15	—	ns	21
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	—	18	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	—	18	—	20	—	ns	23
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15, 23
Data-in hold time	t_{DH}	10	—	15	—	15	—	ns	15, 23

Read-Modify-Write Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	155	—	181	—	205	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	—	98	—	110	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	21
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	22
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	21

Fast Page Mode Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	—	45	ns	9, 17, 22
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM51W16160A/HM51W18160A							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PRWC}	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	60	—	68	—	75	—	ns	14, 22

Refresh (HM51W16160A Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Refresh (HM51W18160A Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	16	ms	1024 cycles
Refresh period (L-version)	t_{REF}	128	ms	1024 cycles

Self Refresh Mode (L-version)

		HM51W16160AL/HM51W18160AL							
		-6		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{RAS}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	100	—	µs	26
$\overline{RAS}$ precharge time (Self refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (Self refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF. (V_{OH} = 2.0 V, V_{OL} = 0.8 V)
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} < t_{CWL}$, invalid data will be out at each I/O.
19. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. t_{CWL}, t_{DH} and t_{DS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.

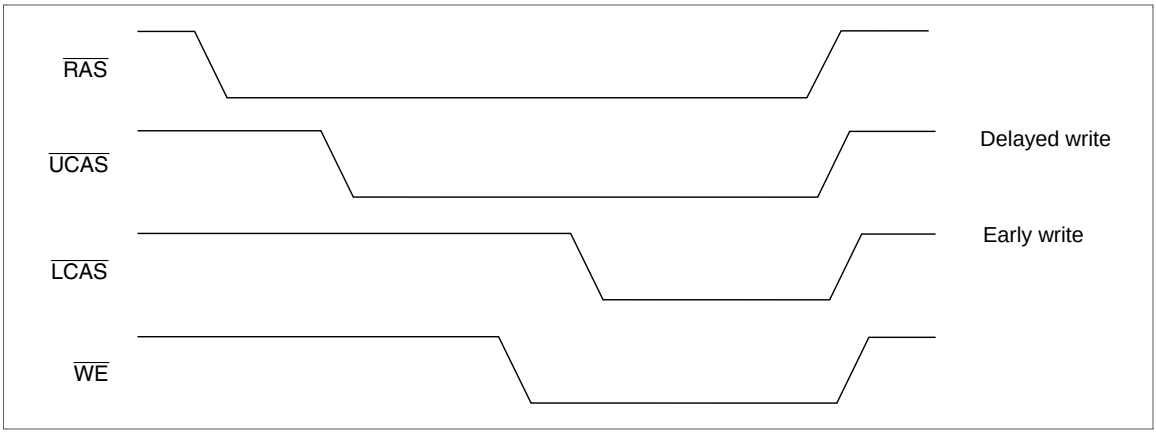
24. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
26. Please do not use t_{RASS} timing, 10 μs ≤ t_{RASS} ≤ 100 μs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 μs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
27. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
28. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles (4096 cycles: HM51W16160A Series, 1024 cycles: HM51W18160A Series) of distributed CBR refresh with 15.6 μs interval should be executed within 64 or 16 ms (64 ms: HM51W16160A, 16 ms: HM51W18160A) immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
30. ⊠ H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))
    ▨ Invalid Dout

Notes concerning 2$\overline{CAS}$ control

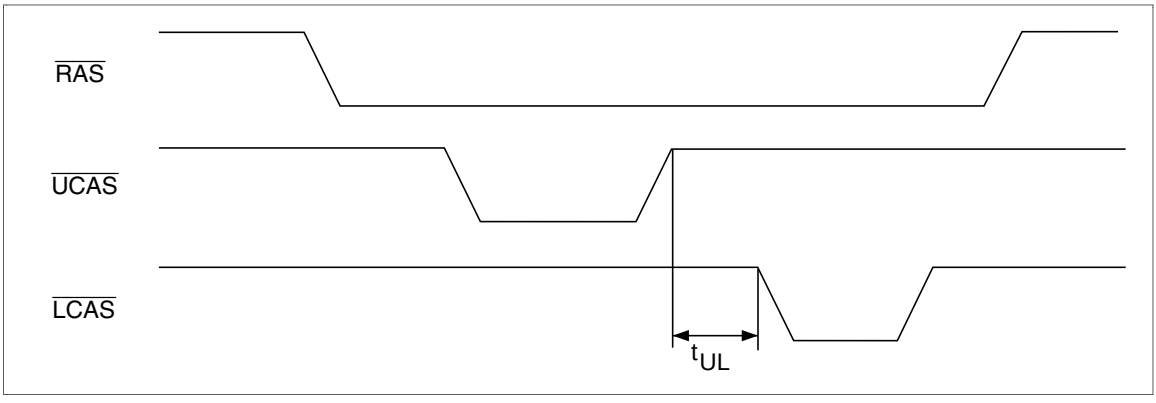
Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between UCAS/LCAS are allowed under the following conditions.

1. Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.

2. Different operation mode for upper/lower byte is not allowed; such as following.



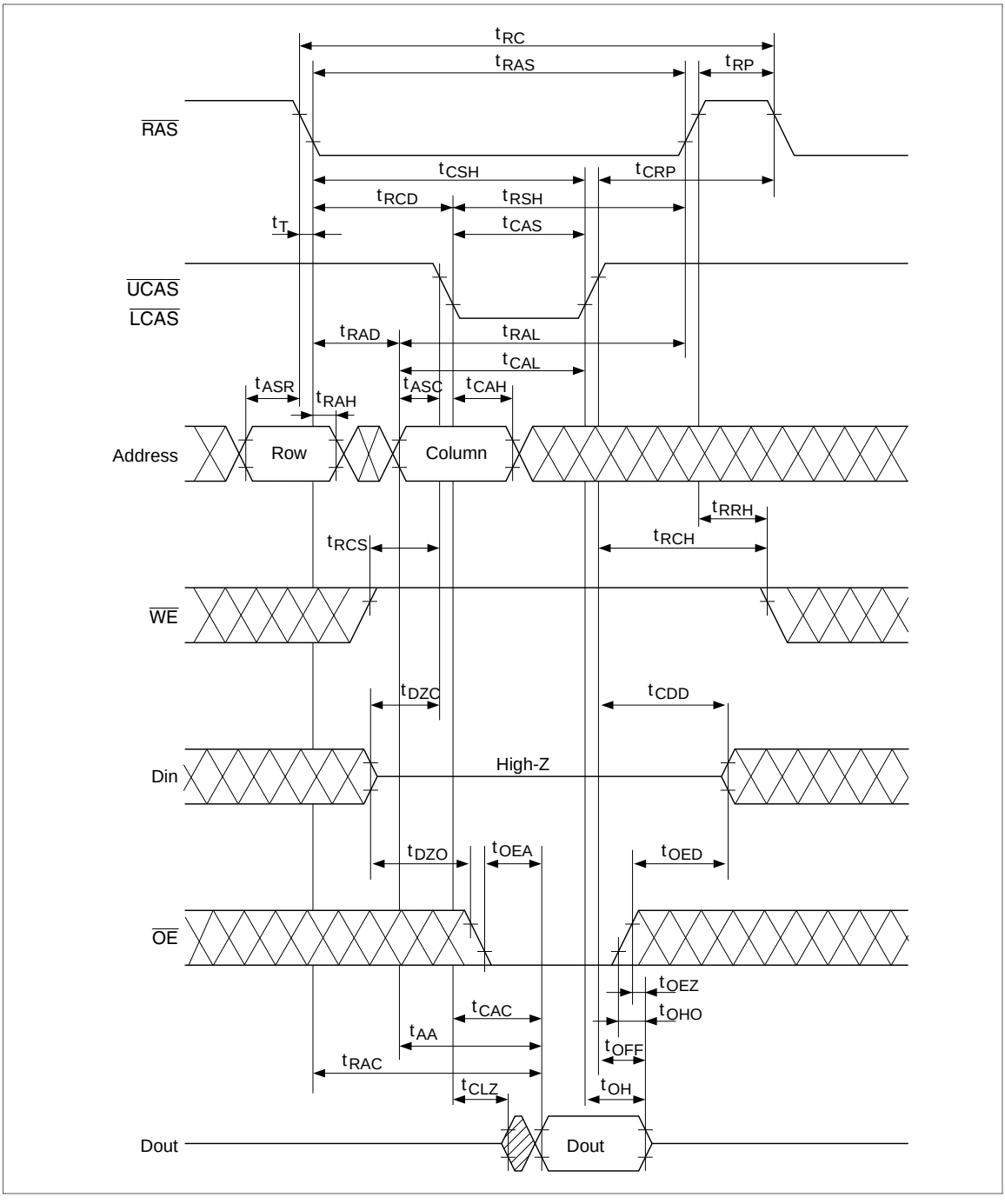
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



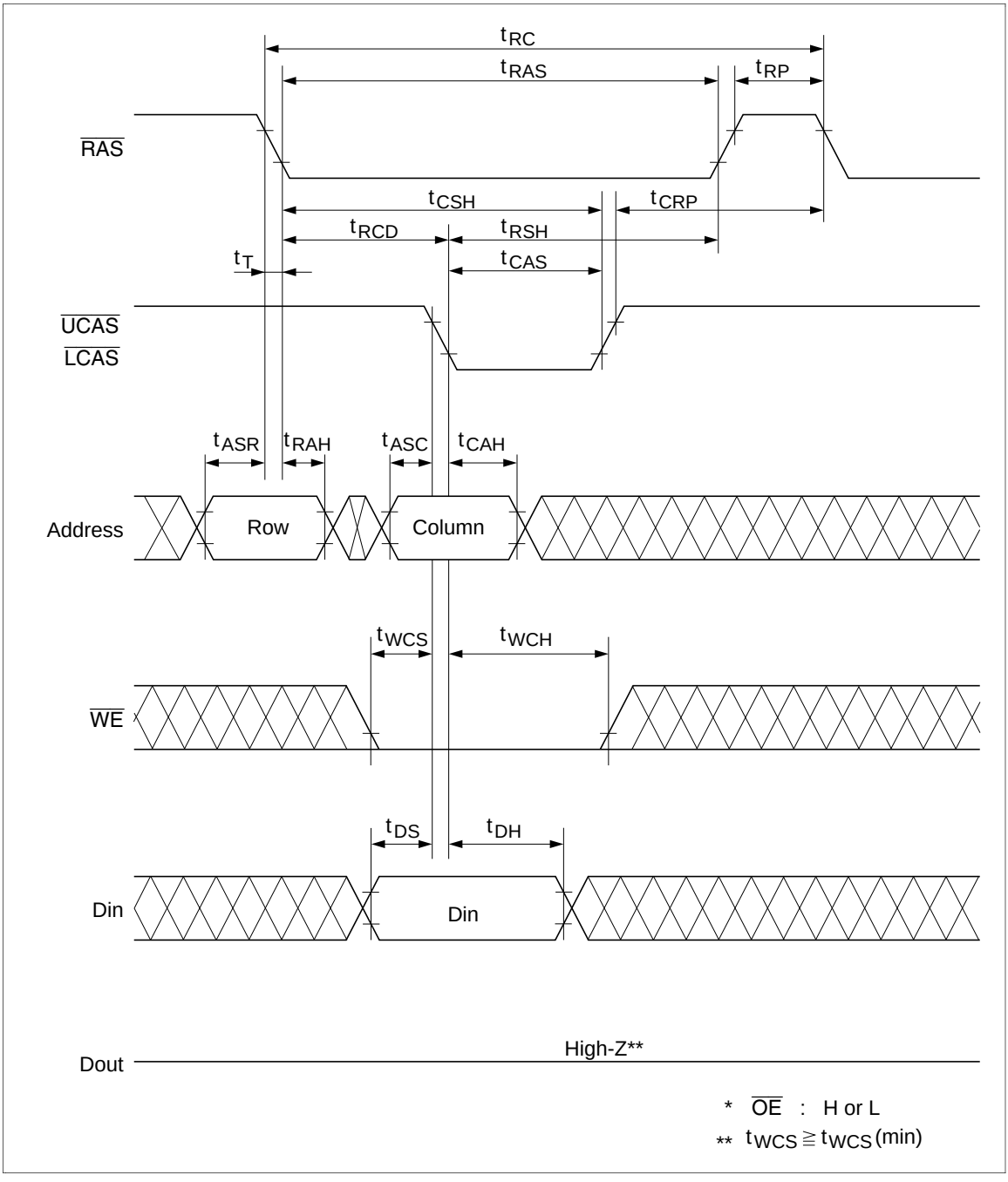
4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

Timing Waveforms*[30]

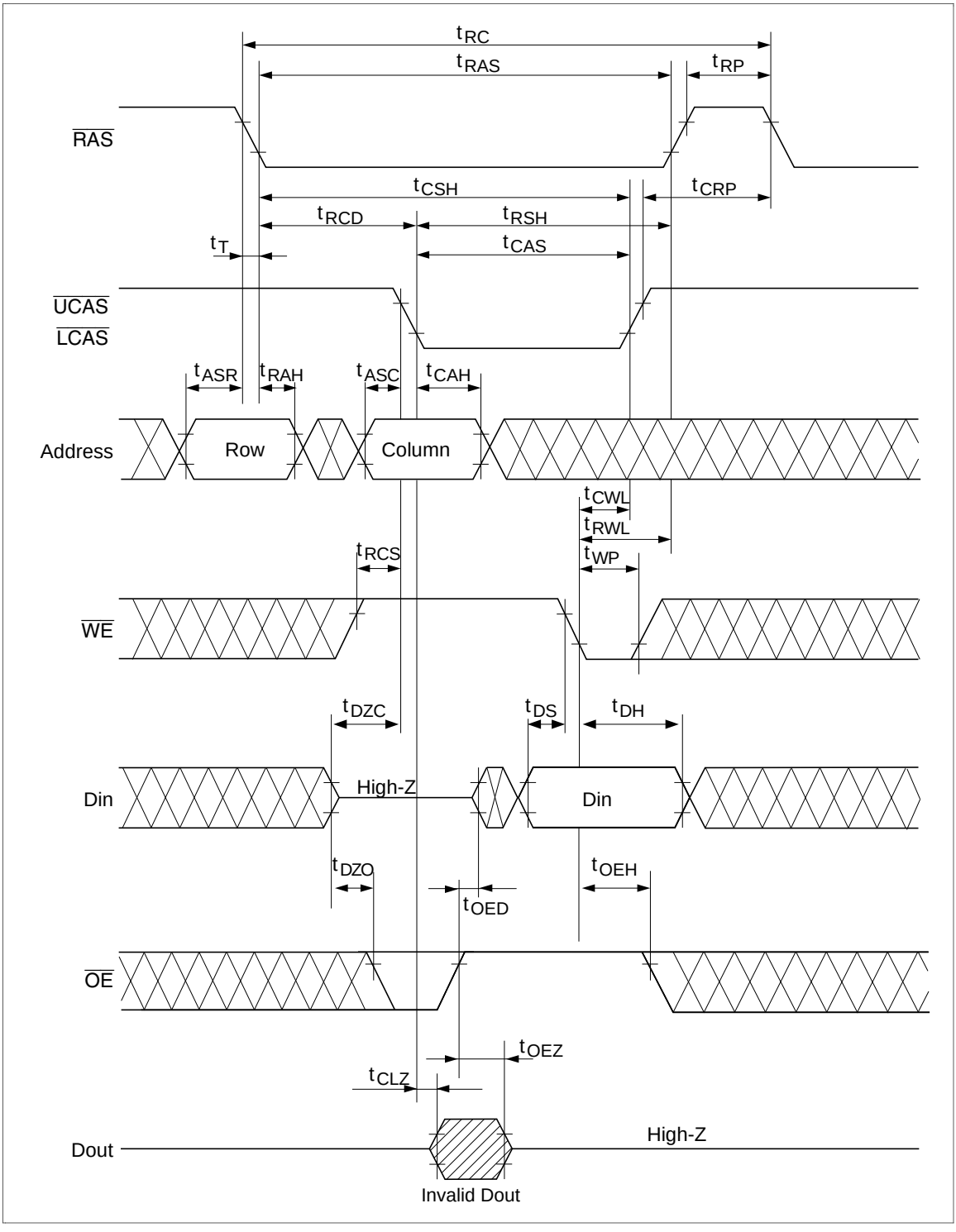
Read Cycle



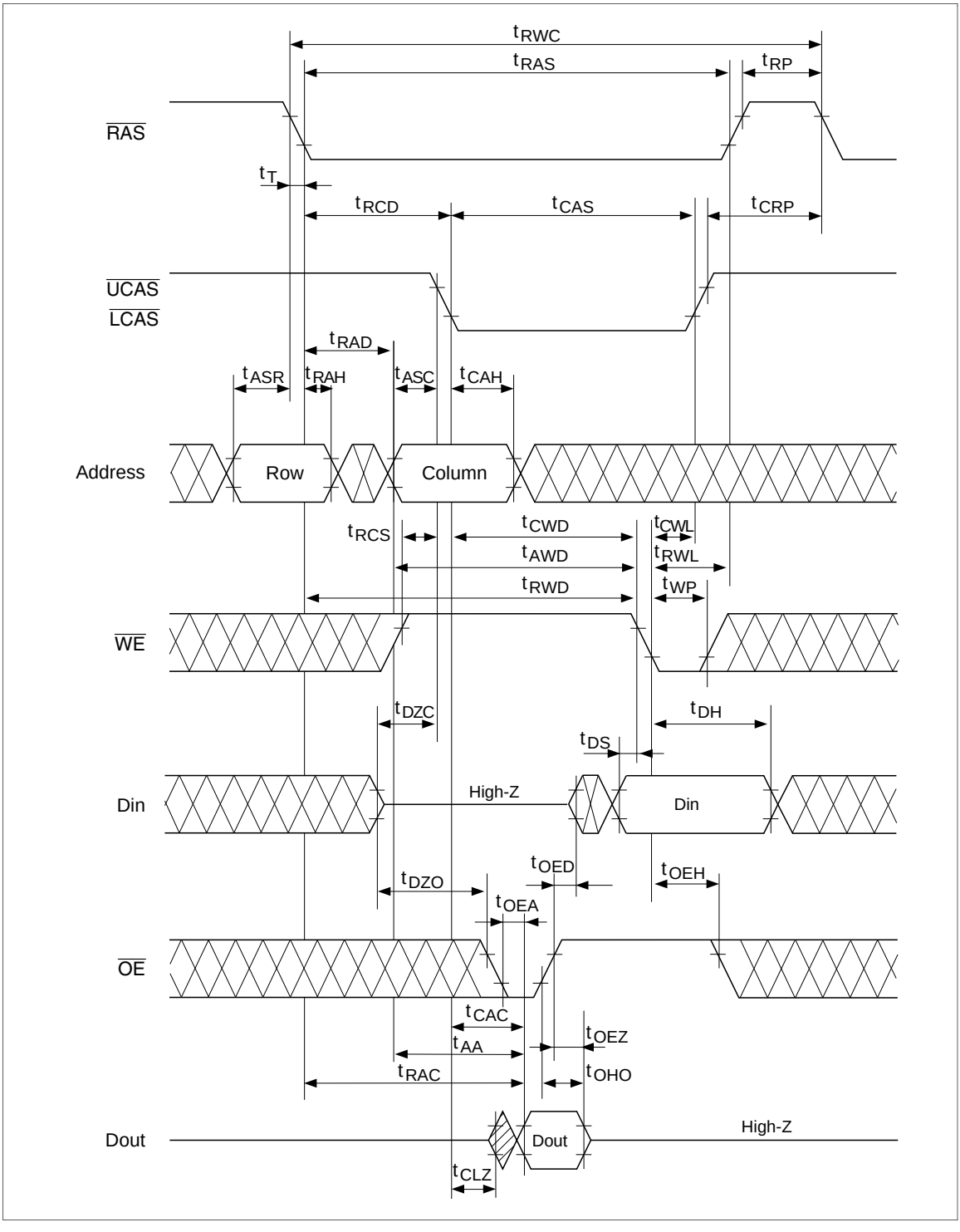
Early Write Cycle



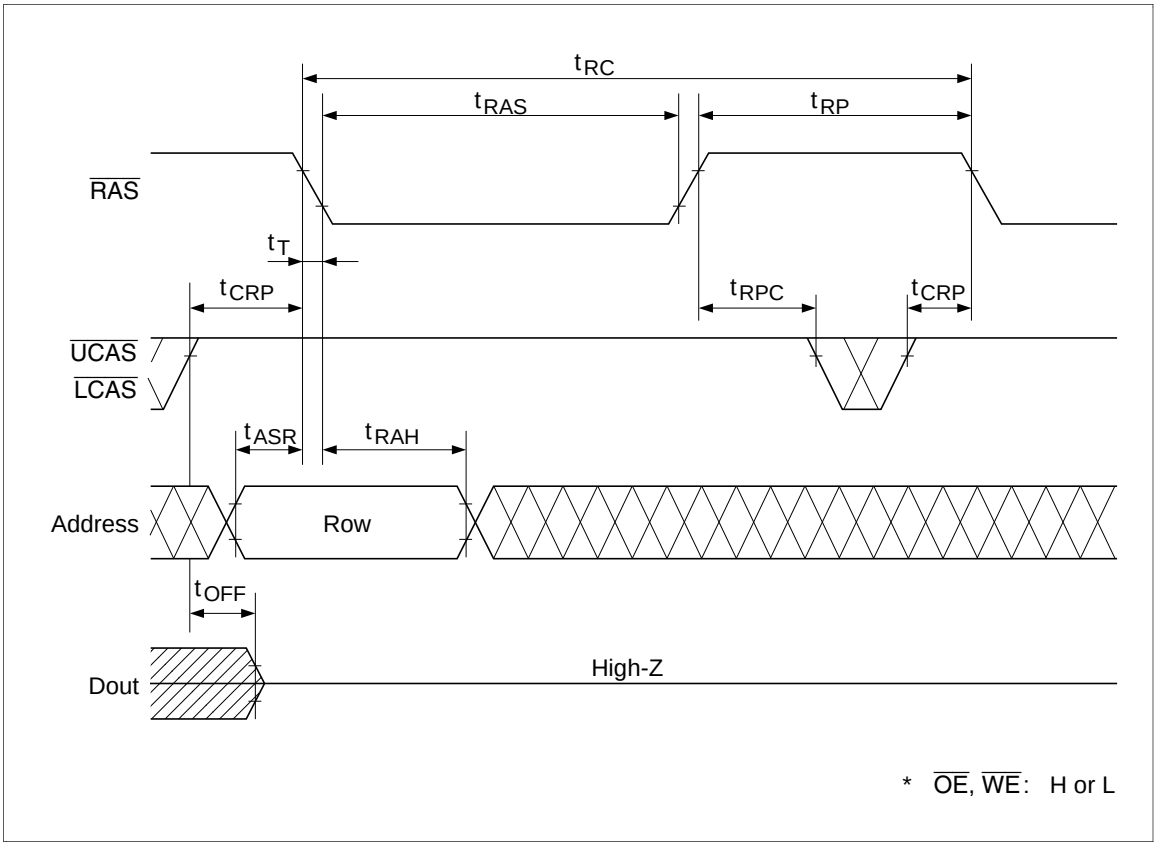
Delayed Write Cycle*[18]



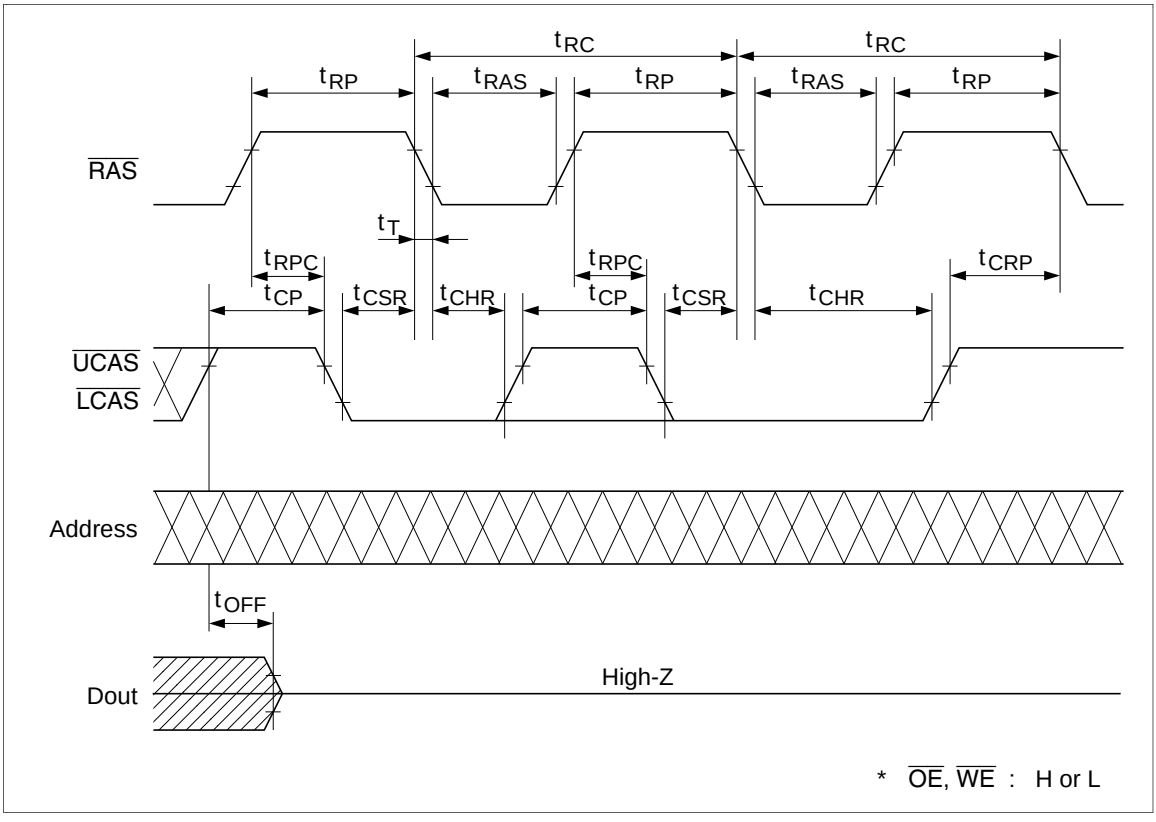
Read-Modify-Write Cycle*[18]



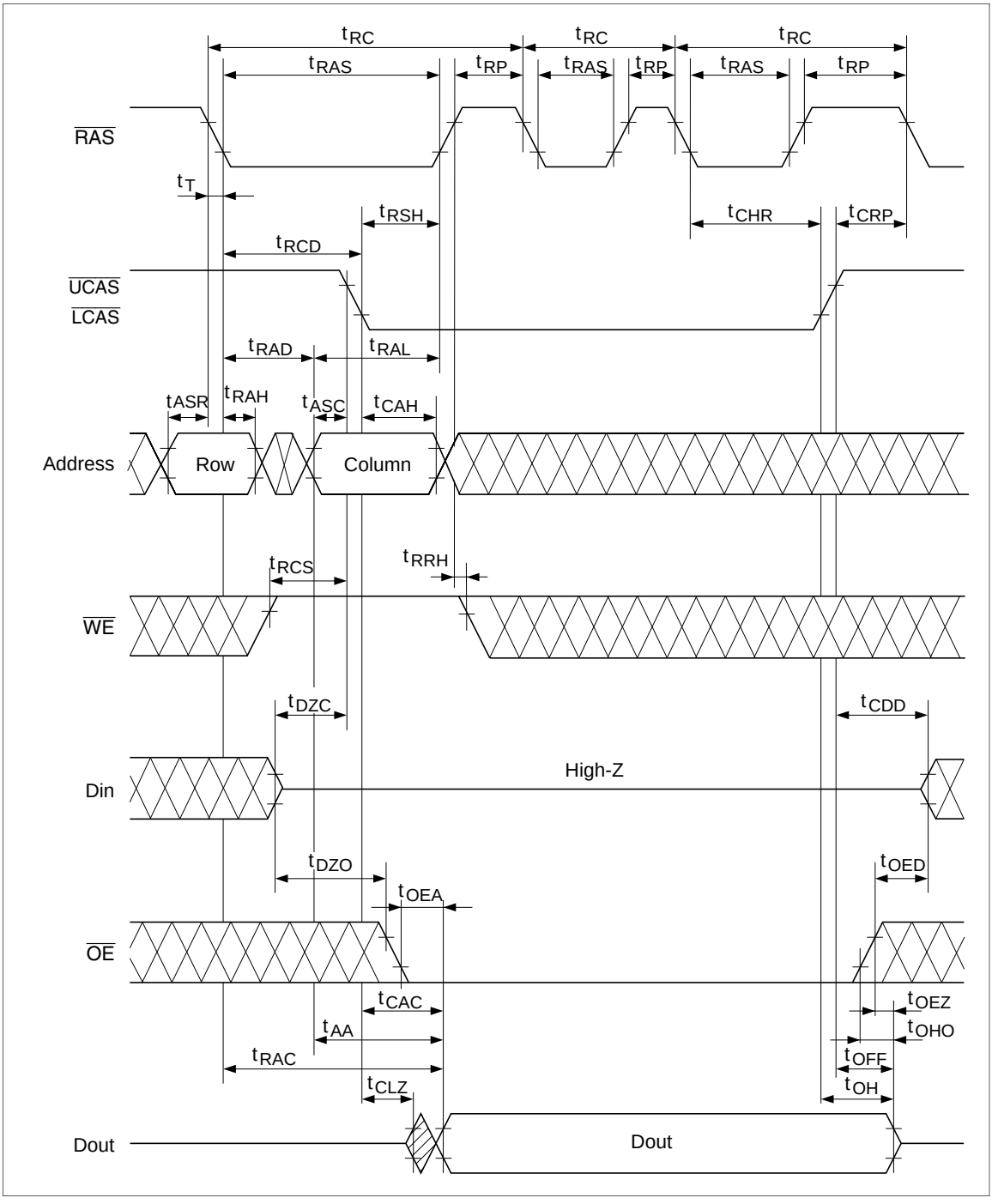
$\overline{\text{RAS}}$-Only Refresh Cycle



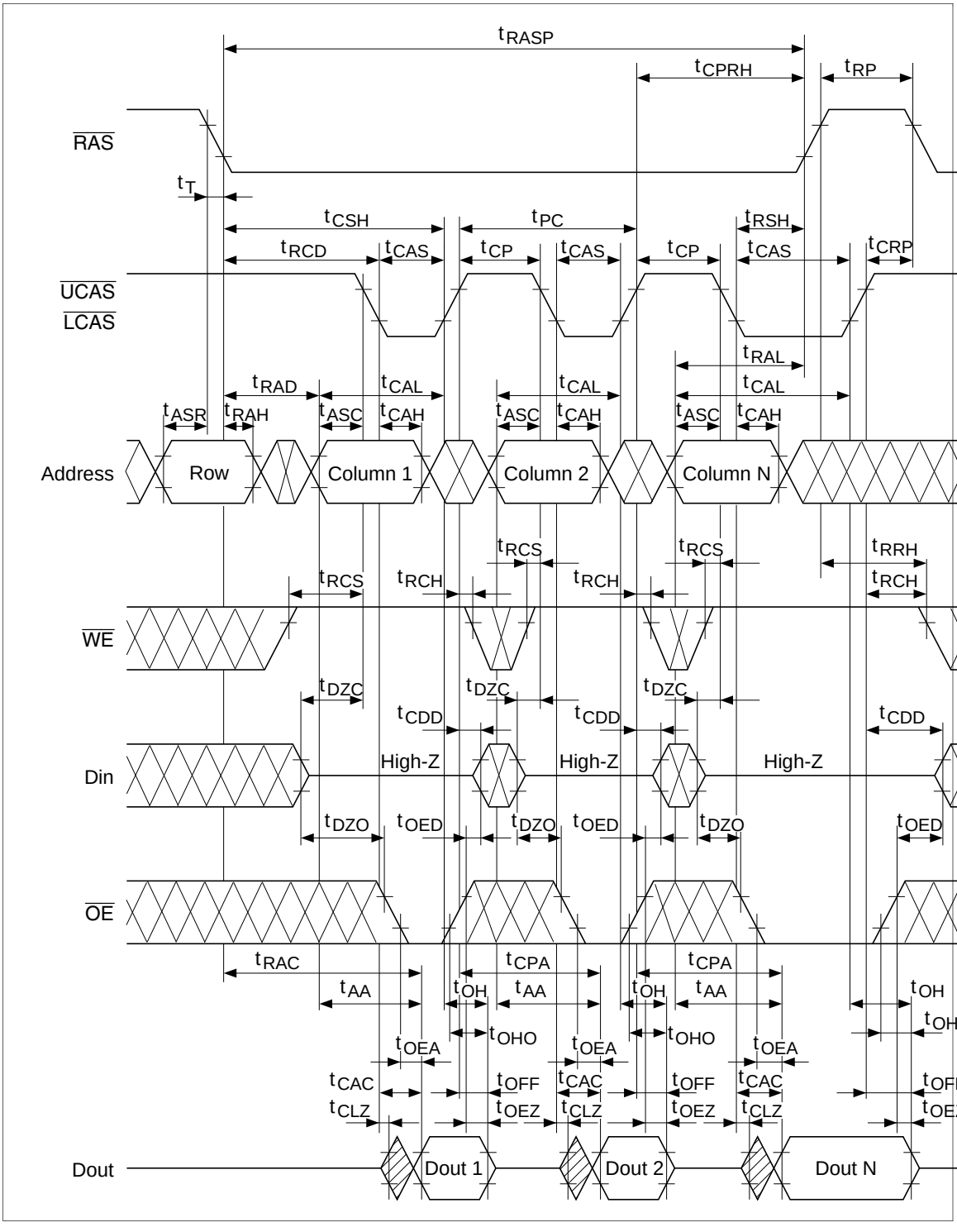
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



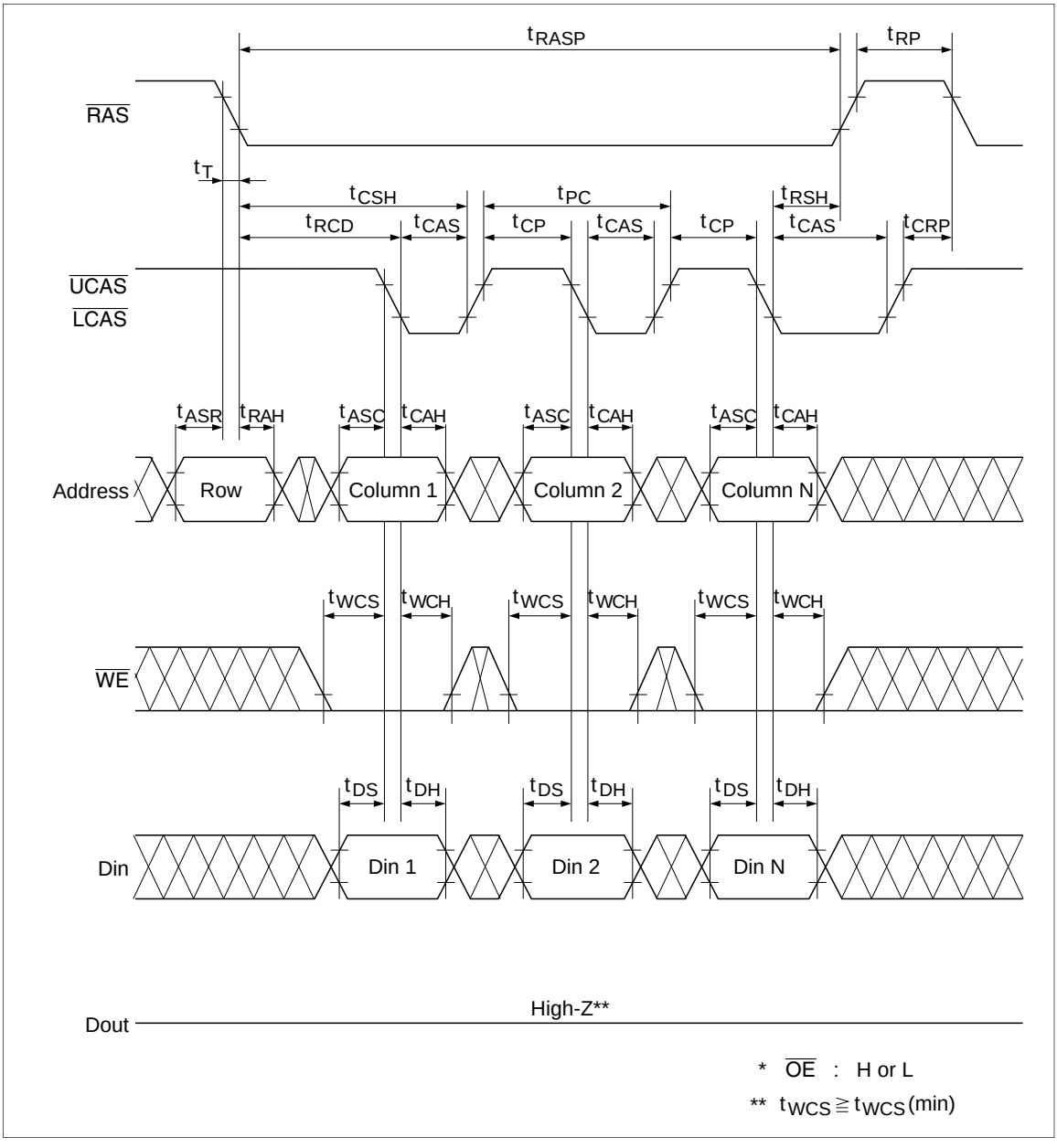
Hidden Refresh Cycle



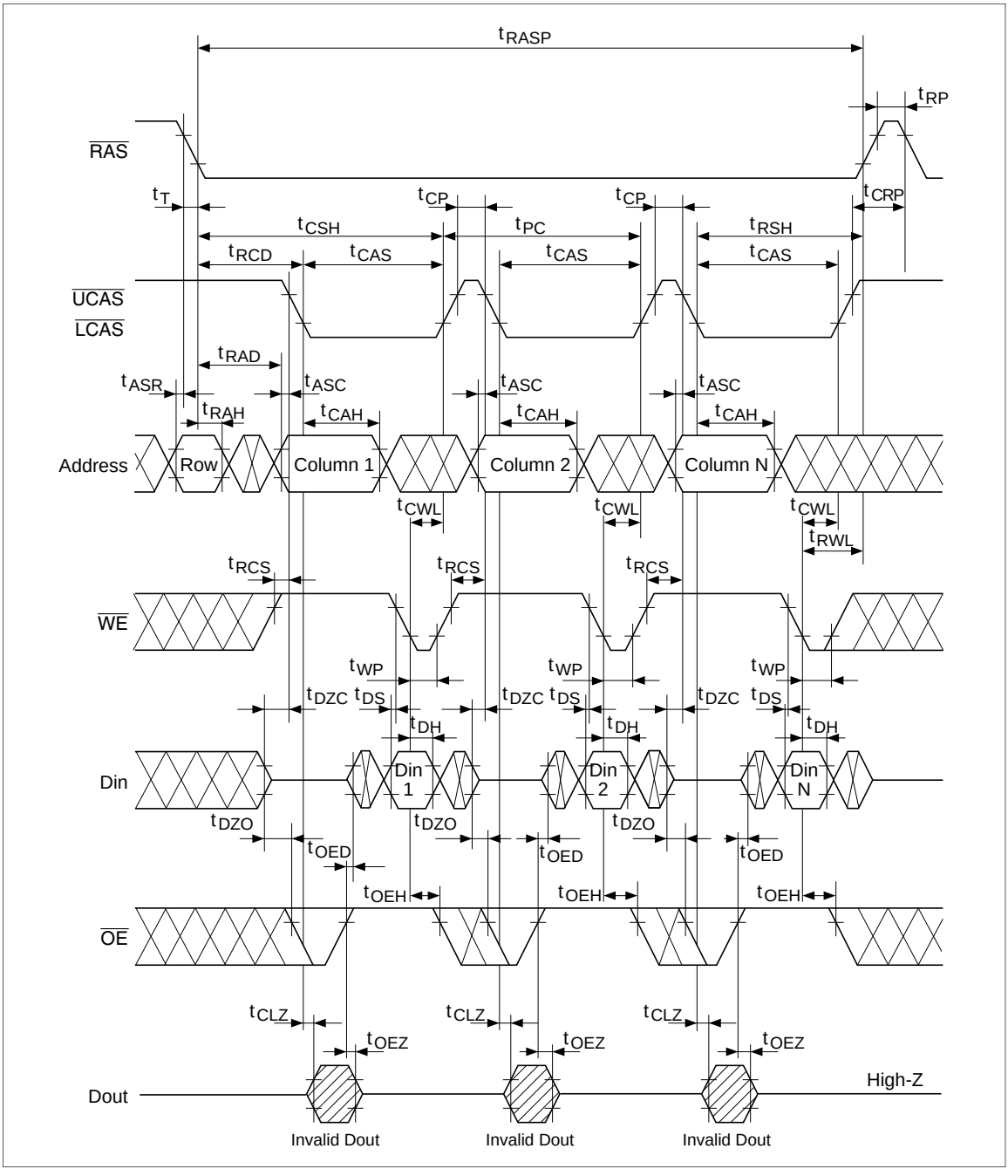
Fast Page Mode Read Cycle



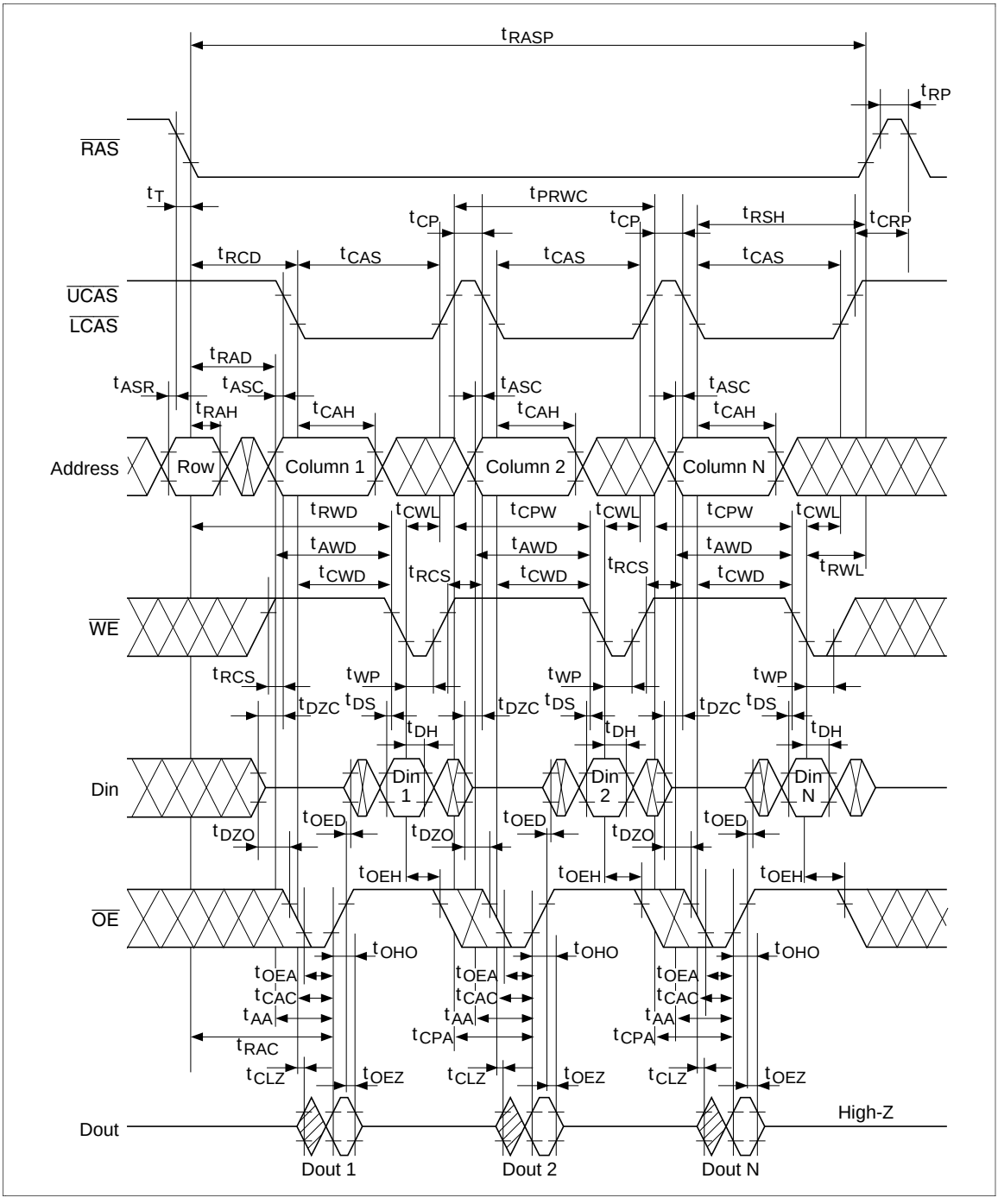
Fast Page Mode Early Write Cycle



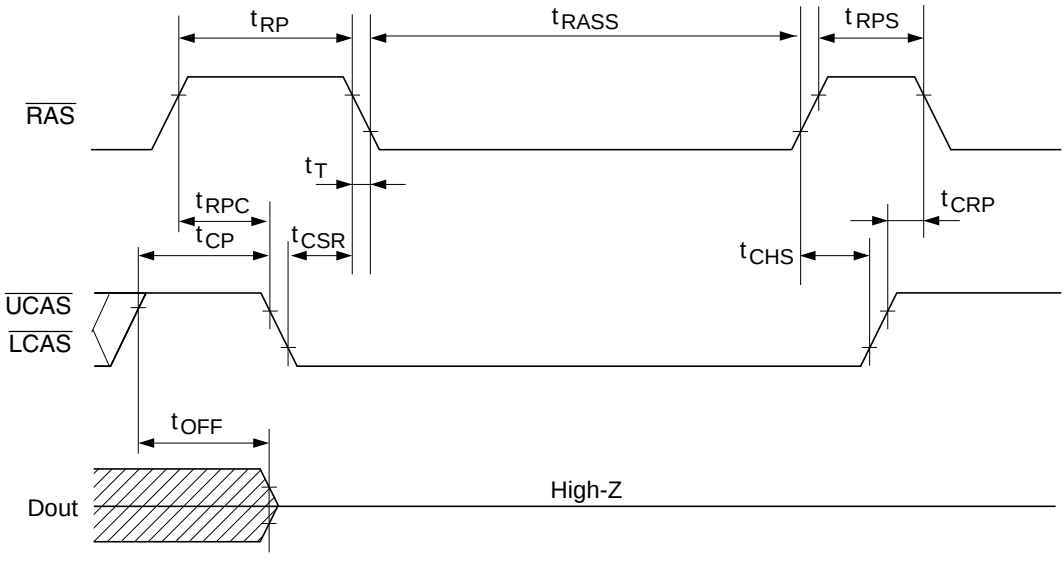
Fast Page Mode Delayed Write Cycle*[18]



Fast Page Mode Read-Modify-Write Cycle*[18]



Self Refresh Cycle (L-version)*[26, 27, 28, 29]

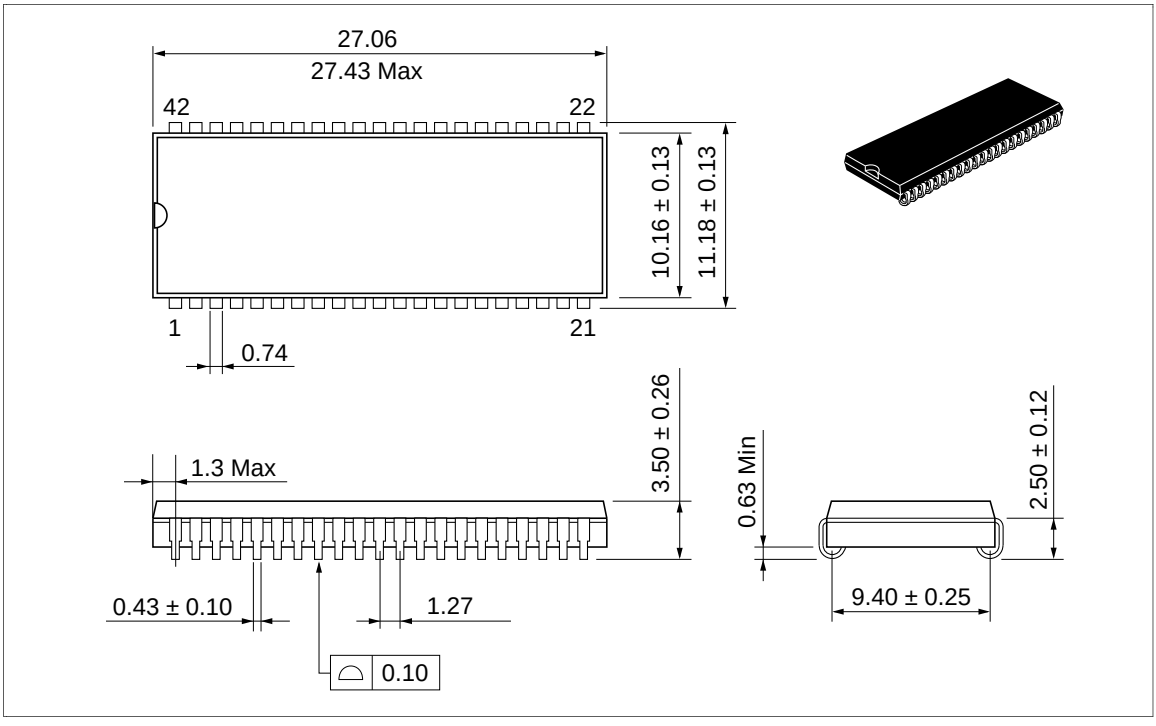


*Address, $\overline{OE}$, $\overline{WE}$: H or L

Package Dimensions

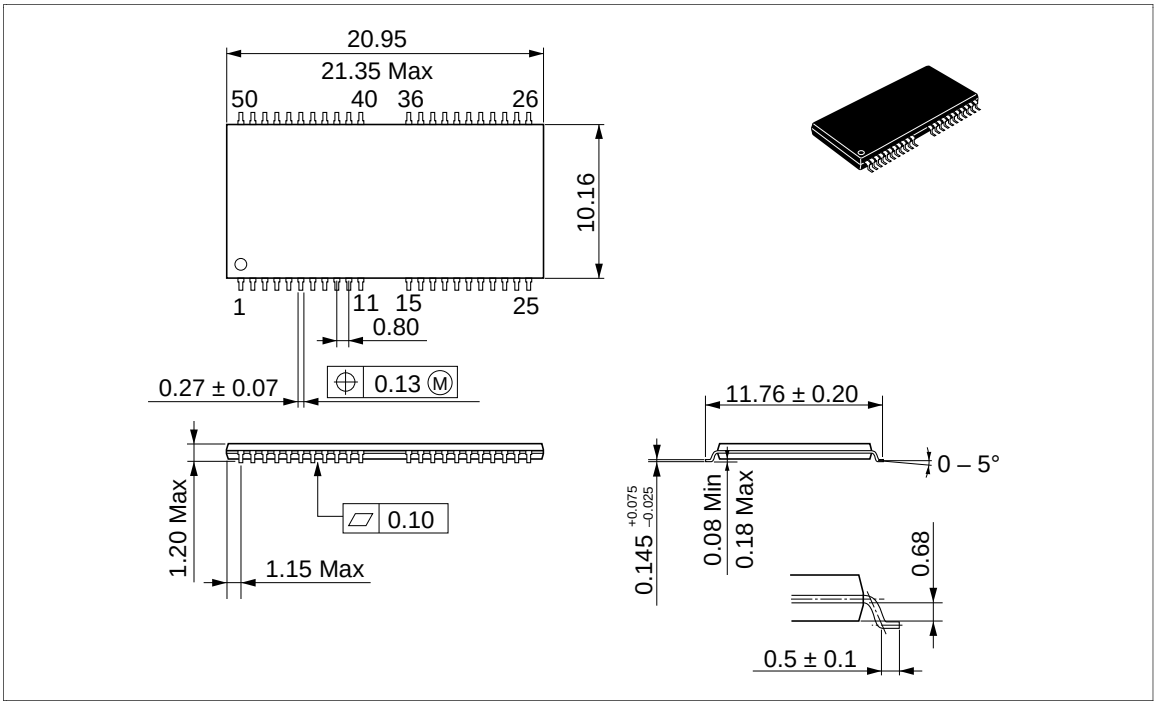
HM51W16160AJ/ALJ Series

HM51W18160AJ/ALJ Series (CP-42D) Unit: mm



HM51W16160ATT/ALTT Series

HM51W18160ATT/ALTT Series (TTP-50/44DC) Unit: mm



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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Feb. 17, 1994	Initial issue	H. Yoshioka	M. Yamamura
0.1	Jun. 1, 1994	Pin Arrangement Addition of Description for JEDEC pin number DC Characteristics I_{CC10} max: 300/300/300 µA to 0.4/0.4/0.4 mA AC Characteristics Deletion of t_{CPT} min: 20/20/20 ns Deletion of note 25 Change of note 2 Timing waveforms Deletion of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Check Cycle	M. Mishima	H. Iijima
1.0	Oct. 12, 1995	Change format Change format of truth table Recommended DC Operating condition Addition of note 2 DC Characteristics I_{CC2} max: 0.1/0.1/0.1 mA to 150/150/150 µA I_{CC11} max: 200/200/200 µA to 250/250/250 µA Addition of note 4 AC Characteristics t_{RRH} min: 0/0/0 ns to 5/5/5 ns Change of notes 11, 12 Addition of note 25: t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high Package dimensions: CP-42D Package overhang: 1.265 mm to 1.3 mm Max	M. Mishima	K. Hayakawa
2.0	Jul. 2, 1996	Unification of HM51W16160A/HM51W18160A Series Change format Addition of HM51W18160A-6 Series Pin Description Addition of Row/Refresh address and Column address to address input AC Characteristics Deletion of note 3: Only row address is indispensable on addrress A8, A9, A10, A11 Notes concerning 2$\overline{CAS}$ control Addition of note 4 Timing waveforms Deletion of note: $t_{OEH} \geq t_{CWE}$ Deletion of notes for $\overline{RAS}$-only refresh cycle		