HN58V65A Series
HN58V66A Series

8192-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-539 (Z)
Preliminary
Rev. 0.1
Nov. 12, 1996

Description

The Hitachi HN58V65A series and HN58V66A series are a electrically erasable and programmable EEPROM's organized as 8192-word × 8-bit. Employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 32-byte page programming function to make their write operations faster.

Features

- Single 2.7 to 5.5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms (max)
- Automatic page write (32 bytes): 10 ms (max)
- Fast access time: 100 ns (max) at 2.7 V ≤ V_{CC} < 4.5 V
  70 ns (max) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Low power dissipation: active: 20 mW/MHz (typ)
  standby: 110 µW (max)
- Ready/$\overline{Busy}$
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change notice.

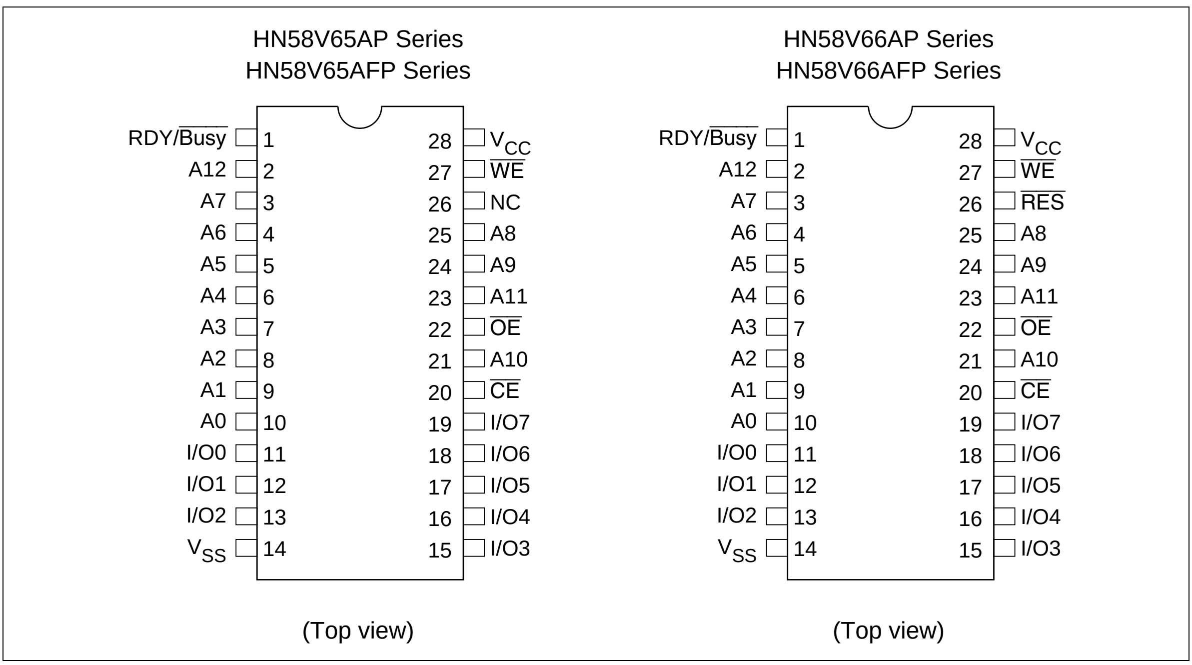
Features (cont)

- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin (only the HN58V66A series)
- Industrial versions (Temperature range: –20 to 85˚C and –40 to 85˚C) are also available.

Ordering Information

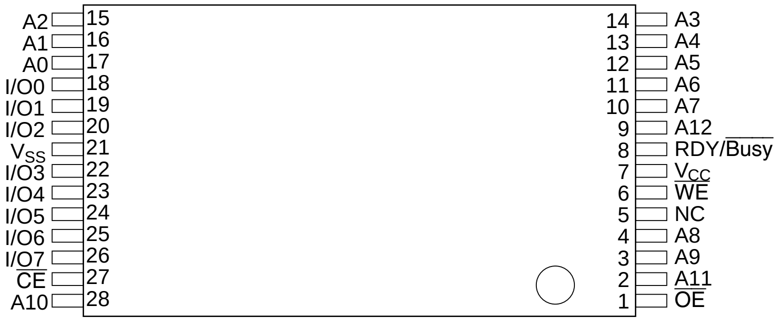
Type No.	Access time 2.7 V ≤ V_{CC} < 4.5 V	 4.5 V ≤ V_{CC} ≤ 5.5 V	Package
HN58V65AP-10	100 ns	70 ns	600 mil 28-pin plastic DIP (DP-28)
HN58V66AP-10	100 ns	70 ns	
HN58V65AFP-10	100 ns	70 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58V66AFP-10	100 ns	70 ns	
HN58V65AT-10	100 ns	70 ns	28-pin plastic TSOP(TFP-28DB)
HN58V66AT-10	100 ns	70 ns	

Pin Arrangement



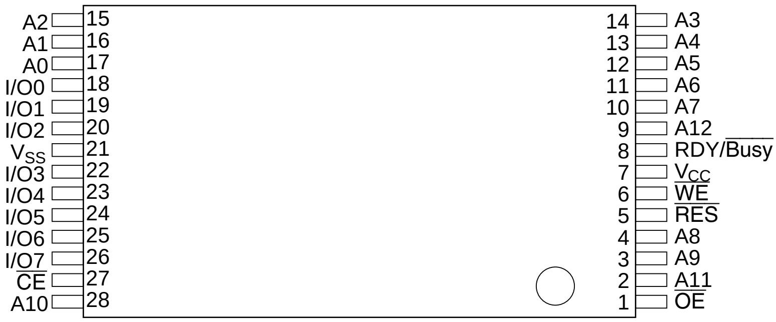
Pin Arrangement (cont)

HN58V65AT Series



(Top view)

HN58V66AT Series



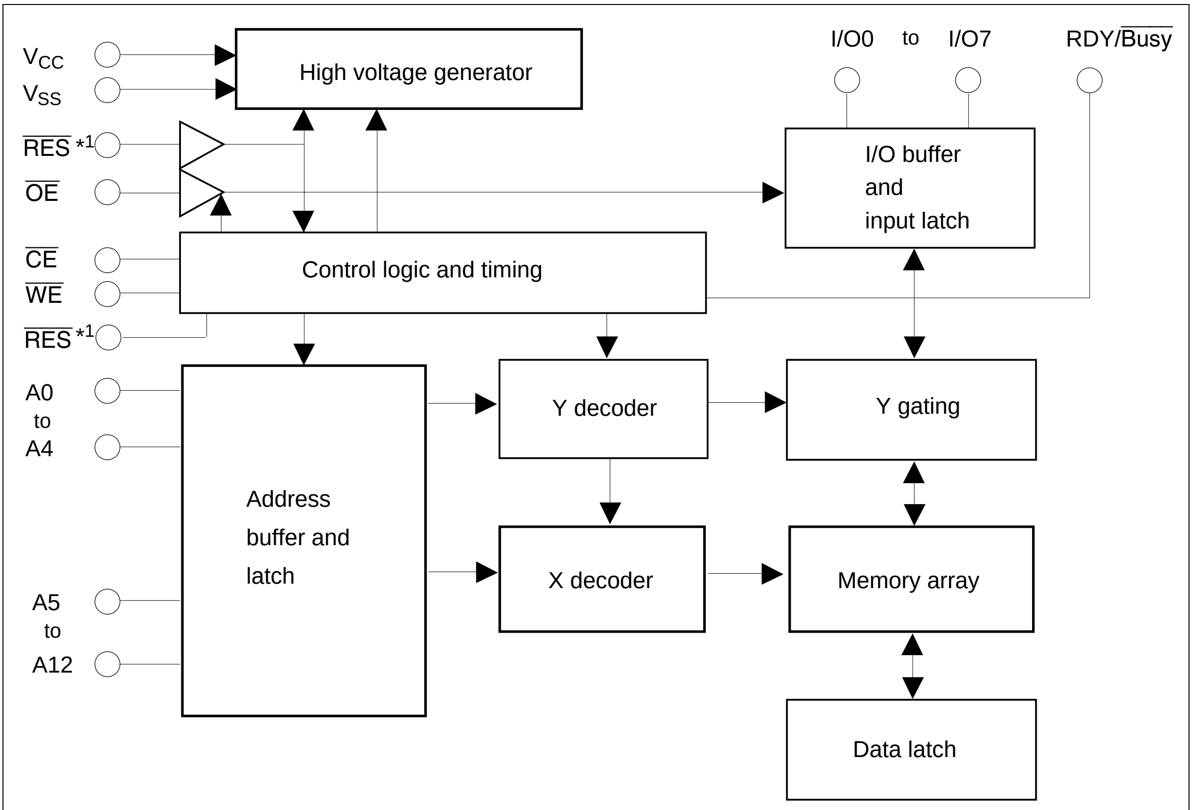
(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O0 to I/O7	Data input/output
$\overline{\text{OE}}$	Output enable
$\overline{\text{CE}}$	Chip enable
$\overline{\text{WE}}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{\text{Busy}}$	Ready busy
$\overline{\text{RES}}$*[1]	Reset
NC	No connection

Notes: 1. This function is supported by only the HN58V66A series.

Block Diagram



Note: 1. This function is supported by only the HN58V66A series.

Mode Selection

Pin mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$*[3]	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*[1]	High-Z	Dout
Standby	V_{IH}	×*[2]	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.
2. × : Don't care
3. This function supported by only the HN58V66A series.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *[1]	V_{CC}	–0.6 to +7.0	V
Input voltage *[1]	Vin	–0.5*[2] to +7.0*[4]	V
Operating temperature range *[3]	Topr	0 to +70	˚C
Storage temperature range	Tstg	–55 to +125	˚C

Notes: 1. With respect to V_{SS}.
2. Vin min : –3.0 V for pulse width ≤ 50 ns.
3. Including electrical characteristics and data retention.
4. Should not exceed V_{CC} + 1 V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	–0.3*[1]	—	0.6	V
	V_{IH}	1.9*[2]	—	V_{CC} + 0.3*[3]	V
	V_H*[4]	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	˚C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} = 2.4 V for V_{CC} = 3.6 to 5.5 V.
3. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.
4. This function is supported by only the HN58V66A series.

DC Characteristics (Ta = 0 to + 70˚C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*[1]	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	6	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	10	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 100 ns at V_{CC} = 3.6 V
		—	—	25	mA	Iout = 0 mA, Duty = 100%, Cycle = 70 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max (only the HN58V66A series)

Capacitance (Ta = 25˚C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin*[1]	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*[1]	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to + 70˚C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

- Input pulse levels : 0.4 V to 2.4 V (V_{CC} = 2.7 to 3.6 V), 0.4 V to 3.0 V (V_{CC} = 3.6 to 5.5 V)
  0.4 V to V_{CC} ($\overline{RES}$ pin*[2])
- Input rise and fall time : ≤ 5 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle 1 (V_{CC} = 2.7 to 4.5 V)

		HN58V65A/HN58V66A			
		-10			
Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	100	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1, 2]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay*[2]	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

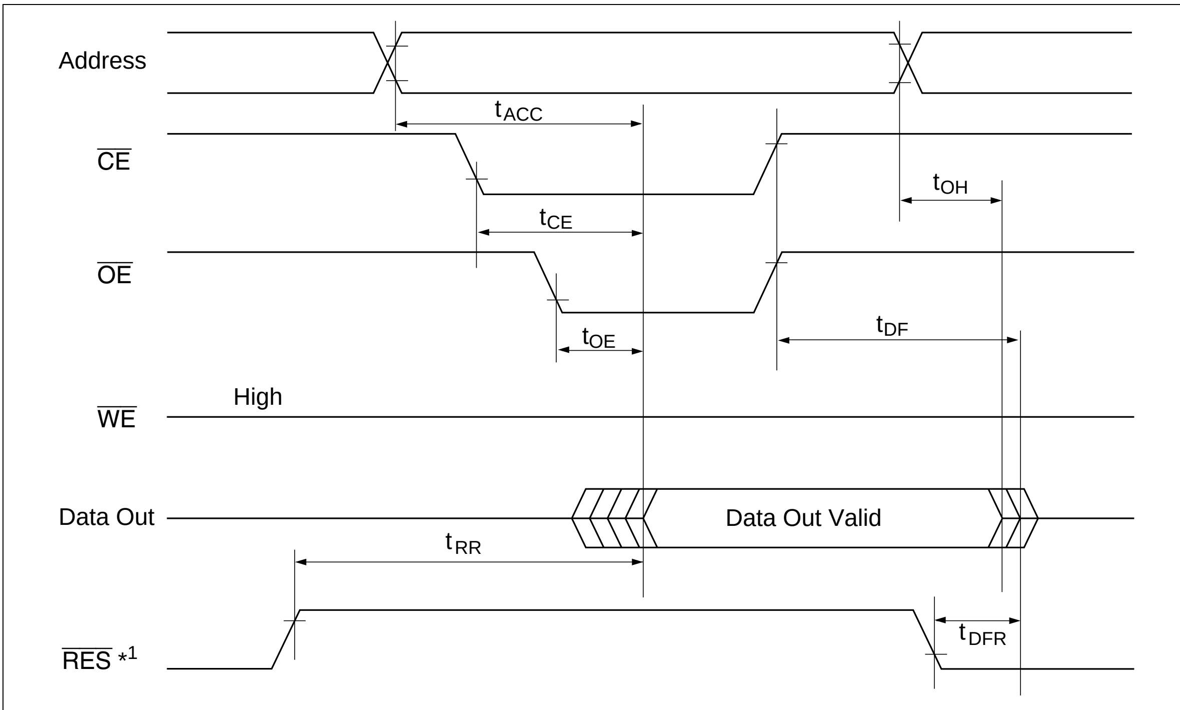
Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. This function is supported by only the HN58V66A series.

Read Cycle 2 (V_{CC} = 4.5 to 5.5 V)

		HN58V65A/HN58V66A			
		-10			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	70	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	30	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1, 2]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay*[2]	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. This function is supported by only the HN58V66A series.

Read Timing Waveform



Note: 1. This function is supported by only the HN58V66A series.

Write Cycle 1 (V_{CC} = 2.7 to 4.5 V)

Parameter	Symbol	Min*[1]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[3]	—	—	ns	
Reset protect time*[4]	t_{RP}	100	—	—	µs	
Reset high time*[4, 5]	t_{RES}	1	—	—	µs	

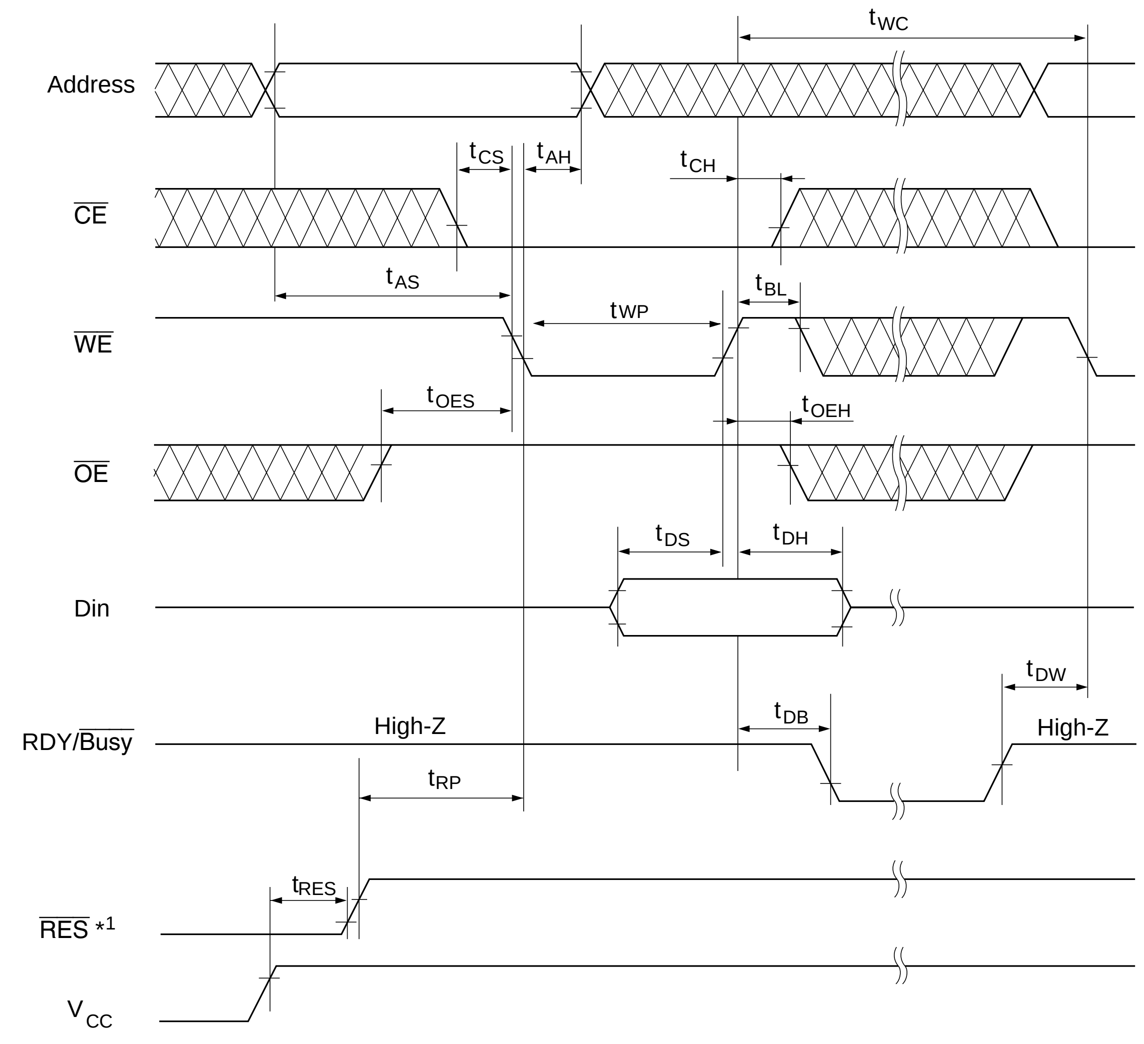
Notes:
1. Use this device in longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
4. This function is supported by only the HN58V66A series.
5. This parameter is sampled and not 100% tested.

Write Cycle 2 (V_{CC} = 4.5 to 5.5 V)

Parameter	Symbol	Min*[1]	Typ	Max	Unit	Test conditions
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	100	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[3]	—	—	ns	
Reset protect time*[4]	t_{RP}	100	—	—	µs	
Reset high time*[4, 5]	t_{RES}	1	—	—	µs	

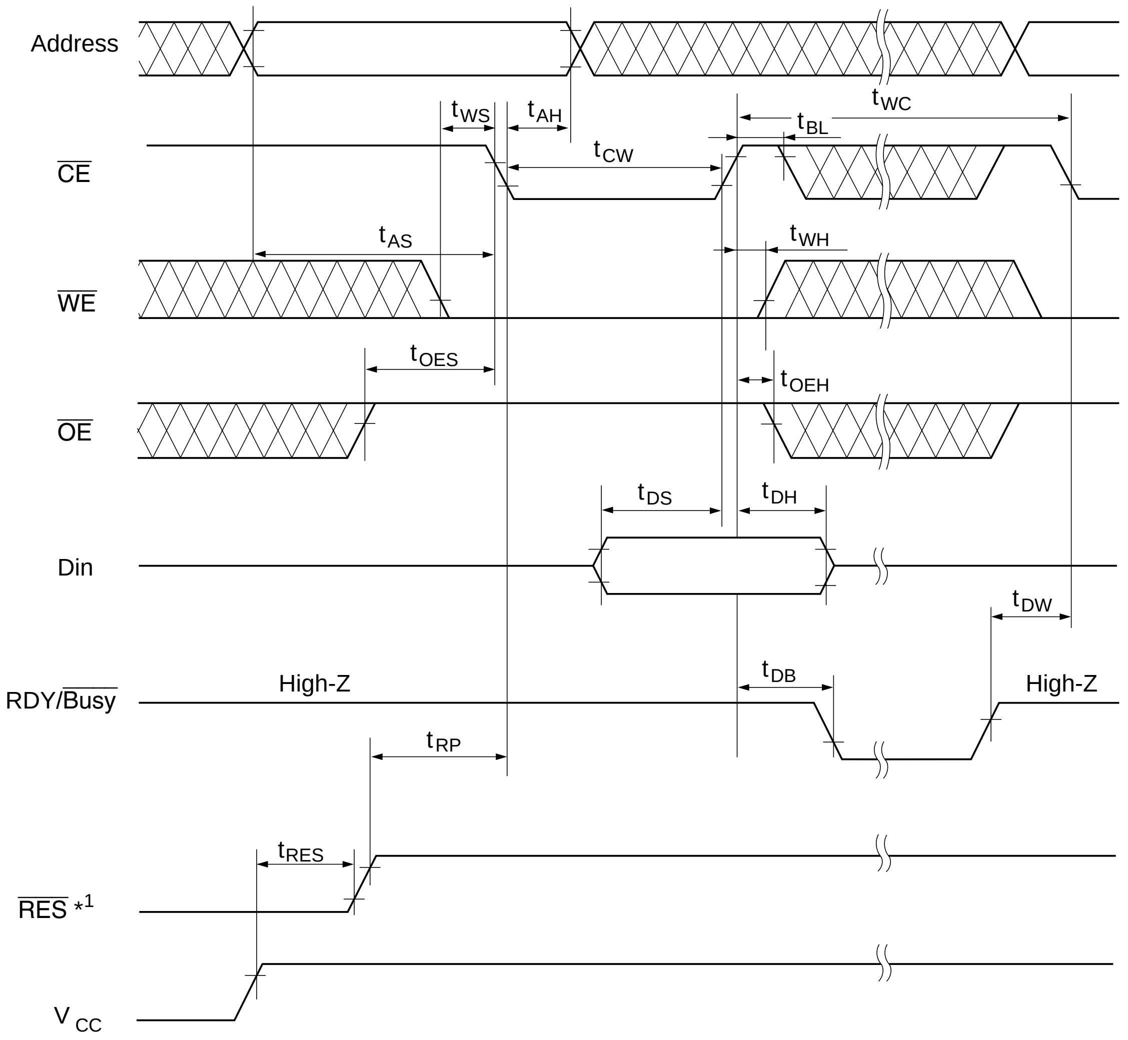
Notes:
1. Use this device in longer cycle than this value.
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
4. This function is supported by only the HN58V66A series.
5. This parameter is sampled and not 100% tested.

Byte Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



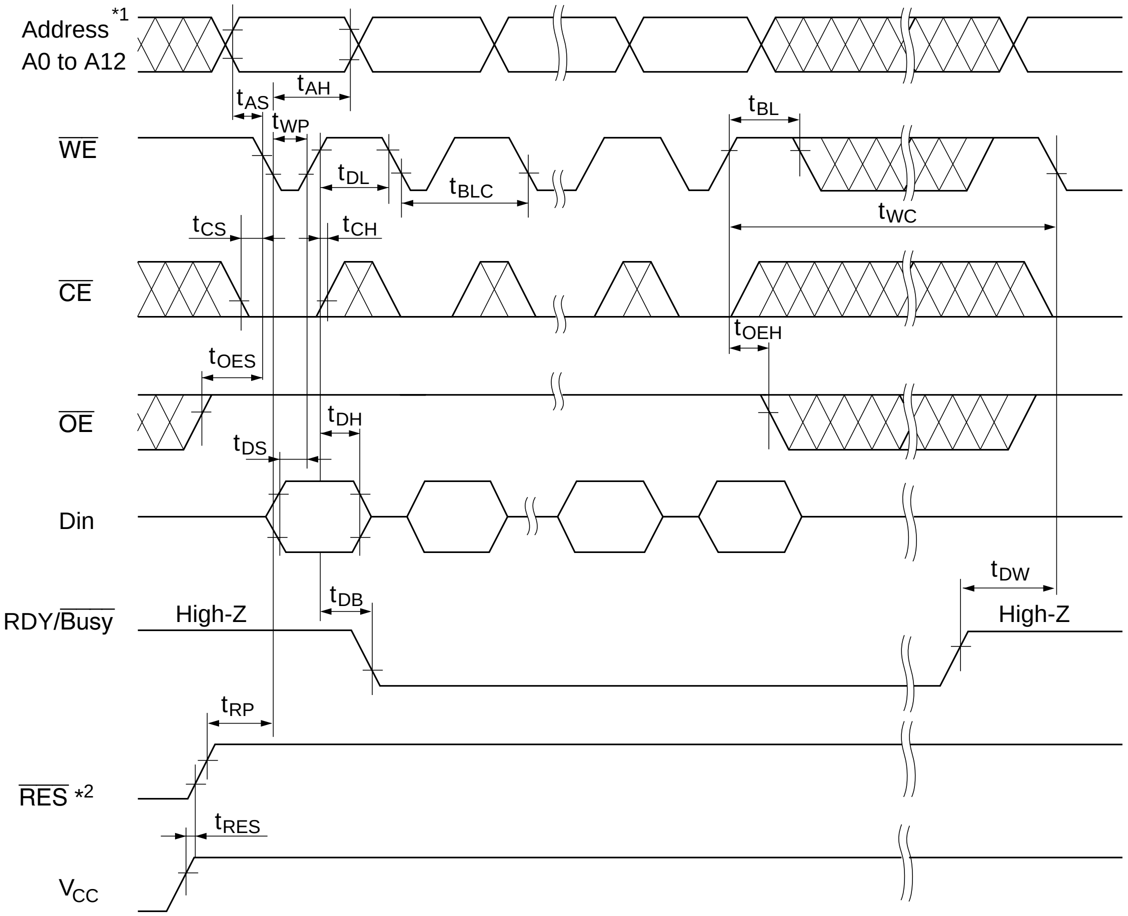
Note: 1. This function is supported by only the HN58V66A series.

Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



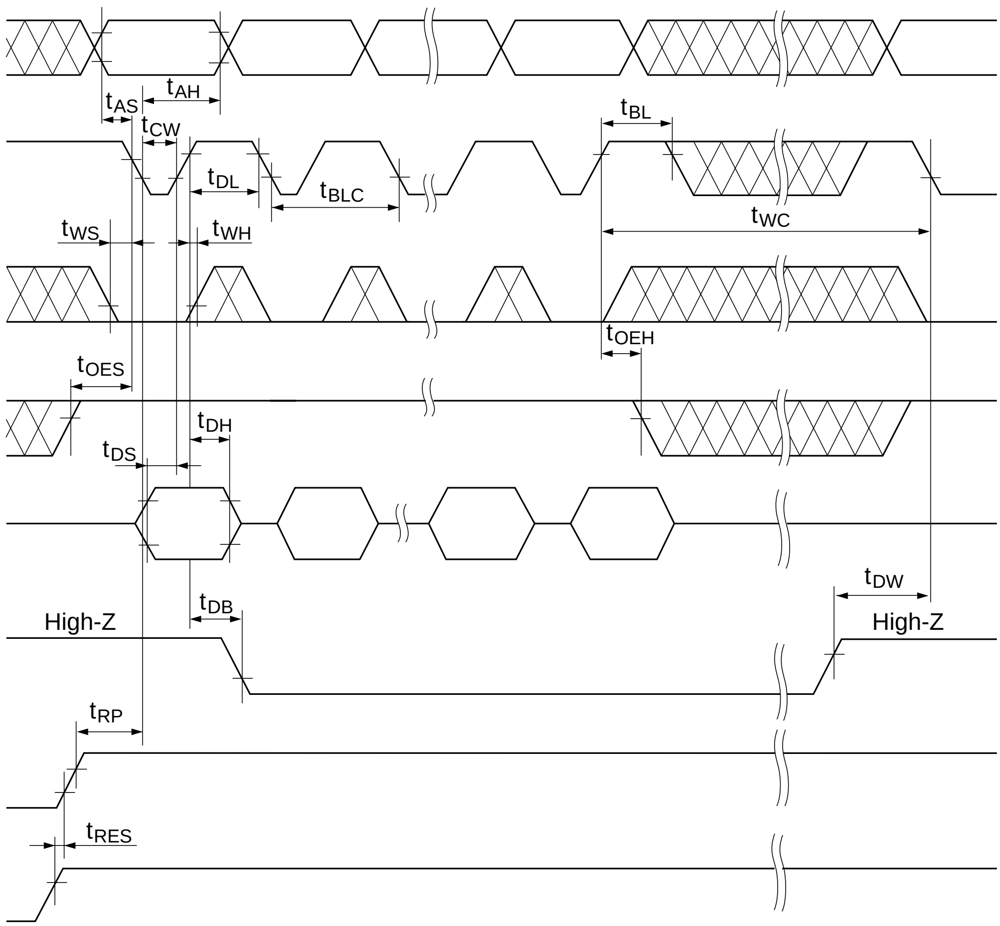
Note: 1. This function is supported by only the HN58V66A series.

Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



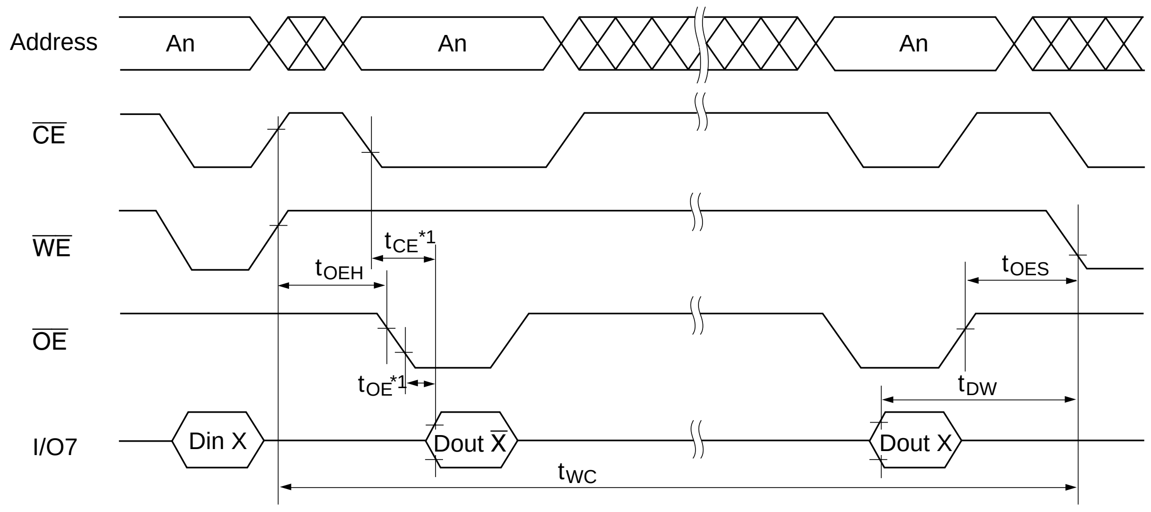
Notes: 1. A5 through A12 are page address and these address are latched at the first falling edge of $\overline{WE}$.
2. This function is supported by only the HN58V66A series.

Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



Notes: 1. A5 through A12 are page address and these address are latched at the first falling edge of $\overline{CE}$.
2. This function is supported by only the HN58V66A series.

$\overline{\text{Data}}$ Polling Timing Waveform

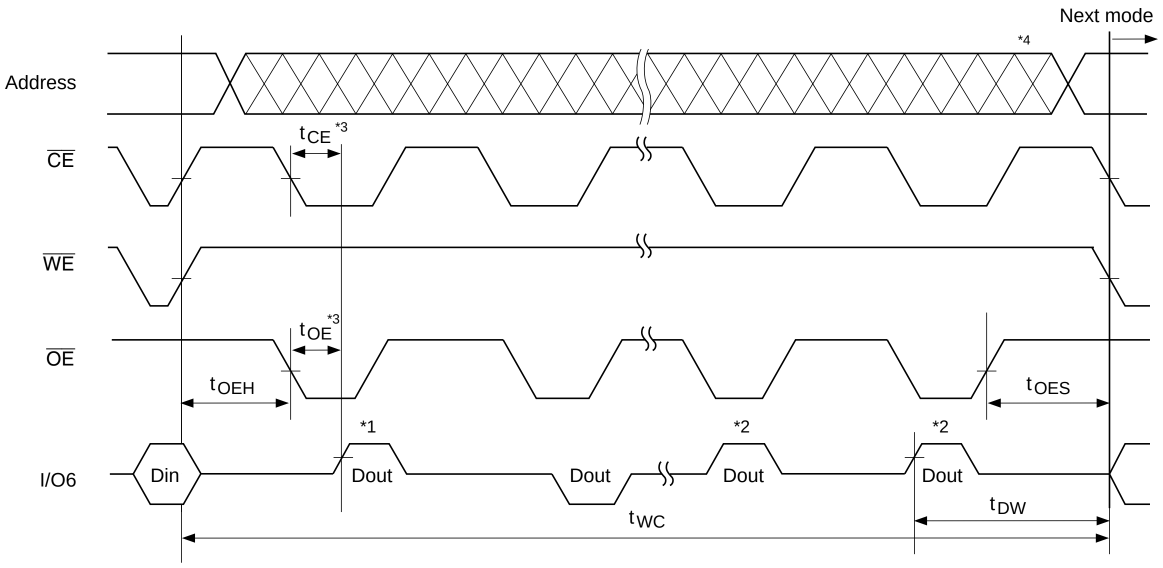


Note: 1. See AC read characteristics.

Toggle Bit

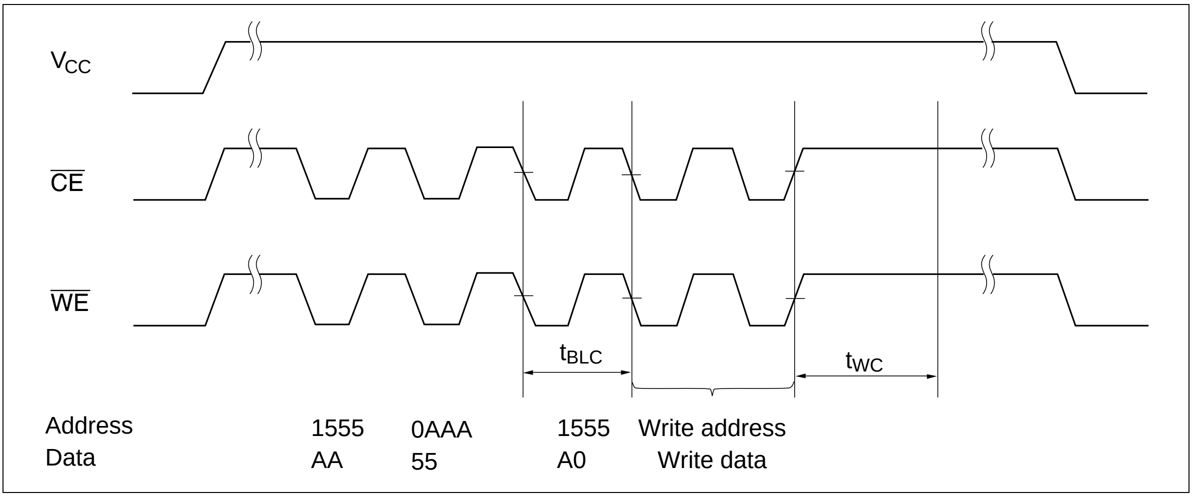
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

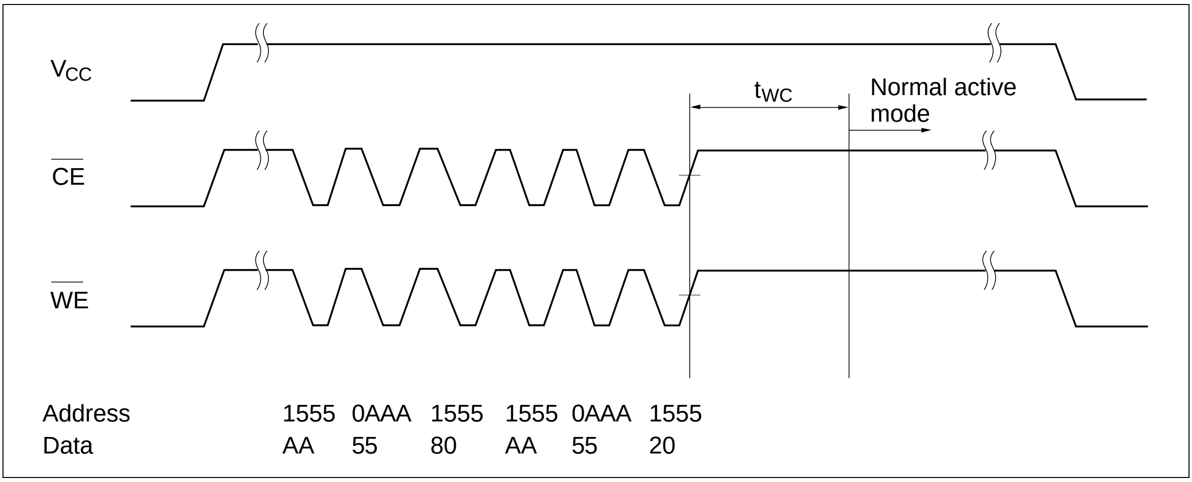


Notes: 1. I/O6 biginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.

Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$. When $\overline{\text{CE}}$ or $\overline{\text{WE}}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

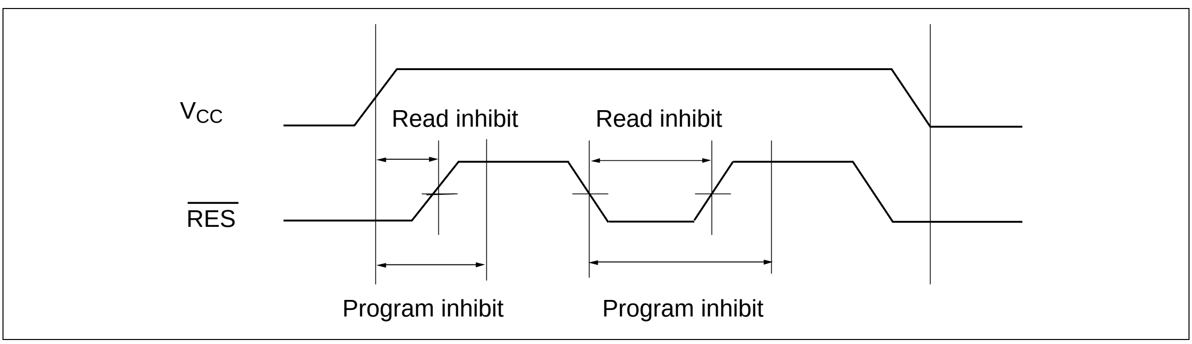
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal (only the HN58V66A series)

When $\overline{\text{RES}}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is switched. $\overline{\text{RES}}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

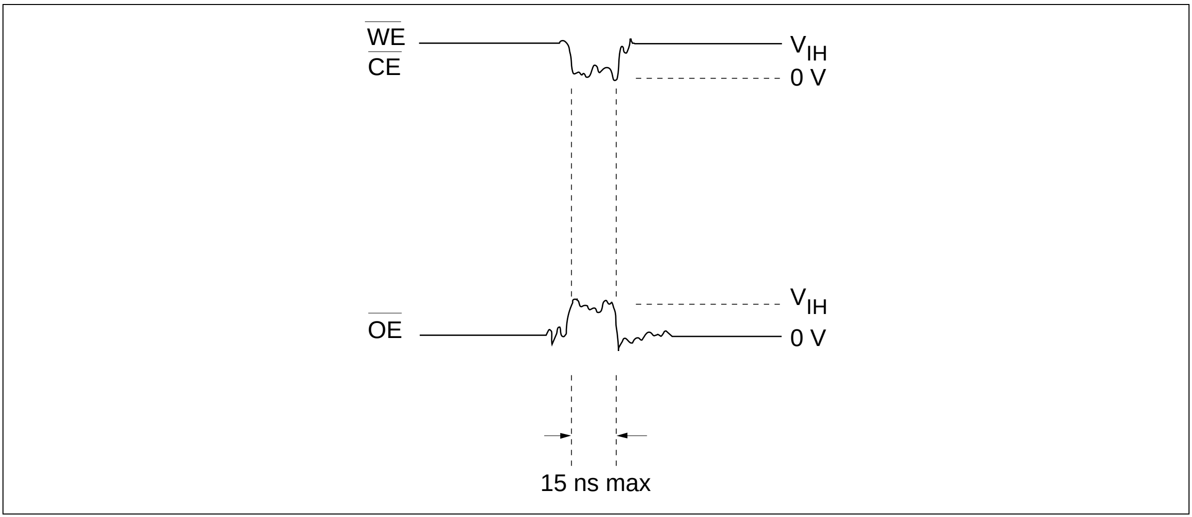
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

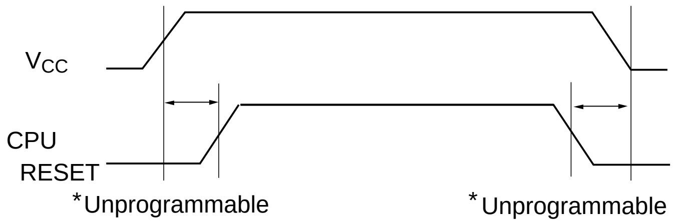
To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 15 ns or less in programming mode.

Be careful not to allow noise of a width of more than 15 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM shoud be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.

(1) Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

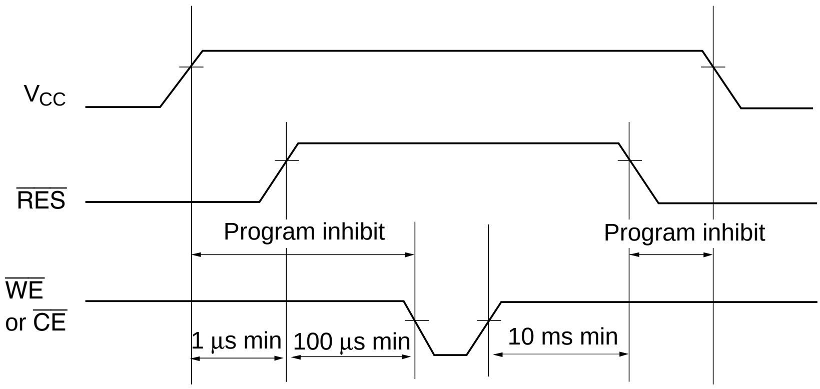
To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don’t care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

(2) Protection by $\overline{RES}$ (only the HN58V66A series)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off. The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, this device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	A0
↓	↓
Write address	Write data } Normal data input

Software data protection mode can be cancelled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the cancelling cycle, the data cannot be written.

Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	80
↓	↓
1555	AA
↓	↓
0AAA	55
↓	↓
1555	20

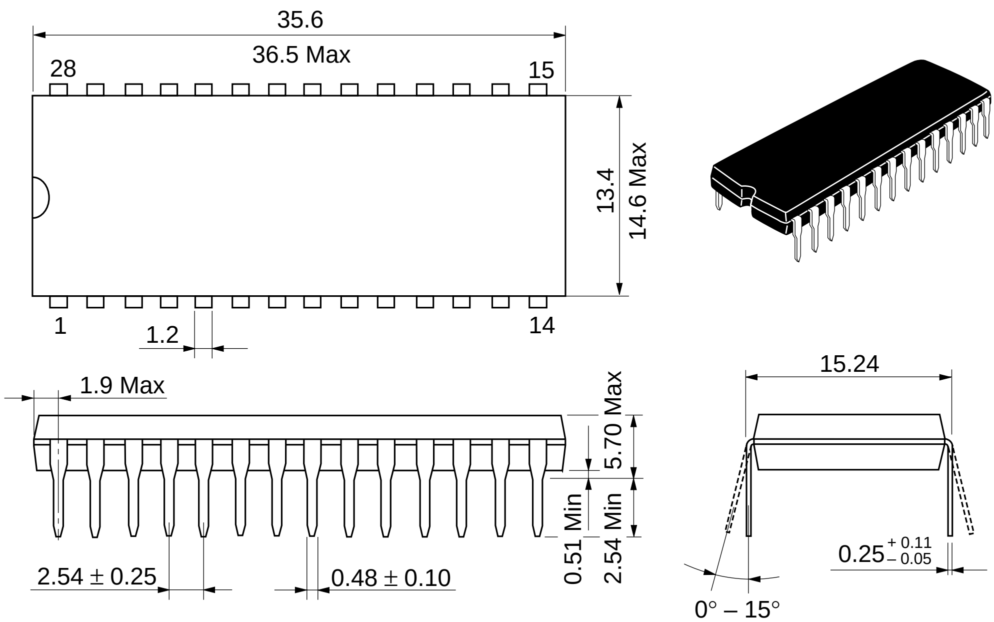
The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi’s and other company’s for enable/disable sequence of software data protection. If there are any questions , please contact with Hitachi sales offices.

Package Dimensions

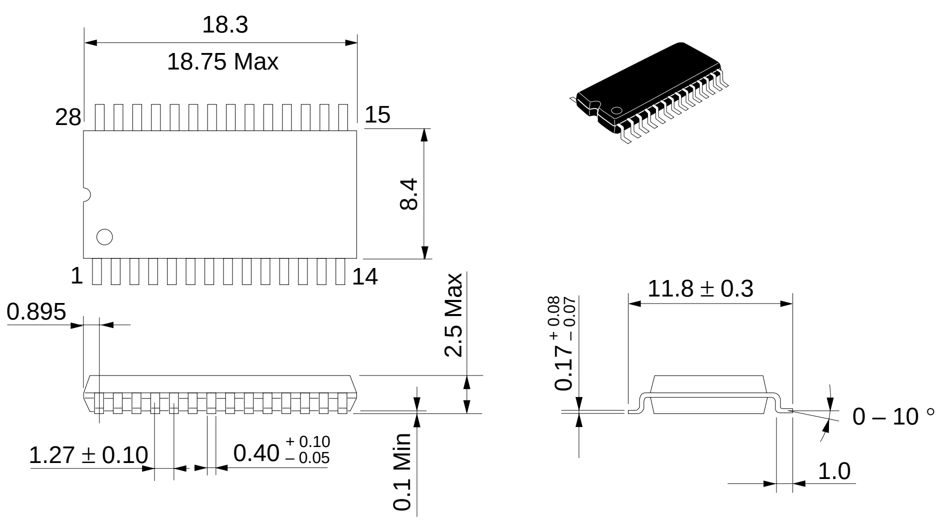
HN58V65AP Series
HN58V66AP Series (DP-28)

Unit : mm



HN58V65AFP Series
HN58V66AFP Series (FP-28D)

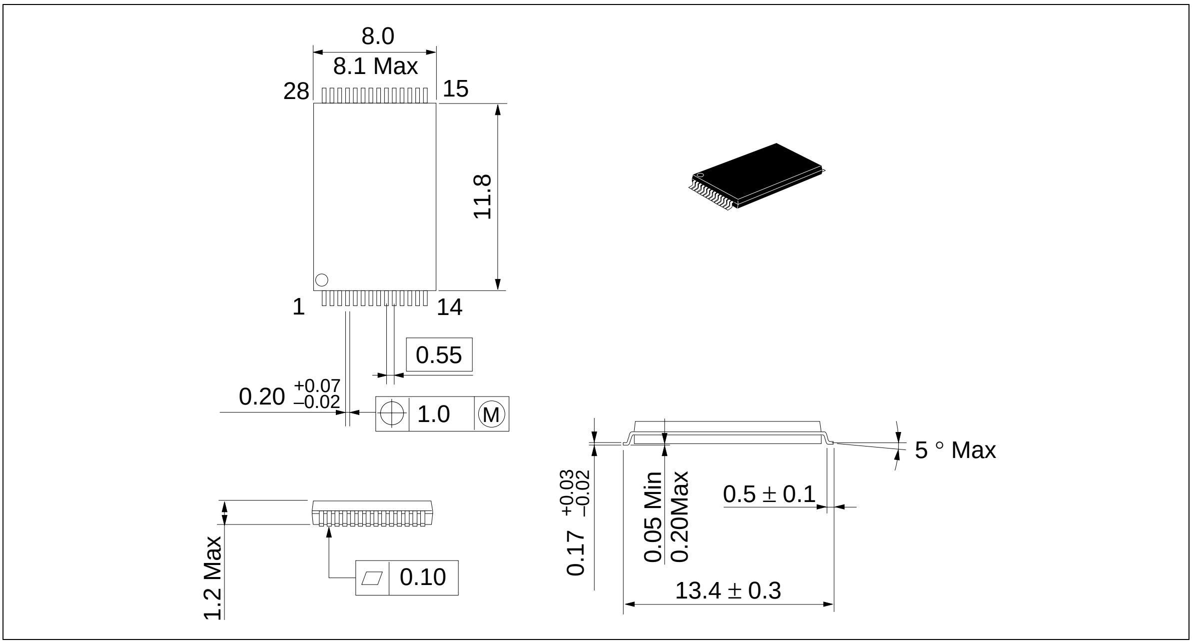
Unit : mm



Package Dimensions (cont)

HN58V65AT Series

HN58V66AT Series (TFP-28DB) Unit : mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Mar. 18, 1996	Initial issue	M. Terasawa	T. Muto
0.1	Nov. 12, 1996	Change of FP-28DA to DP-28 Addition of 5 V specification		