

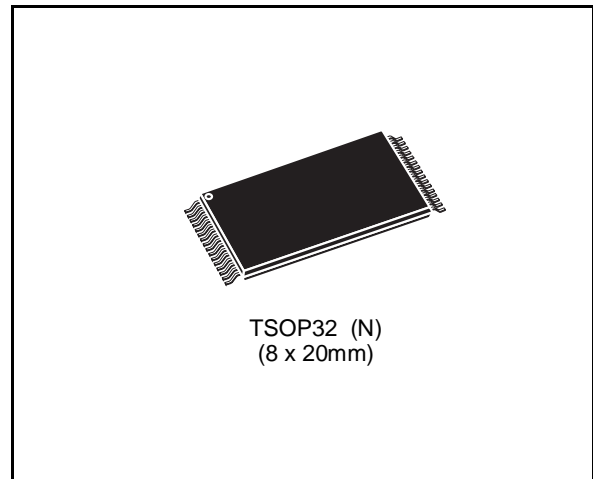


M68Z128

5V, 1 Mbit (128Kb x8) Low Power SRAM with Output Enable

PRELIMINARY DATA

- ULTRA LOW DATA RETENTION CURRENT
 - 10nA (typical)
 - 2.0μA (max)
- OPERATION VOLTAGE: 5V ±10%
- 128Kb x 8 VERY FAST SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 55ns
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER
- AUTOMATIC POWER-DOWN WHEN DESELECTED
- INTENDED FOR USE WITH ST ZEROPOWER AND TIMEKEEPER CONTROLLERS



DESCRIPTION

The M68Z128 is a 1 Mbit (1,048,576 bit) CMOS SRAM, organized as 131,072 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 5V ±10% supply, and all inputs and outputs are TTL compatible.

Table 1. Signal Names

A0-A16	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}1$	Chip Enable 1
E2	Chip Enable 2
\overline{G}	Output Enable
\overline{W}	Write Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

Figure 1. Logic Diagram

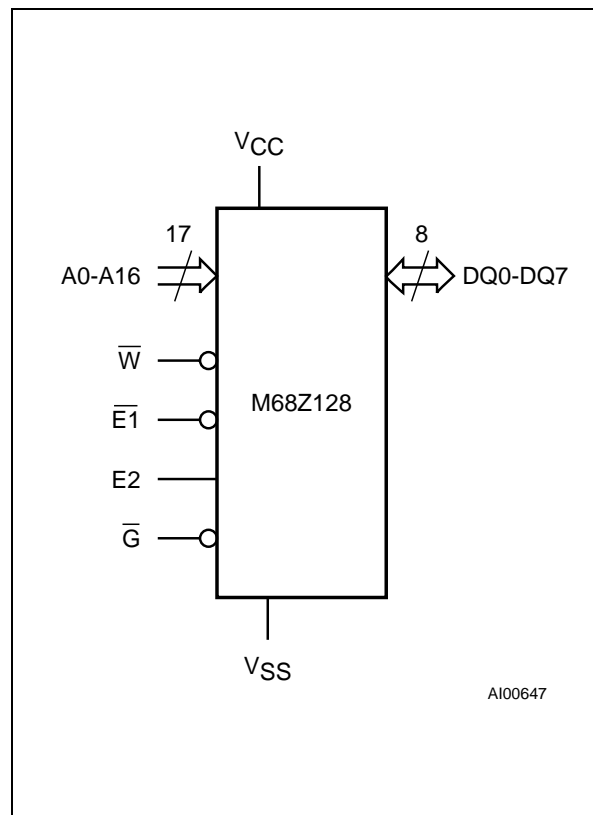


Table 2. Absolute Maximum Ratings ⁽¹⁾

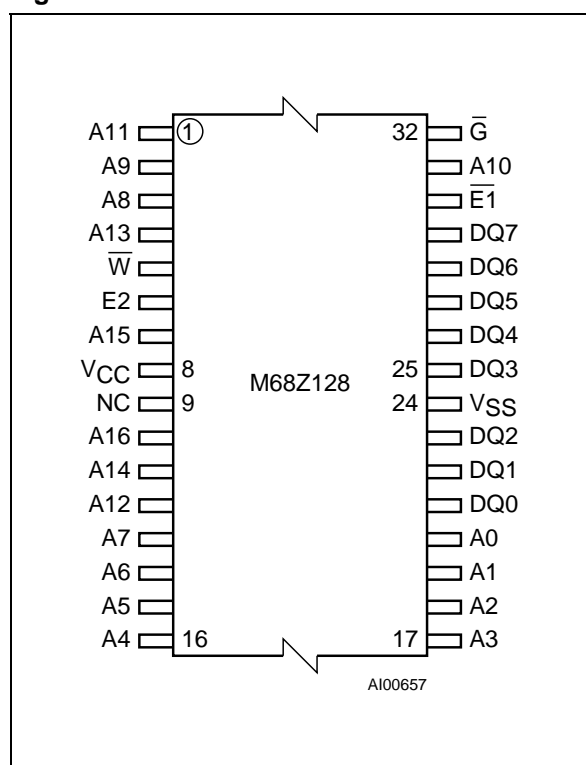
Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	0 to 70	°C
T _{STG}	Storage Temperature	–65 to 150	°C
V _{IO} ⁽²⁾	Input or Output Voltages	–0.3 to V _{CC} + 0.3	V
V _{CC}	Supply Voltage	–0.3 to 7.0	V
I _O ⁽³⁾	Output Current	20	mA
P _D	Power Dissipation	1	W

Notes: 1. Except for the rating "Operating Temperature Range" stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Up to a maximum operating V_{CC} of 5.5V only.

3. One output at a time, not to exceed 1 second duration.

Figure 2. TSOP Pin Connections

**DESCRIPTION** (cont'd)

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68Z128 is available in TSOP32 (8 x 20mm) package.

READ MODE

The M68Z128 is in the Read mode whenever Write Enable (\overline{W}) is High with Output Enable (\overline{G}) Low, and both Chip Enables ($\overline{E1}$ and $E2$) are asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing \overline{G} is Low, $\overline{E1}$ is Low and $E2$ is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV} , t_{E2HQV} , or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX} , t_{E2HQX} and t_{GLQX} , but data lines will always be valid at t_{AVQV} .

WRITE MODE

The M68Z128 is in the Write mode whenever the \overline{W} and $\overline{E1}$ pins are Low, with $E2$ High. Either the Chip Enable inputs ($\overline{E1}$ and $E2$) or the Write Enable input (\overline{W}) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with \overline{W} low. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL} , t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, \overline{W} , or the falling edge of $E2$.

If the Output is enabled ($\overline{E1}$ = Low, $E2$ = High and \overline{G} = Low), then \overline{W} will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the

Table 3. Operating Modes

Mode	$\overline{E1}$	E2	\overline{W}	\overline{G}	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}

Table 4. AC Measurement Conditions

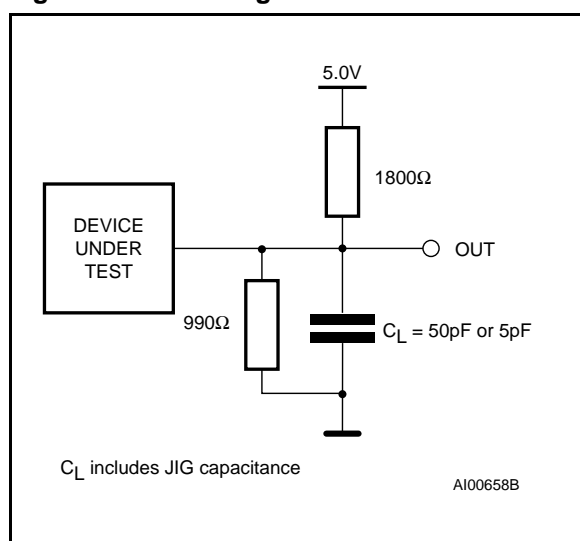
Input Rise and Fall Times	$\leq 5\text{ns}$
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

falling edge of E2, whichever occurs first, and remain valid for t_{WHDX} , t_{E1HDX} or t_{E2LDX} .

OPERATIONAL MODE

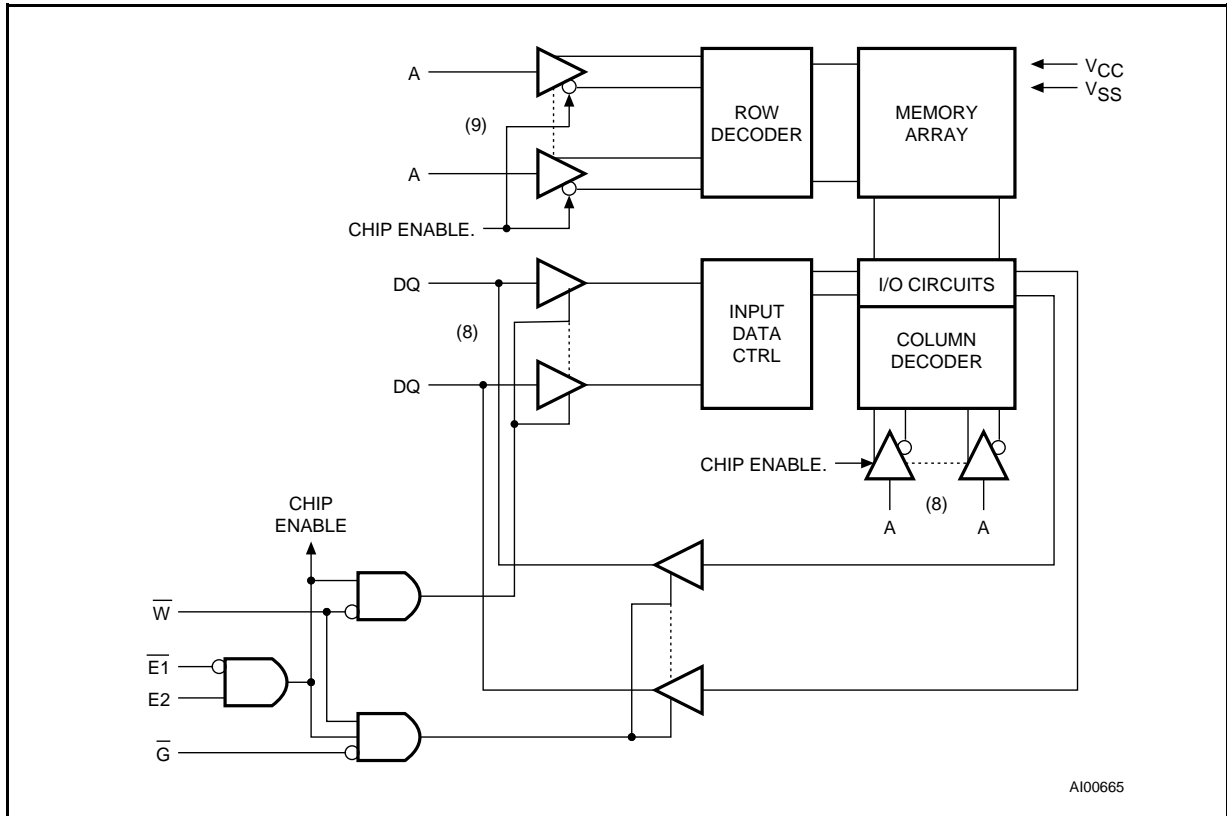
The M68Z128 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ = High or E2 = Low). An Output Enable (\overline{G}) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs \overline{W} , $\overline{E1}$, and E2 as summarized in the Operating Modes table.

Figure 4. AC Testing Load Circuit**Table 5. Capacitance ⁽¹⁾** ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	$V_{IN} = 0\text{V}$		9	pF
$C_{OUT}^{(2)}$	Output Capacitance	$V_{OUT} = 0\text{V}$		9	pF

Notes: 1. Sampled only, not 100% tested
2. Outputs deselected

Figure 3. Block Diagram

Table 6. DC Characteristics ($T_A = 0$ to 70°C ; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$			± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$			± 1	μA
$I_{CC1}^{(1)}$	Supply Current	$V_{CC} = 5.5V, (-55)$		30	70	mA
$I_{CC2}^{(2)}$	Supply Current (Standby) TTL	$V_{CC} = 5.5V, \overline{E1} = V_{IH}$ or $E2 = V_{IL}, f = 0$		0.1	2	mA
$I_{CC3}^{(3)}$	Supply Current (Standby) CMOS	$V_{CC} = 5.5V, \overline{E1} \geq V_{CC} - 0.3V$ or $E2 \leq 0.3V, f = 0$		0.4	20	μA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2		$V_{CC} + 0.3$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4			V

Notes: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum
 2. All other Inputs at $V_{IL} \leq 0.8V$ or $V_{IH} \geq 2.2V$
 3. All other Inputs at $V_{IL} \leq 0.3V$ or $V_{IH} \geq V_{CC} - 0.3V$

Table 7. Read and Standby Modes AC Characteristics(T_A = 0 to 70°C; V_{CC} = 5V ±10%)

Symbol	Parameter	M68Z128		Unit
		-55		
		Min	Max	
t _{AVAV}	Read Cycle Time	55		ns
t _{AVQV} ⁽¹⁾	Address Valid to Output Valid		55	ns
t _{E1LQV} ⁽¹⁾	Chip Enable 1 Low to Output Valid		55	ns
t _{E2HQV} ⁽¹⁾	Chip Enable 2 High to Output Valid		55	ns
t _{GLQV} ⁽¹⁾	Output Enable Low to Output Valid		20	ns
t _{E1LQX} ⁽³⁾	Chip Enable 1 Low to Output Transition	5		ns
t _{E2HQX} ⁽³⁾	Chip Enable 2 High to Output Transition	5		ns
t _{GLQX} ⁽³⁾	Output Enable Low to Output Transition	0		ns
t _{E1HQZ} ^(2,3)	Chip Enable 1 High to Output Hi-Z		20	ns
t _{E2LQZ} ^(2,3)	Chip Enable 2 Low to Output Hi-Z		20	ns
t _{GHQZ} ^(2,3)	Output Enable High to Output Hi-Z		20	ns
t _{AXQX} ⁽¹⁾	Address Transition to Output Transition	5		ns
t _{PU}	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns
t _{PD}	Chip Enable 1 High or Chip Enable 2 Low to Power Down		55	ns

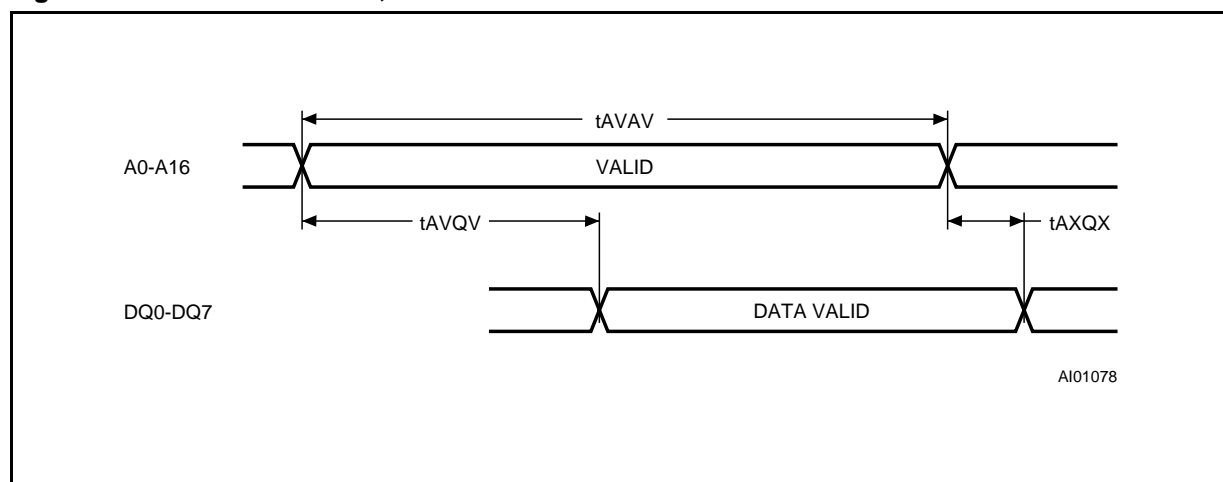
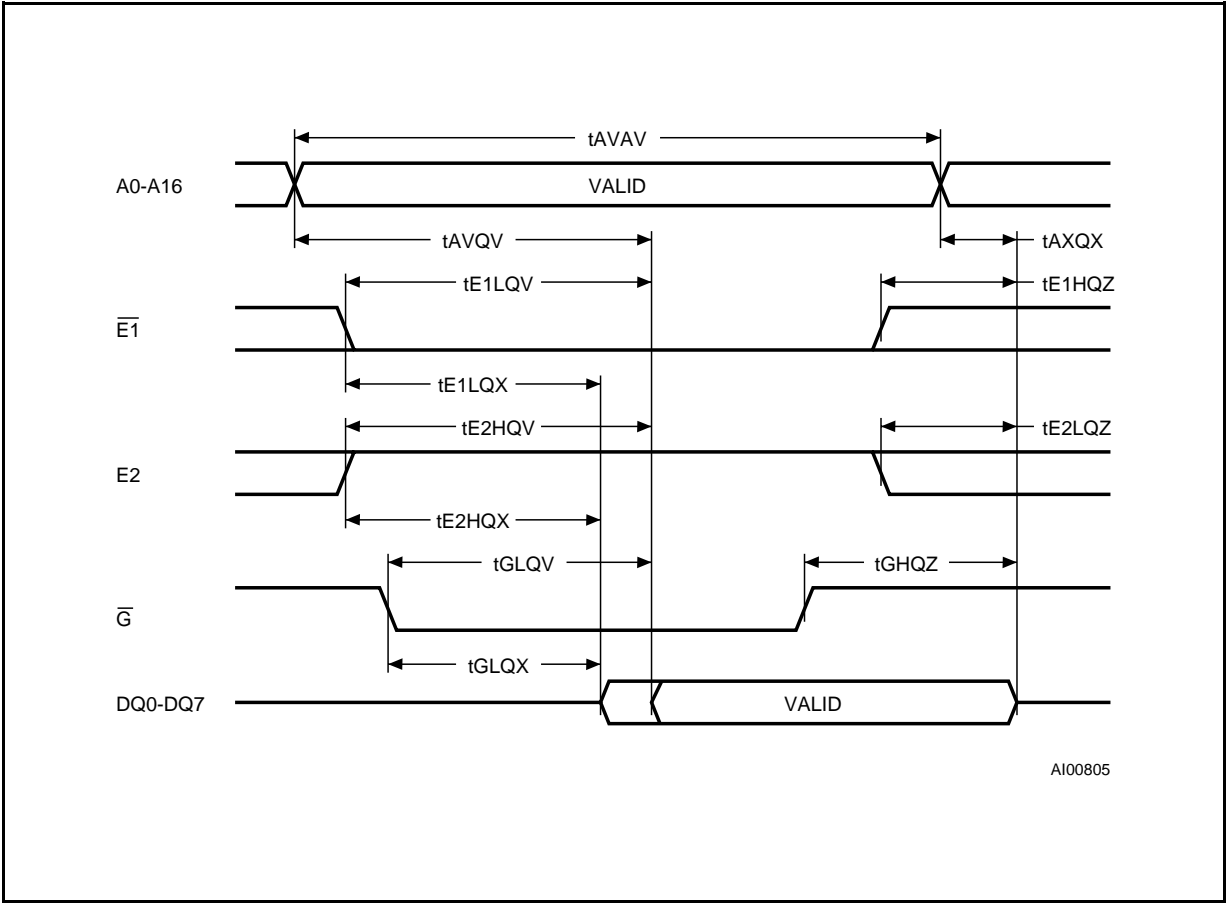
Notes: 1. C_L = 100pF (see Figure 4)2. C_L = 5pF (see Figure 4)3. At any given temperature and voltage condition, t_{E1HQZ} + t_{E2HQZ} is less than t_{E1LQX} and t_{E2LQX}, t_{GHQZ} is less than t_{GLQX} for any given device.**Figure 5. Address Controlled, Read Mode AC Waveforms****Note:** $\overline{E1}$ = Low, E2 = High, \overline{G} = Low, \overline{W} = High

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable (\overline{W}) = High

Figure 7. Standby Mode AC Waveforms

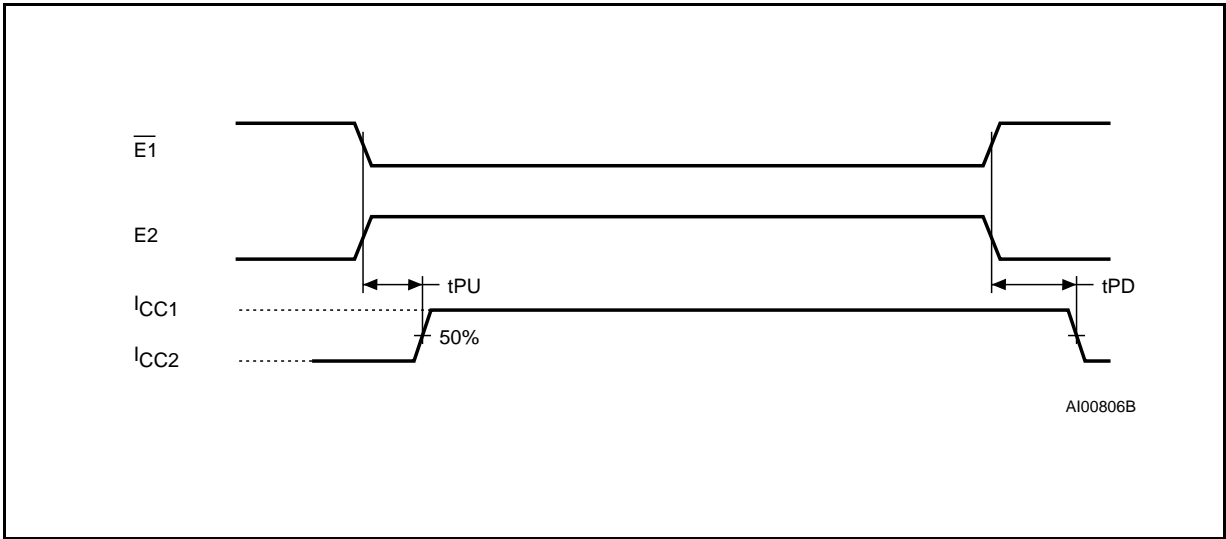


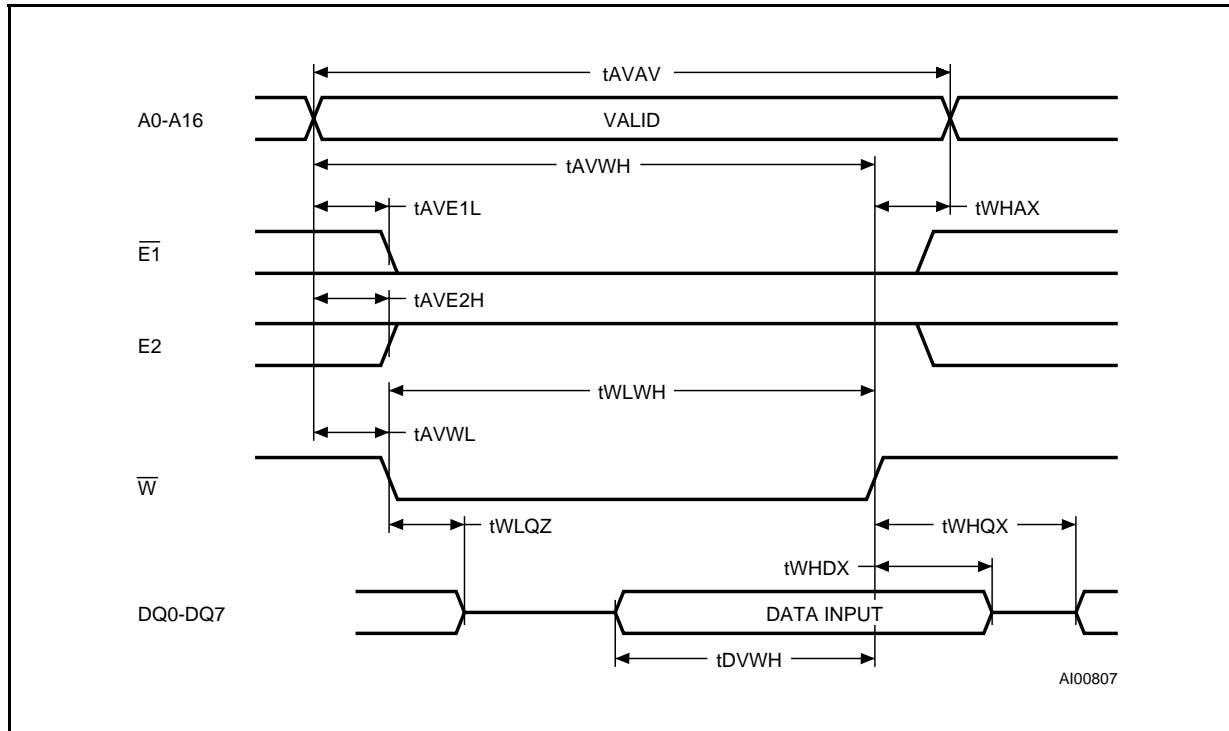
Table 8. Write Mode AC Characteristics ($T_A = 0$ to 70°C ; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	M68Z128		Unit
		-55		
		Min	Max	
t _{AVAV}	Write Cycle Time	55		ns
t _{AVWL}	Address Valid to Write Enable Low	0		ns
t _{AVWH}	Address Valid to Write Enable High	45		ns
t _{AVE1H}	Address Valid to Chip Enable 1 High	45		ns
t _{AVE2L}	Address Valid to Chip Enable 2 Low	45		ns
t _{WLWH}	Write Enable Pulse Width	45		ns
t _{WHAX}	Write Enable High to Address Transition	0		ns
t _{WHDX}	Write Enable High to Input Transition	0		ns
t _{WHQX} ⁽²⁾	Write Enable High to Output Transition	5		ns
t _{WLQZ} ^(1,2)	Write Enable Low to Output Hi-Z		20	ns
t _{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t _{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t _{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	45		ns
t _{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	45		ns
t _{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t _{E2LAX}	Chip Enable 2 Low to Address Transition	0		ns
t _{DVWH}	Input Valid to Write Enable High	25		ns
t _{DVE1H}	Input Valid to Chip Enable 1 High	25		ns
t _{DVE2L}	Input Valid to Chip Enable 2 Low	25		ns

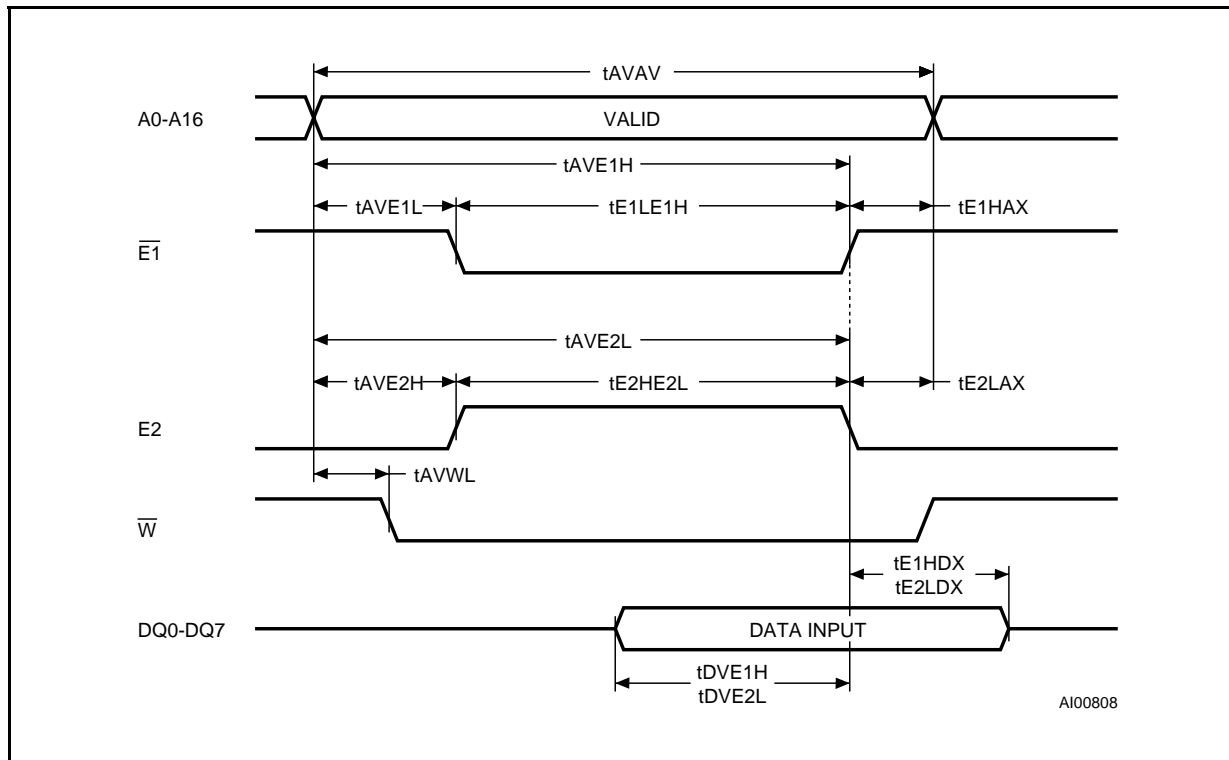
Note: 1. $C_L = 5\text{pF}$ (see Figure 4)

2. At any given temperature and voltage condition, t_{WHQX} is less than t_{WLQZ} for any given device.

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: Output Enable (\overline{G}) = Low

Figure 9. Chip Enable Controlled, Write AC Waveforms ^(1,2)

Notes: 1. Output Enable (\overline{G}) = High

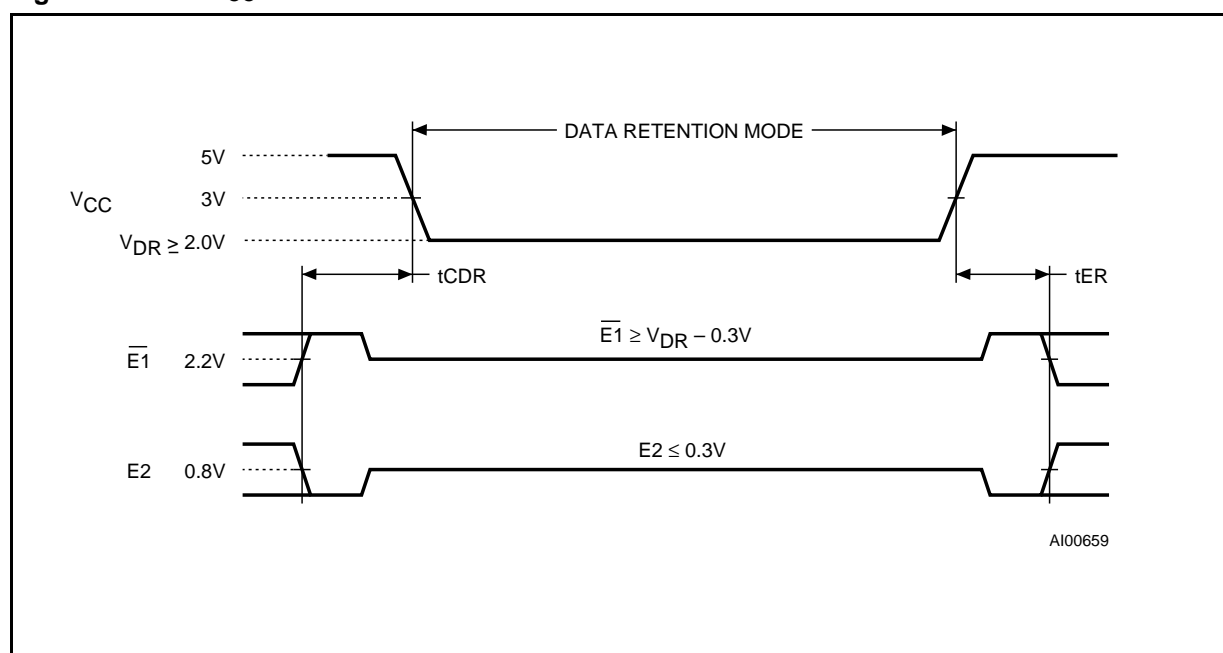
2. If $\overline{E1}$ goes High or $\overline{E2}$ goes Low simultaneously with \overline{W} high, the output remains in a high-impedance state.

Table 9. Low V_{CC} Data Retention Characteristics
($T_A = 0$ to 70°C)

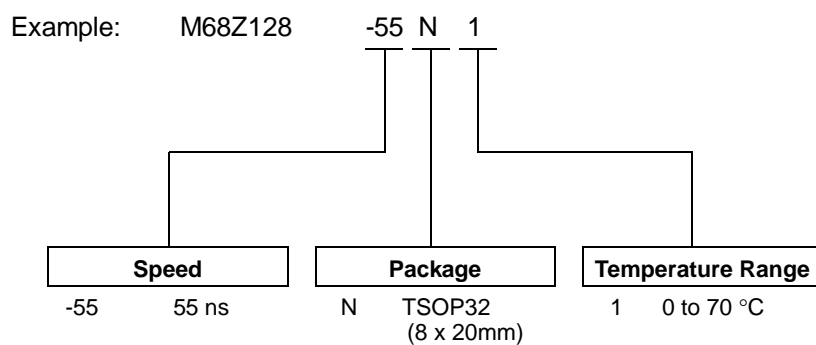
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CCDR}	Supply Current (Data Retention)	$V_{CC} = 3\text{V}$, $\overline{E1} \geq V_{CC} - 0.3\text{V}$ or $E2 \leq 0.3\text{V}$, $f = 0$		0.01	2	μA
V_{DR}	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.3\text{V}$ or $E2 \leq 0.3\text{V}$, $f = 0$	2			V
t_{CDR}	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.3\text{V}$ or $E2 \leq 0.3\text{V}$, $f = 0$	0			ns
$t_{ER}^{(1)}$	Operation Recovery Time		t_{AVAV}			ns

Note: 1. See Figure 10 for measurement points. Guaranteed but not tested. t_{AVAV} is Read cycle time.

Figure 10. Low V_{CC} Data Retention AC Waveforms



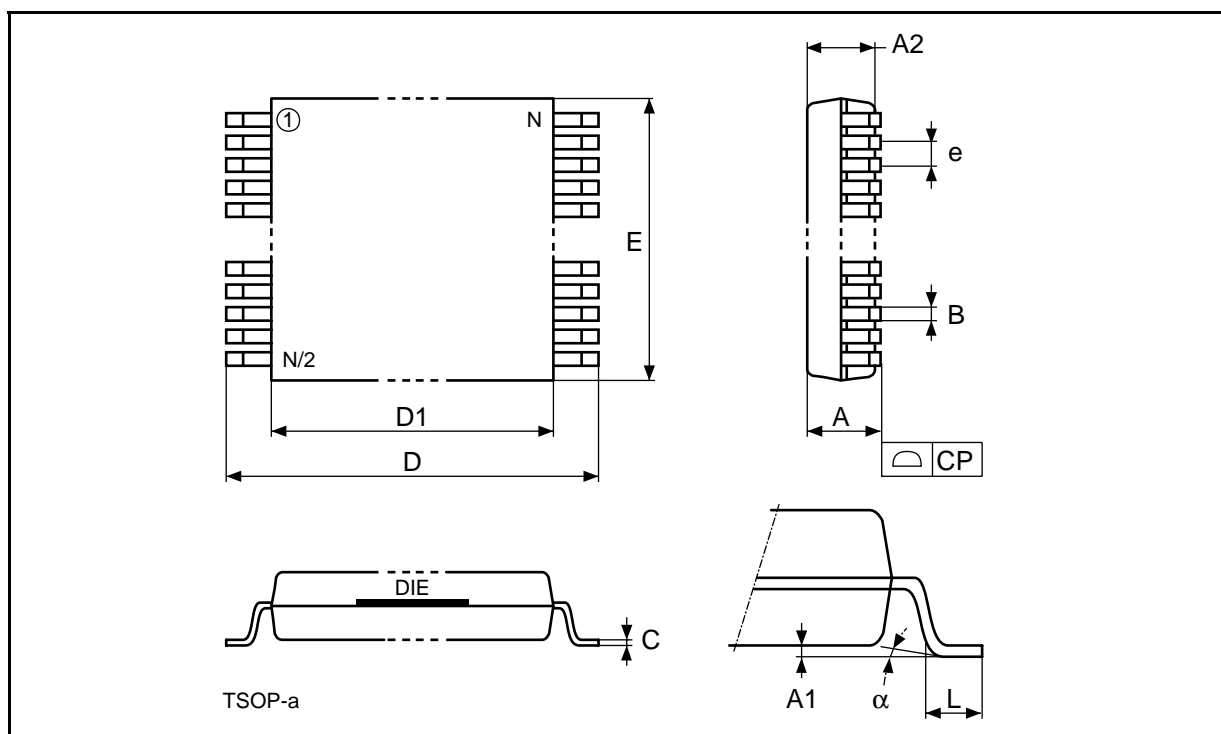
ORDERING INFORMATION SCHEME



For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP32 - 32 lead Plastic Thin Small Outline (8 x 20mm)

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.007
A2		0.95	1.05		0.037	0.041
B		0.17	0.23		0.006	0.010
C		0.10	0.20		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.80	8.20		0.307	0.323
e	0.50	-	-	0.020	-	-
L		0.40	0.60		0.016	0.024
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004



Drawing is not to scale

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