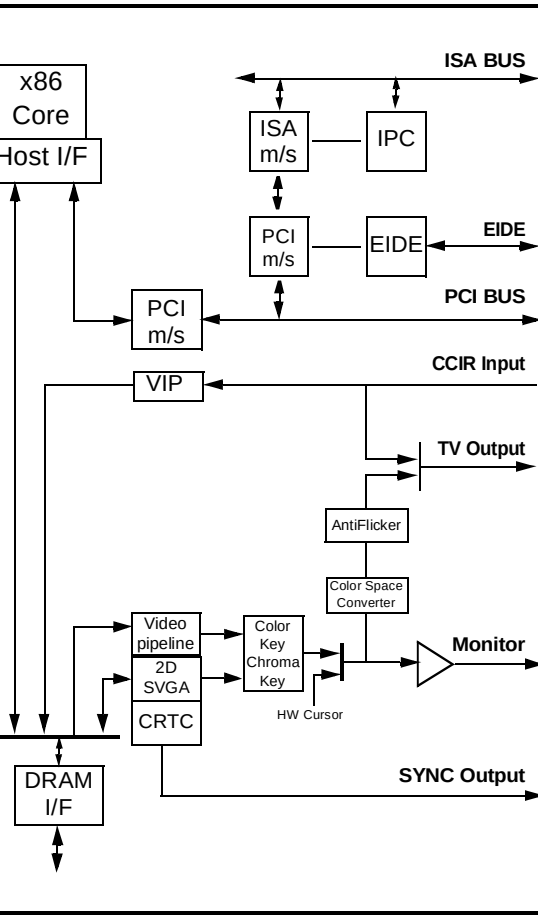
# STPC CLIENT

## Multimedia PC on a Chip

- POWERFUL X86 PROCESSOR
- 64-BIT 66MHz BUS INTERFACE
- 64-BIT DRAM CONTROLLER
- SVGA GRAPHICS CONTROLLER
- UMA ARCHITECTURE
- VIDEO SCALER
- VIDEO OUTPUT PORT
- VIDEO INPUT PORT
- CRT CONTROLLER
- 135MHz RAMDAC
- UP TO 3-LINE FLICKER FILTER
- SCAN CONVERTER
- PCI MASTER / SLAVE / ARBITER
- ISA MASTER/SLAVE
- IDE CONTROLLER
- DMA CONTROLLER
- INTERRUPT CONTROLLER
- TIMER / COUNTERS
- POWER MANAGEMENT


PBGA388

**Logic Diagram**




**DESCRIPTION**

The STPC Client integrates a standard 5th generation x86 core, a DRAM controller, a graphics subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single Consumer orientated PC compatible subsystem on a single device.

The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing the same memory array between the CPU main memory and the graphics and video frame buffers.

Extra facilities are implemented to handle video streams. Features include smooth scaling and colour space conversion of the video input stream and mixing of the video stream with non-video data from the frame buffer. The chip also includes anti-flicker filters to provide a stable, high-quality Digital TV output.

The STPC Client is packaged in a 388 Plastic Ball Grid Array (PBGA).