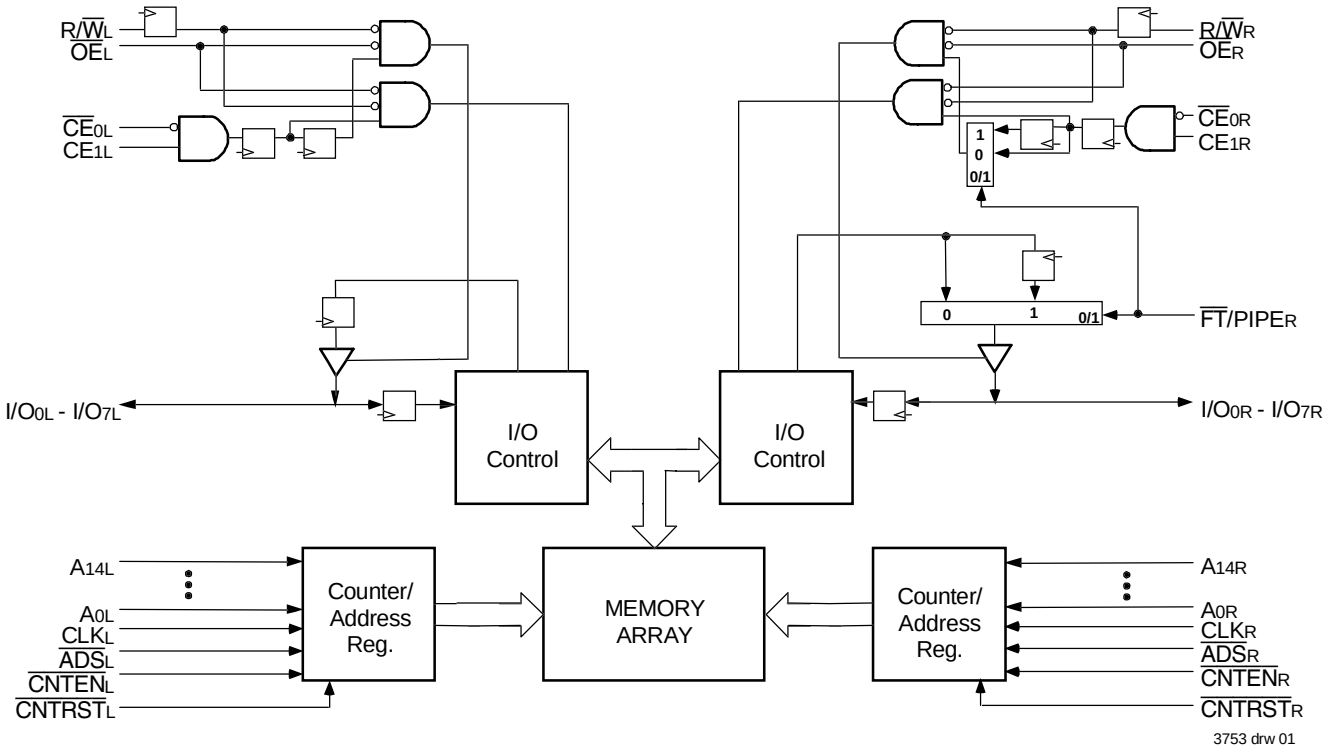
# HIGH-SPEED 3.3V 32K x 8 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

***PRELIMINARY***
***IDT70V9079S/L***

## Features:

- **True Dual-Ported memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 9/12/15ns (max.)*
- **Low-power operation**
  - *IDT70V9079S*
    *Active: 429mW (typ.)*
    *Standby: 3.3mW (typ.)*
  - *IDT70V9079L*
    *Active: 429mW (typ.)*
    *Standby: 1.32mW (typ.)*
- **Flow-Through or Pipelined output mode on Right Port via the $\overline{FT}$/PIPE$_R$ pin**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 9ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *15ns cycle time, 66MHz operation in the Pipelined output mode*
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **LVTTL- compatible, single 3.3V (±0.3V) power supply**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Available in a 100 pin Thin Quad Flatpack (TQFP)**

## Functional Block Diagram




3753 drw 01

**JUNE 1999**





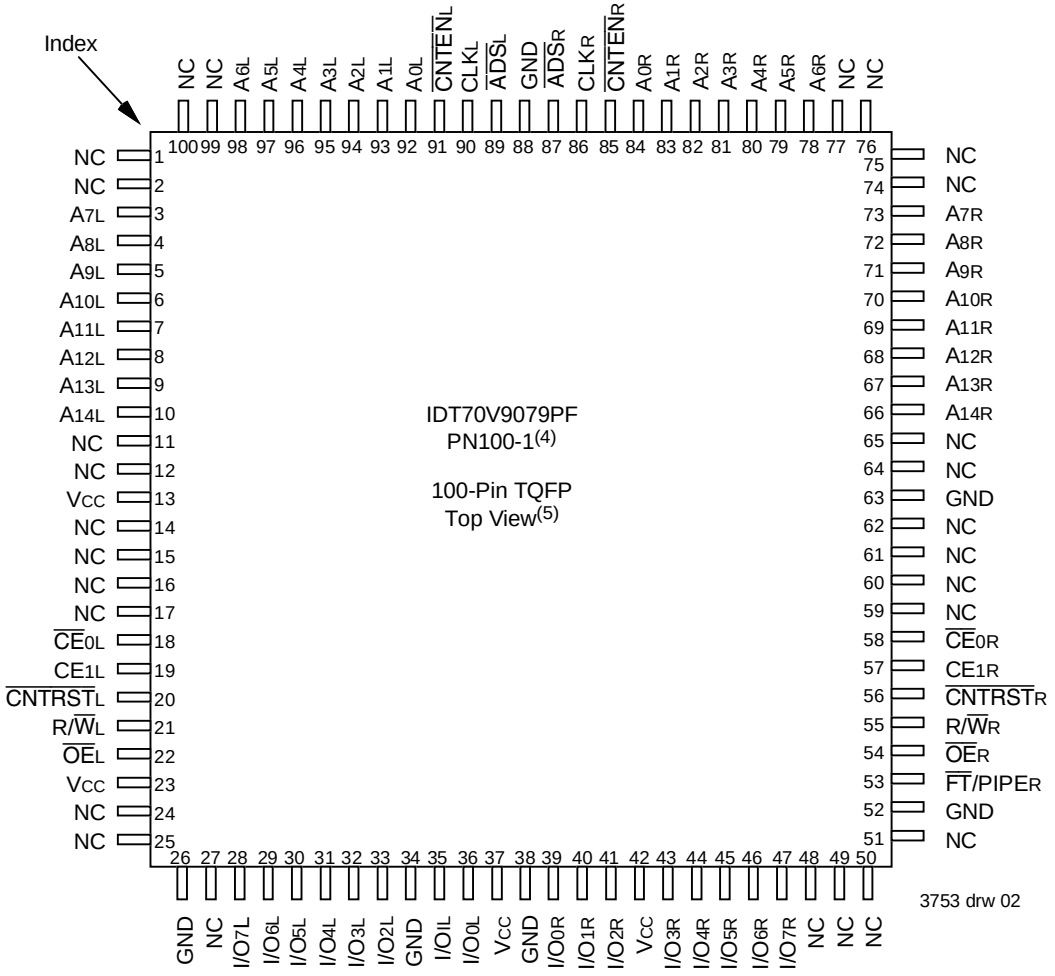
DSC 3753/4

## Description:

The IDT70V9079 is a high-speed 32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9079 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $CE_0$ and $CE_1$, permits the on-chip circuitry of each port to enter a very LOW standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 429mW of power.

## Pin Configurations[1,2,3]




**NOTES:**
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

## Pin Names

| Left Port | Right Port | Names |
|---|---|---|
| $\overline{CE}_{0L}$, $CE_{1L}$ | $\overline{CE}_{0R}$, $CE_{1R}$ | Chip Enables |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L}$ - $A_{14L}$ | $A_{0R}$ - $A_{14R}$ | Address |
| $I/O_{0L}$ - $I/O_{7L}$ | $I/O_{0R}$ - $I/O_{7R}$ | Data Input/Output |
| $CLK_L$ | $CLK_R$ | Clock |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable |
| $\overline{CNTRST}_L$ | $\overline{CNTRST}_R$ | Counter Reset |
| — | $\overline{FT}/PIPE_R$ | Flow-Through/Pipeline |
| $V_{CC}$ | | Power |
| GND | | Ground |

3753 tbl 01

## Truth Table I—Read/Write and Enable Control(1,2,3)

| $\overline{OE}$ | CLK | $\overline{CE}_0$ | $CE_1$ | R/$\overline{W}$ | $I/O_{0-7}$ | Mode |
|---|---|---|---|---|---|---|
| X | ↑ | H | X | X | High-Z | Deselected |
| X | ↑ | X | L | X | High-Z | Deselected |
| X | ↑ | L | H | L | $DATA_{IN}$ | Write |
| L | ↑ | L | H | H | $DATA_{OUT}$ | Read |
| H | X | L | H | X | High-Z | Outputs Disabled |

3753 tbl 02

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

## Truth Table II—Address Counter Control(1,2)

| Address | Previous Address | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{CNTRST}$ | I/O(3) | Mode |
|---|---|---|---|---|---|---|---|
| X | X | ↑ | H | H | L | $DATA_{I/O(0)}$ | Counter Reset to Address 0 |
| An | X | ↑ | L(4) | H | H | $DATA_{I/O(n)}$ | External Address Utilized |
| X | An | ↑ | H | H | H | $DATA_{I/O(n)}$ | External Address Blocked—Counter Disabled |
| X | An | ↑ | H | L(5) | H | $DATA_{I/O(n+1)}$ | Counter Enable—Internal Address Generation |

3753 tbl 03

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{CE}_0$ and $\overline{OE}$ = $V_{IL}$; $CE_1$ and R/$\overline{W}$ = $V_{IH}$.
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ is independent of all other signals including $\overline{CE}_0$ and $CE_1$.
5. The address counter advances if $\overline{CNTEN}$ = $V_{IL}$ on the rising edge of CLK, regardless of all other signals including $\overline{CE}_0$ and $CE_1$.

## Recommended Operating Temperature and Supply Voltage[1,2]

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | 0V | 3.3V ± 0.3V |

3753 tbl 04

**NOTES:**
1. This is the parameter TA.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

## Recommend DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| GND | Ground | 0 | 0 | 0 | V |
| VIH | Input High Voltage | 2.2 | — | VCC + 0.3V[2] | V |
| VIL | Input Low Voltage | -0.3[2] | — | 0.8 | V |

3753 tbl 05

**NOTES:**
1. VTERM must not exceed VCC +0.3V.
2. VIL ≥ -1.5V for pulse width less than 10ns.

## Absolute Maximum Ratings[1]

| Symbol | Rating | Commercial & Industrial | Unit |
|---|---|---|---|
| VTERM[2] | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| TBIAS | Temperature Under Bias | -55 to +125 | °C |
| TSTG | Storage Temperature | -55 to +125 | °C |
| IOUT | DC Output Current | 50 | mA |

3753 tbl 06

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC +0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ VCC + 0.3V.

## Capacitance (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter[1] | Conditions[2] | Max. | Unit |
|---|---|---|---|---|
| CIN | Input Capacitance | VIN = 3dV | 9 | pF |
| COUT[3] | Output Capacitance | VOUT = 3dV | 10 | pF |

3753 tbl 07

**NOTES:**
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. COUT also references CI/O.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{CC}$ = 3.3V ± 0.3V)

| Symbol | Parameter | Test Conditions | 70V9079S | | 70V9079L | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current[1] | $V_{CC}$ = 3.3V, $V_{IN}$ = 0V to $V_{CC}$ | — | 10 | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{CE}_0$ = $V_{IH}$ or $CE_1$ = $V_{IL}$, $V_{OUT}$ = 0V to $V_{CC}$ | — | 10 | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +4mA | — | 0.4 | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA | 2.4 | — | 2.4 | — | V |

3753 tbl 08

**NOTE:**
1. At $V_{CC}$ ≤ 2.0V input leakages are undefined.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6,7] ($V_{CC}$ = 3.3V ± 0.3V)

| Symbol | Parameter | Test Condition | Version | | 70V9079X9 Com'l Only | | 70V9079X12 Com'l Only | | 70V9079X15 Com'l Only | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ.[4] | Max. | Typ.[4] | Max. | Typ.[4] | Max. | |
| $I_{CC}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IL}$ Outputs Open f = $f_{MAX}$[1] | COM'L | S | 180 | 260 | 150 | 240 | 130 | 220 | mA |
| | | | | L | 180 | 225 | 150 | 205 | 130 | 185 | |
| | | | IND | S | — | — | — | — | — | — | |
| | | | | L | — | — | — | — | — | — | |
| $I_{SB1}$ | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$[1] | COM'L | S | 50 | 75 | 40 | 65 | 30 | 55 | mA |
| | | | | L | 50 | 65 | 40 | 50 | 30 | 35 | |
| | | | IND | S | — | — | — | — | — | — | |
| | | | | L | — | — | — | — | — | — | |
| $I_{SB2}$ | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$[3] Active Port Outputs Open, f=$f_{MAX}$[1] | COM'L | S | 110 | 170 | 100 | 160 | 90 | 150 | mA |
| | | | | L | 110 | 150 | 100 | 140 | 90 | 130 | |
| | | | IND | S | — | — | — | — | — | — | |
| | | | | L | — | — | — | — | — | — | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports $\overline{CE}_R$ and $\overline{CE}_L$ ≥ $V_{CC}$ - 0.2V $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V, f = 0[2] | COM'L | S | 1.0 | 5 | 1.0 | 5 | 1.0 | 5 | mA |
| | | | | L | 0.4 | 3 | 0.4 | 3 | 0.4 | 3 | |
| | | | IND | S | — | — | — | — | — | — | |
| | | | | L | — | — | — | — | — | — | |
| $I_{SB4}$ | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{CC}$ - 0.2V[5] $V_{IN}$ ≥ $V_{CC}$ - 0.2V or $V_{IN}$ ≤ 0.2V, Active Port Outputs Open, f = $f_{MAX}$[1] | COM'L | S | 100 | 160 | 90 | 150 | 80 | 140 | mA |
| | | | | L | 100 | 140 | 90 | 130 | 80 | 120 | |
| | | | IND | S | — | — | — | — | — | — | |
| | | | | L | — | — | — | — | — | — | |

3753 tbl 09

**NOTES:**
1. At f = $f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/$t_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. $V_{CC}$ = 3.3V, TA = 25°C for Typ, and are not production tested. $I_{CC\,DC}$(f=0) = 90mA (Typ).
5. $\overline{CE}_X$ = $V_{IL}$ means $\overline{CE}_{0X}$ = $V_{IL}$ and $CE_{1X}$ = $V_{IH}$
   $\overline{CE}_X$ = $V_{IH}$ means $\overline{CE}_{0X}$ = $V_{IH}$ or $CE_{1X}$ = $V_{IL}$
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and $CE_{1X}$ ≥ $V_{CC}$ - 0.2V
   $\overline{CE}_X$ ≥ $V_{CC}$ - 0.2V means $\overline{CE}_{0X}$ ≥ $V_{CC}$ - 0.2V or $CE_{1X}$ ≤ 0.2V
   'X' represents "L" for left port or "R" for right port.
6. 'X' in part number indicates power rating (S or L).
7. Industrial temperature: for specific speeds, packages and powers contact your sales office.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1,2 and 3 |

3753 tbl 10

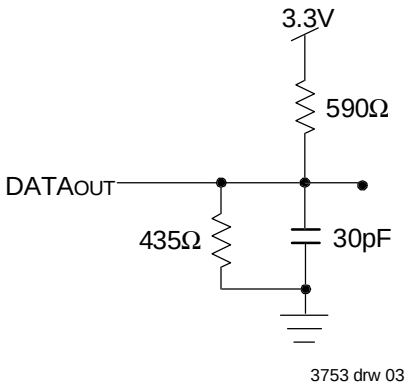



**Figure 1. AC Output Test load.**

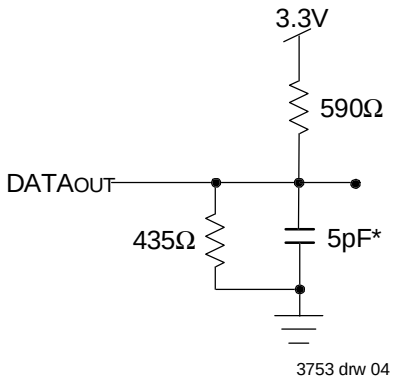



**Figure 2. Output Test Load (For $t_{CKLZ}$, $t_{CKHZ}$, $t_{OLZ}$, and $t_{OHZ}$).**
*Including scope and jig.

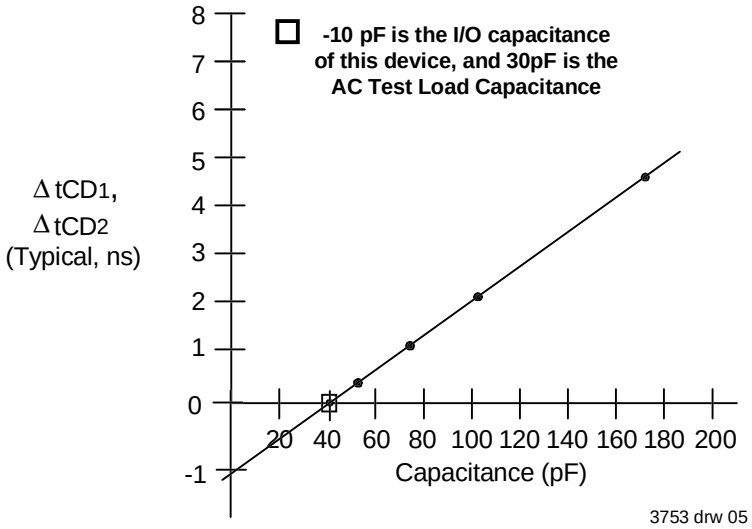



**Figure 3. Typical Output Derating (Lumped Capacitive Load).**

# AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4,5] ($V_{CC}$ = 3.3V ± 0.3, $T_A$ = 0°C to +70°C)

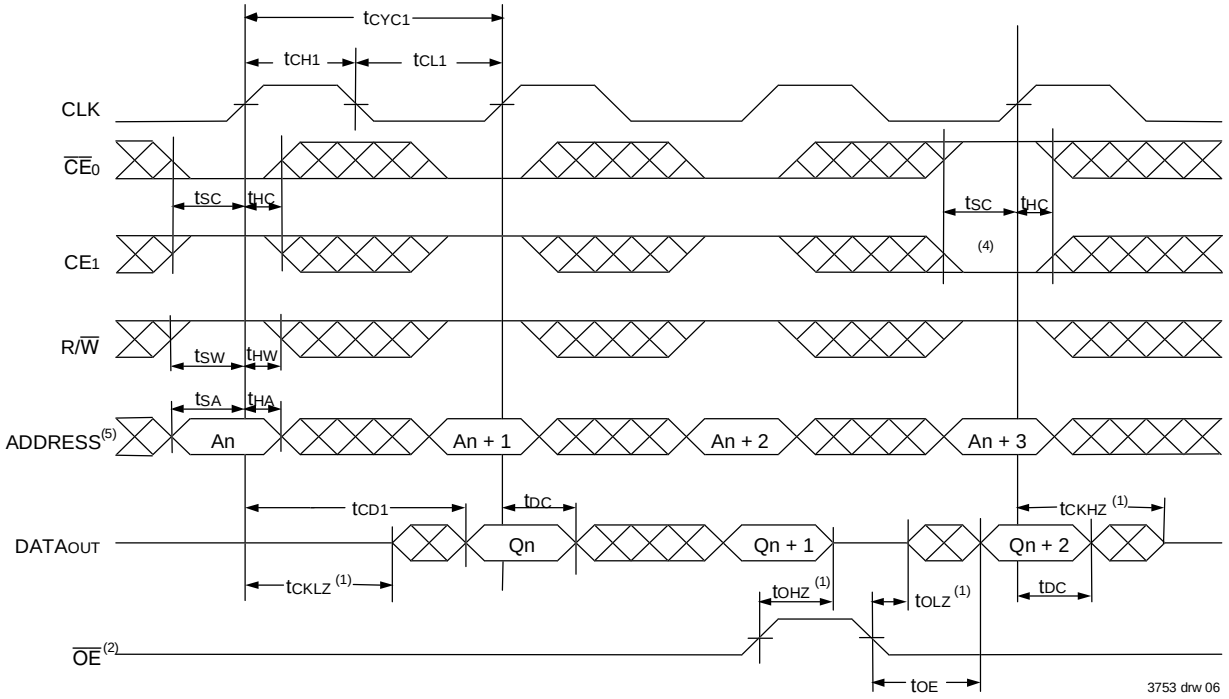
| | | 70V9079X9 Com'l Only | | 70V9079X12 Com'l Only | | 70V9079X15 Com'l Only | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $t_{CYC1}$ | Clock Cycle Time (Flow-Through)[2] | 25 | — | 30 | — | 35 | — | ns |
| $t_{CYC2}$ | Clock Cycle Time (Pipelined)[2] | 15 | — | 20 | — | 25 | — | ns |
| $t_{CH1}$ | Clock High Time (Flow-Through)[2] | 12 | — | 12 | — | 12 | — | ns |
| $t_{CL1}$ | Clock Low Time (Flow-Through)[2] | 12 | — | 12 | — | 12 | — | ns |
| $t_{CH2}$ | Clock High Time (Pipelined)[2] | 6 | — | 8 | — | 10 | — | ns |
| $t_{CL2}$ | Clock Low Time (Pipelined)[2] | 6 | — | 8 | — | 10 | — | ns |
| $t_R$ | Clock Rise Time | — | 3 | — | 3 | — | 3 | ns |
| $t_F$ | Clock Fall Time | — | 3 | — | 3 | — | 3 | ns |
| $t_{SA}$ | Address Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HA}$ | Address Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SC}$ | Chip Enable Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HC}$ | Chip Enable Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SW}$ | R/$\overline{W}$ Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HW}$ | R/$\overline{W}$ Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SD}$ | Input Data Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HD}$ | Input Data Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SAD}$ | $\overline{ADS}$ Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{SRST}$ | $\overline{CNTRST}$ Setup Time | 4 | — | 4 | — | 4 | — | ns |
| $t_{HRST}$ | $\overline{CNTRST}$ Hold Time | 1 | — | 1 | — | 1 | — | ns |
| $t_{OE}$ | Output Enable to Data Valid | — | 12 | — | 12 | — | 15 | ns |
| $t_{OLZ}$ | Output Enable to Output Low-Z[1] | 2 | — | 2 | — | 2 | — | ns |
| $t_{OHZ}$ | Output Enable to Output High-Z[1] | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| $t_{CD1}$ | Clock to Data Valid (Flow-Through)[2] | — | 20 | — | 25 | — | 30 | ns |
| $t_{CD2}$ | Clock to Data Valid (Pipelined)[2] | — | 9 | — | 12 | — | 15 | ns |
| $t_{DC}$ | Data Output Hold After Clock High | 2 | — | 2 | — | 2 | — | ns |
| $t_{CKHZ}$ | Clock High to Output High-Z[1] | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| $t_{CKLZ}$ | Clock High to Output Low-Z[1] | 2 | — | 2 | — | 2 | — | ns |
| **Port-to-Port Delay** | | | | | | | | |
| $t_{CWDD}$ | Write Port Clock High to Read Data Delay | — | 35 | — | 40 | — | 50 | ns |
| $t_{CCS}$ | Clock-to-Clock Setup Time | — | 15 | — | 15 | — | 20 | ns |

3753 tbl 11

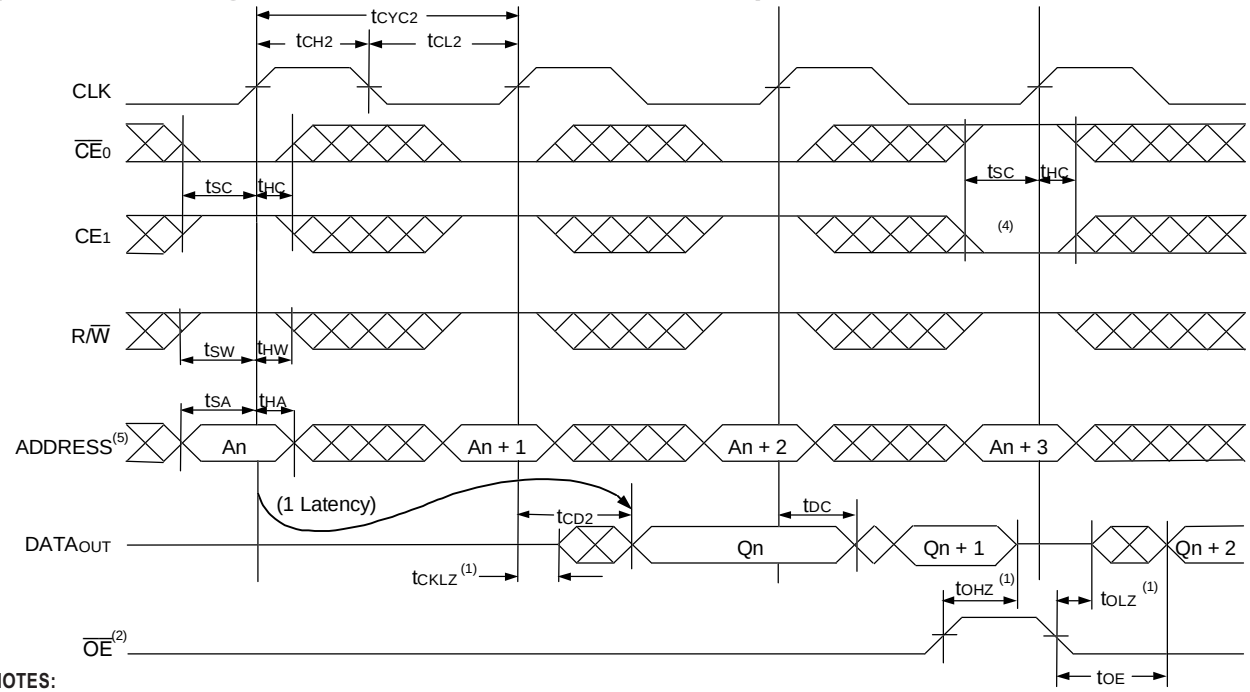
**NOTES:**

1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters ($t_{CYC2}$, $t_{CD2}$) always apply to the Left Port. The Right Port uses the Pipelined $t_{CYC2}$ and $t_{CD2}$ when $\overline{FT}$/PIPE$_R$ = $V_{IH}$ and the Flow-Through parameters ($t_{CYC1}$, $t_{CD1}$) when $\overline{FT}$/PIPE$_R$ = $V_{IL}$.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE$_R$. $\overline{FT}$/PIPE$_R$ should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).
5. Industrial temperature: for specific speeds, packages and powers contact your sales office.

## Timing Waveform Read Cycle for Flow-Through Output on Right Port ($\overline{FT}$/PIPE$_R$ = $V_{IL}$)(3)



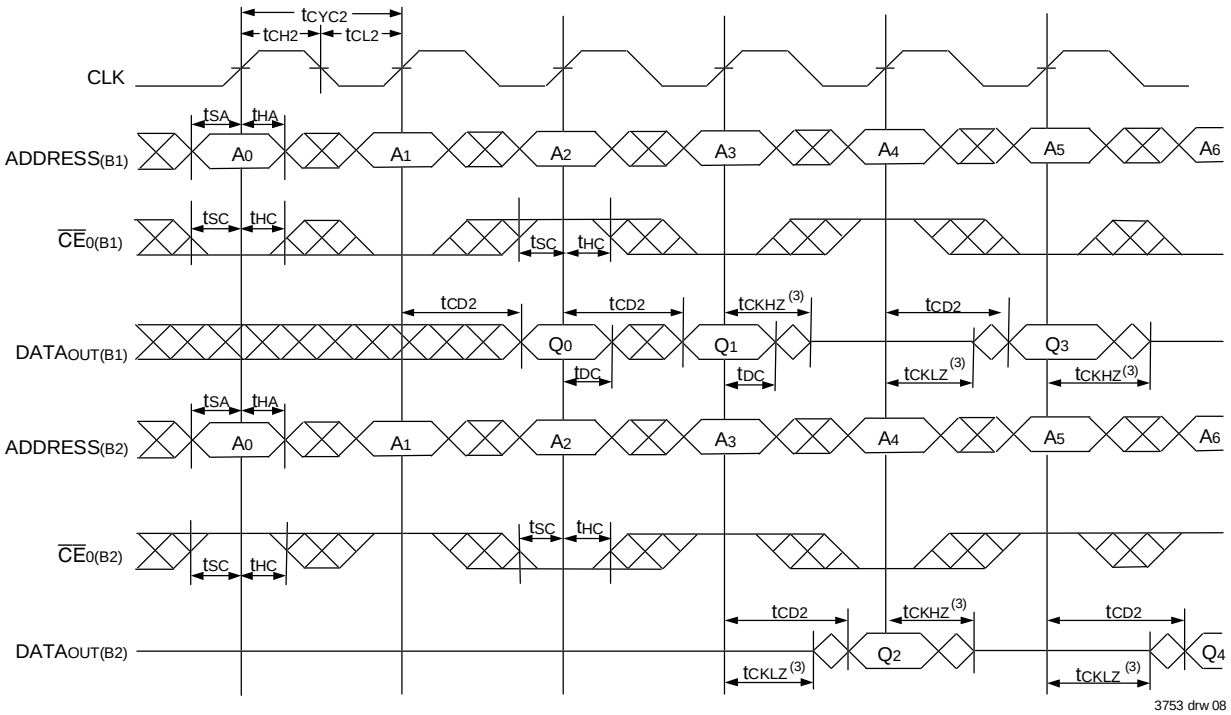

## Timing Waveform of Read Cycle for Pipeline Operation (Left Port; Right Port when $\overline{FT}$/PIPE$_R$ = $V_{IH}$)(3)




**NOTES:**

1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
4. The output is disabled (HIGH-impedance state) by $\overline{CE}_0$ = $V_{IH}$ or $CE_1$ = $V_{IL}$ following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.

## Timing Waveform of a Bank Select Pipelined Read(1,2)

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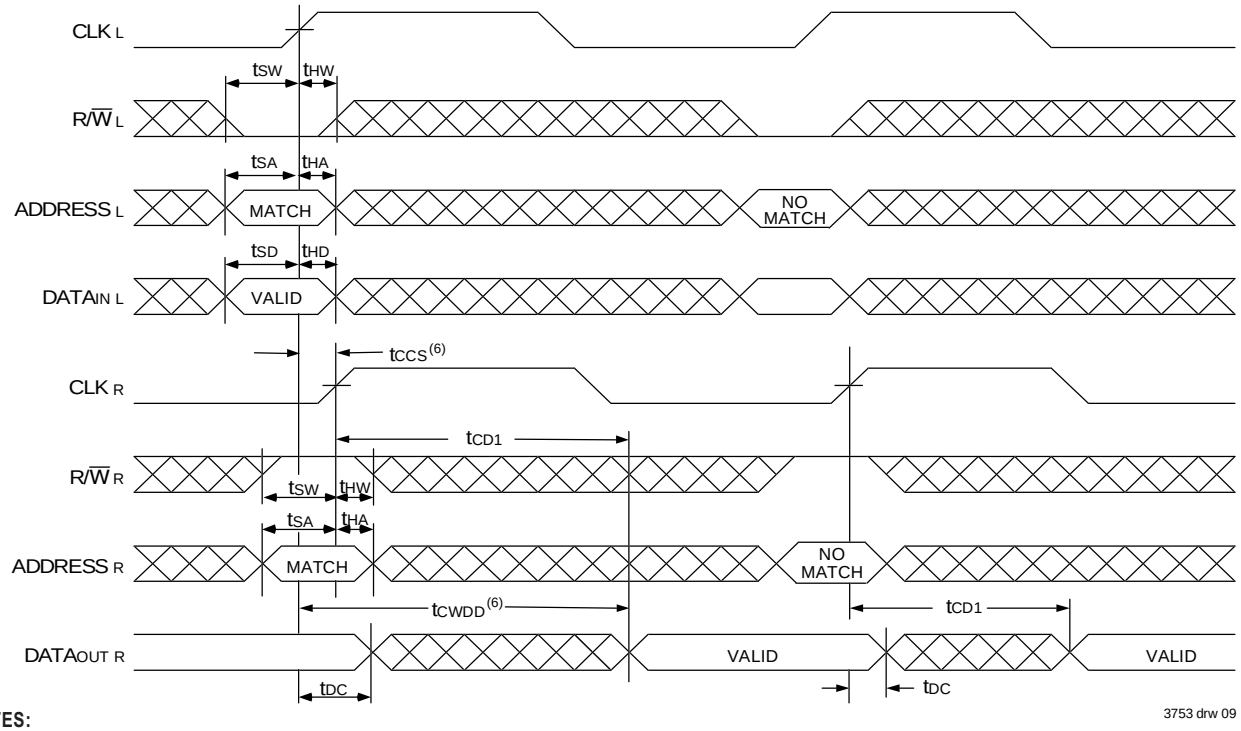
## Timing Waveform of a Left Port Write of Flow-Through Right Port Read(4,5)

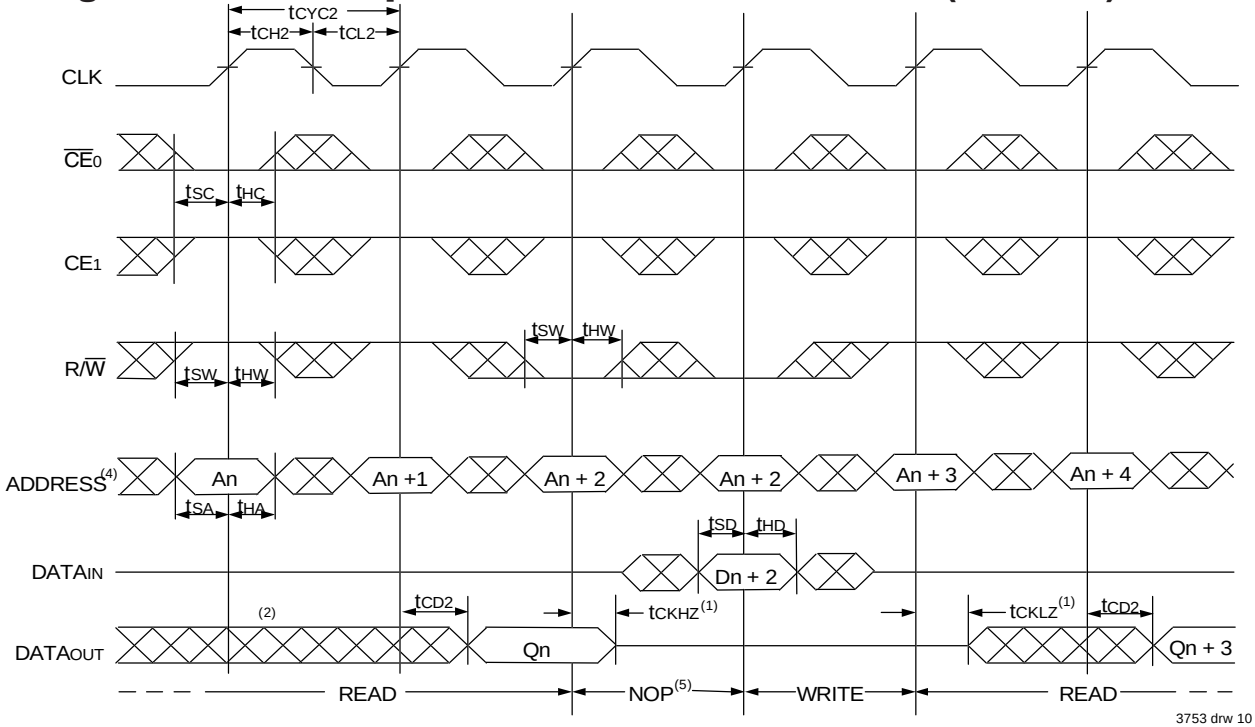



3753 drw 09

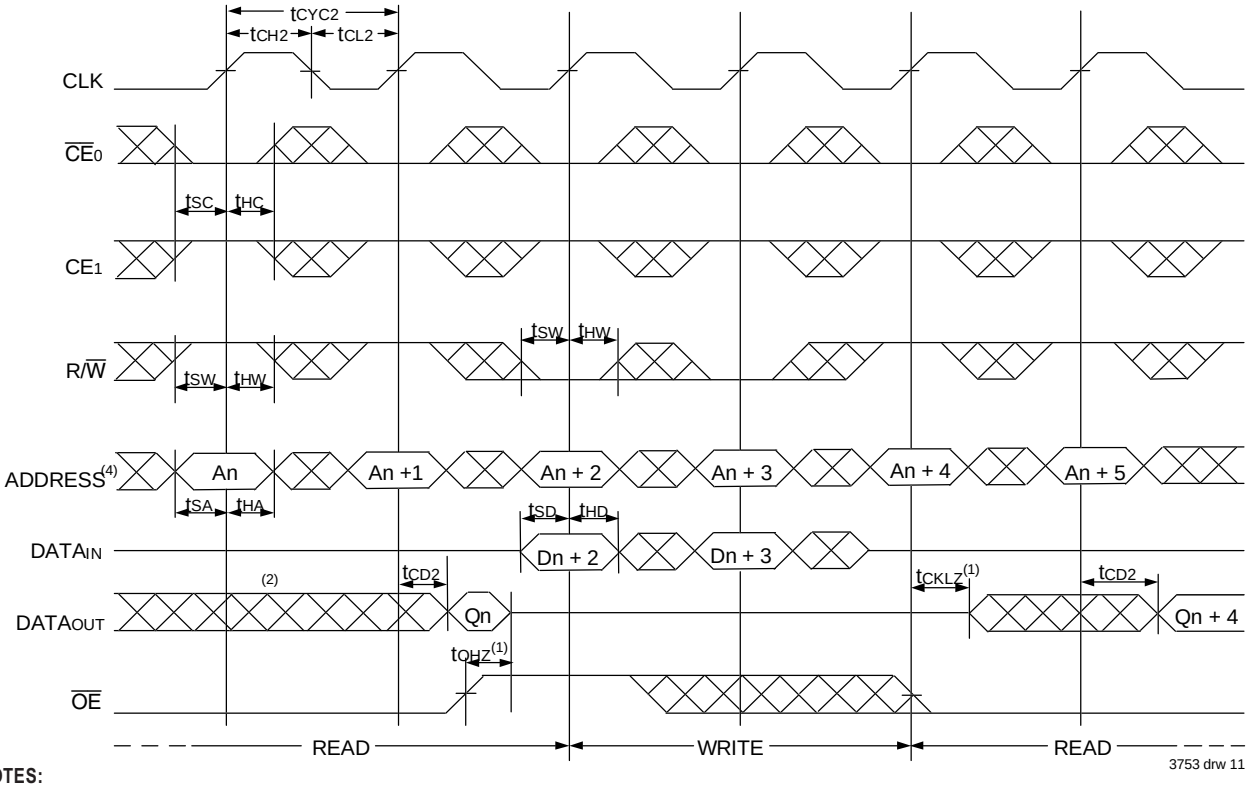
**NOTES:**

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9079 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{OE}$ and $\overline{ADS}$ = VIL; CE1(B1), CE1(B2), R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
3. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}_0$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
5. $\overline{OE}$ = VIL for the Right Port, which is being read from. $\overline{OE}$ = VIH for the Left Port, which is being written to.
6. If tCCS ≤ maximum specified, then data from right port READ is not valid until the maximum specified for tCWDD. If tCCS > maximum specified, then data from right port READ is not valid until tCCS + tCD1. tCWDD does not apply in this case.

## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



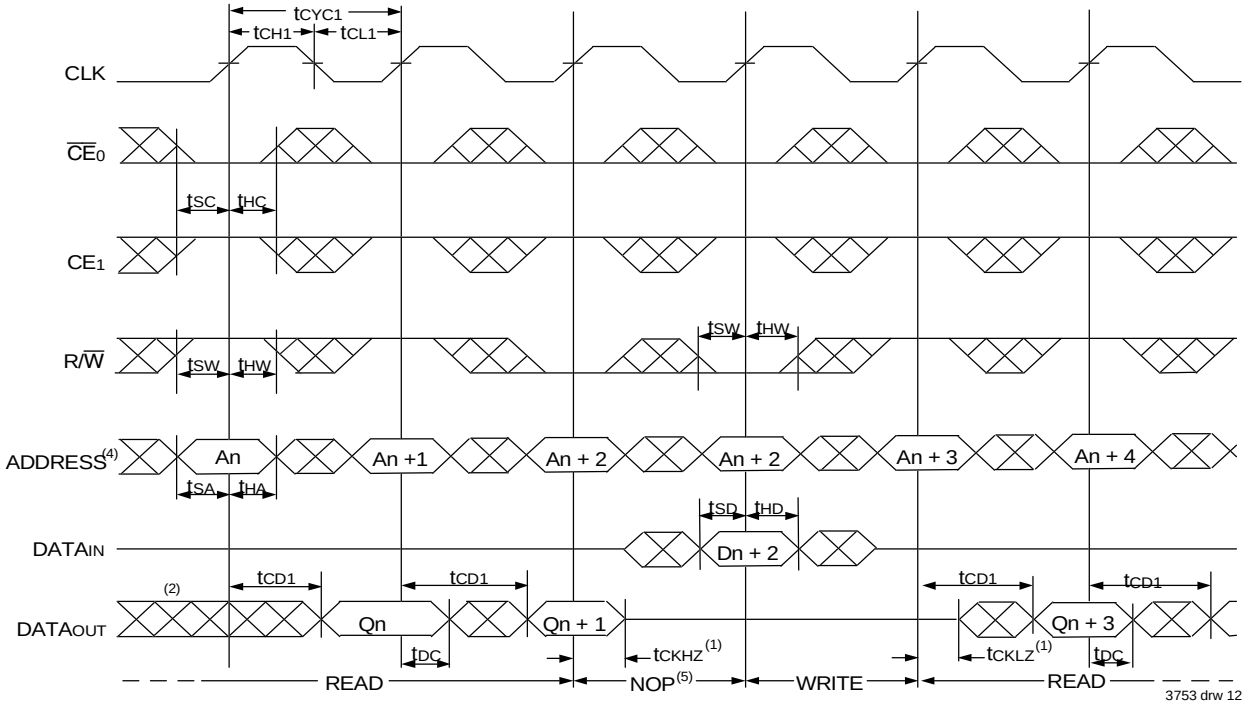

## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)



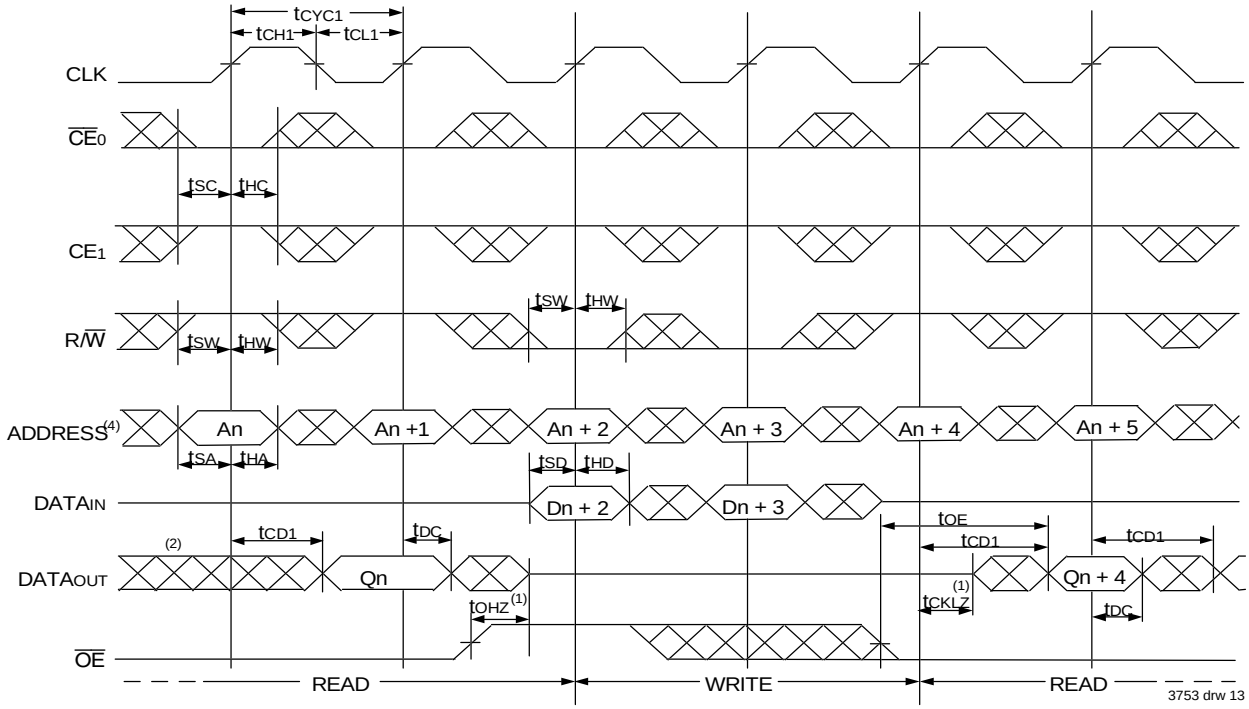

**NOTES:**

1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE_0}$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



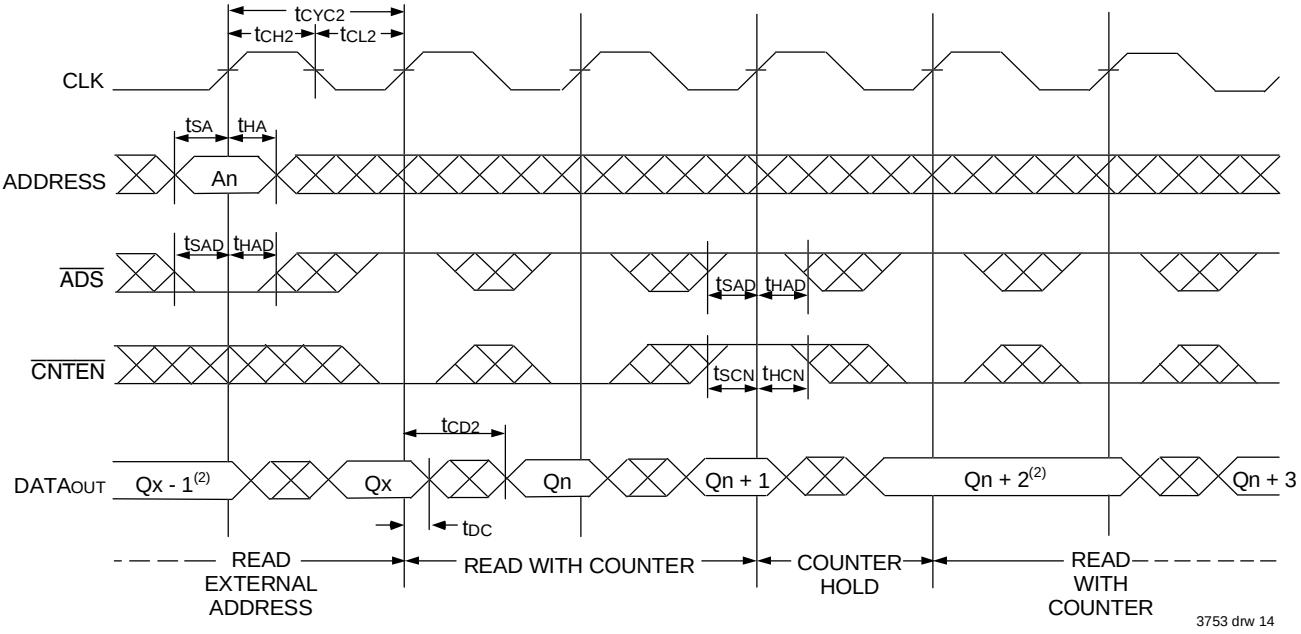

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)



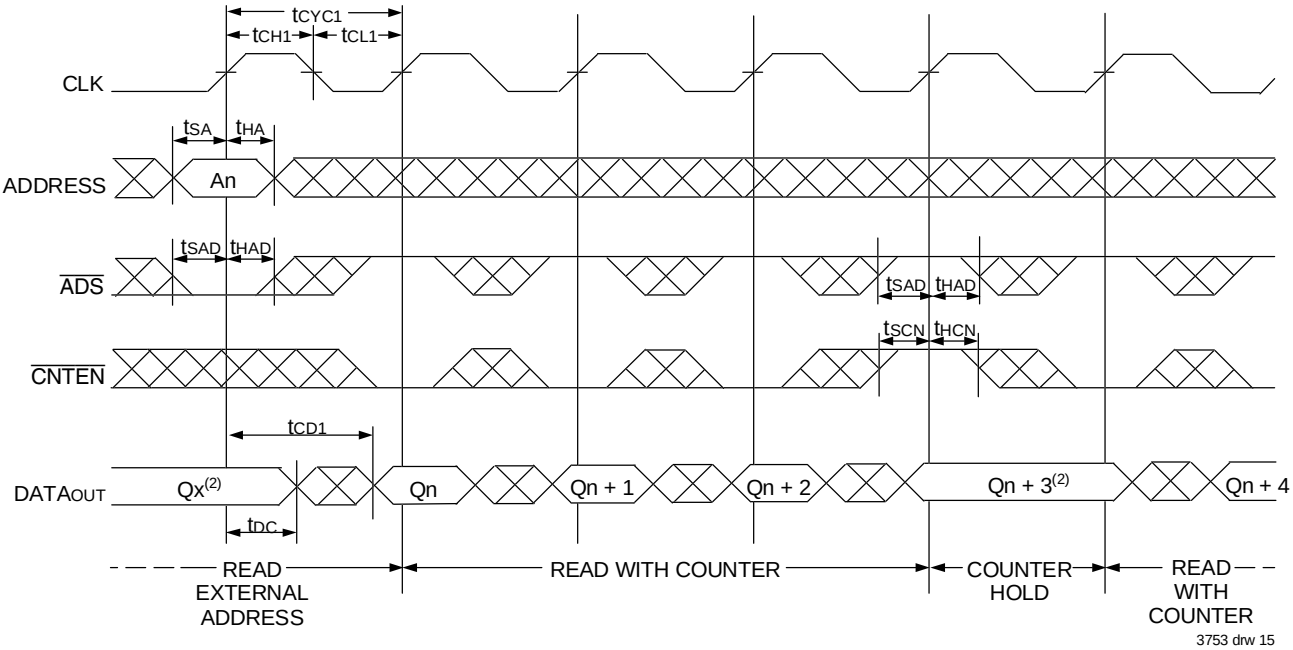

**NOTES:**

1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

## Timing Waveform of Pipelined Read with Address Counter Advance(1)



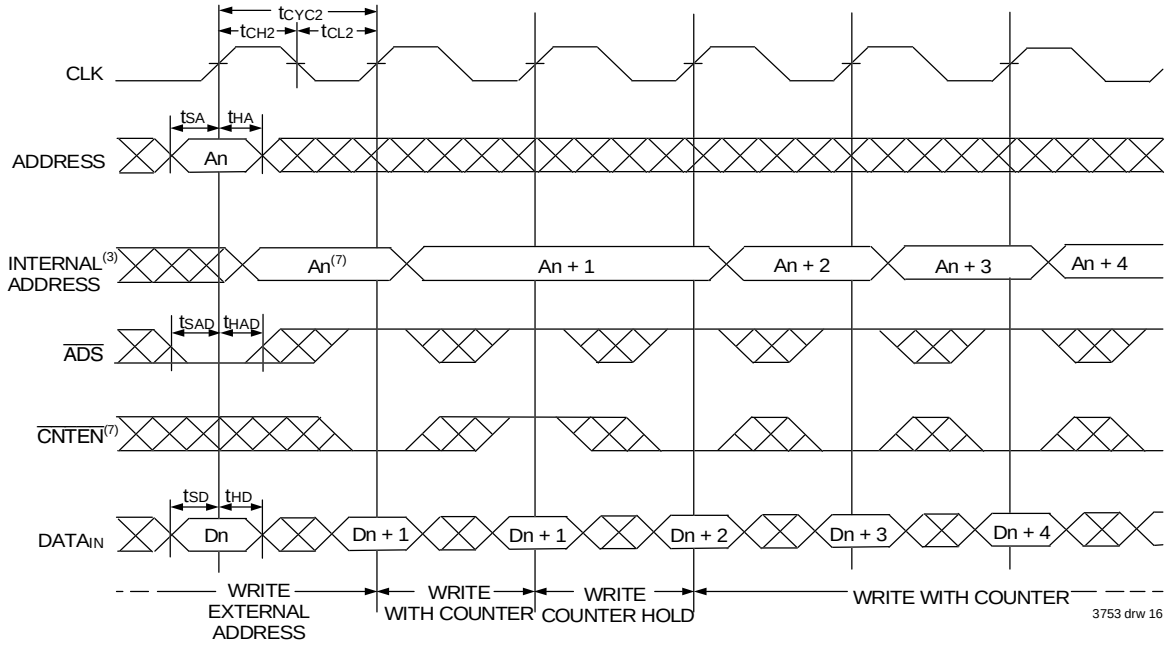

## Timing Waveform of Flow-Through Counter Read with Address Counter Advance(1)



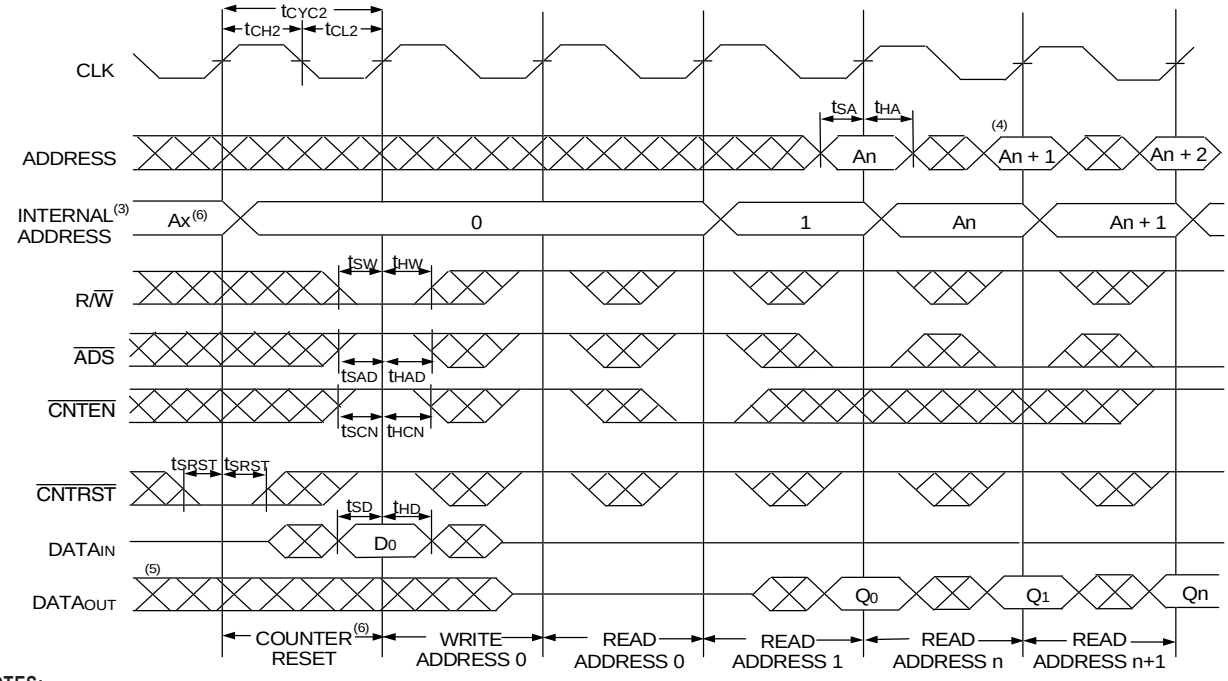

**NOTES:**

1. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$, R/$\overline{W}$, and $\overline{CNTRST}$ = $V_{IH}$.
2. If there is no address change via $\overline{ADS}$ = $V_{IL}$ (loading a new address) or $\overline{CNTEN}$ = $V_{IL}$ (advancing the address), i.e. $\overline{ADS}$ = $V_{IH}$ and $\overline{CNTEN}$ = $V_{IH}$, then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)




## Timing Waveform of Counter Reset (Pipelined Outputs)(2)




**NOTES:**

1. $\overline{CE_0}$ and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{CNTRST}$ = $V_{IH}$.
2. $\overline{CE_0}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = $V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

## Functional Description

The IDT70V9079 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the counter registers for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on $CE_1$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9079's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and $CE_1$ HIGH to re-activate the outputs.

## Depth and Width Expansion

The IDT70V9079 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The 70V9079 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.

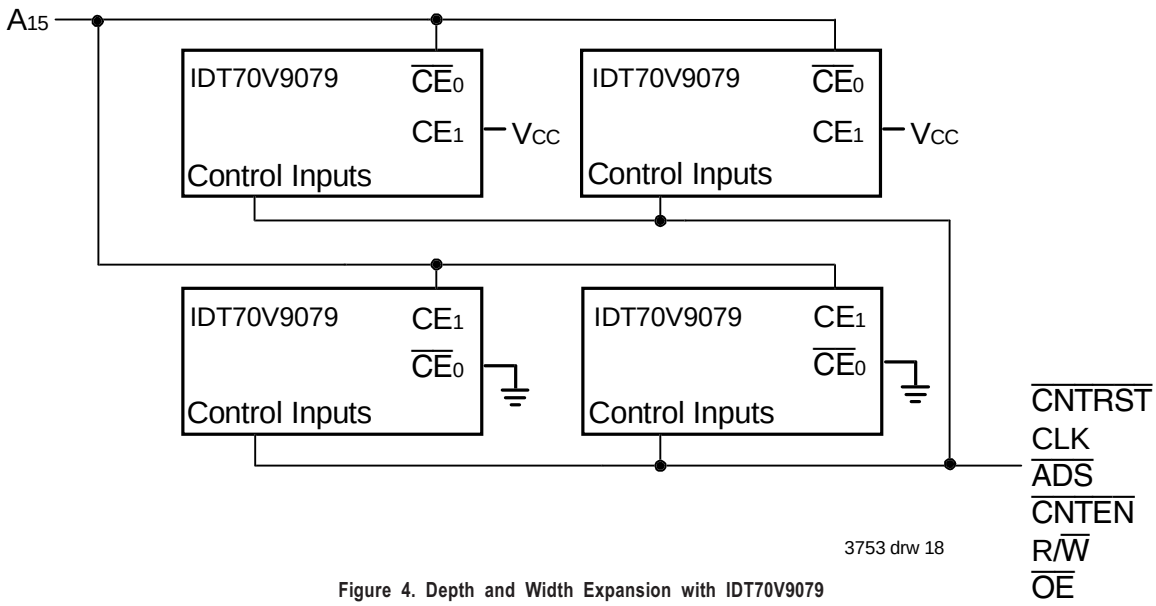
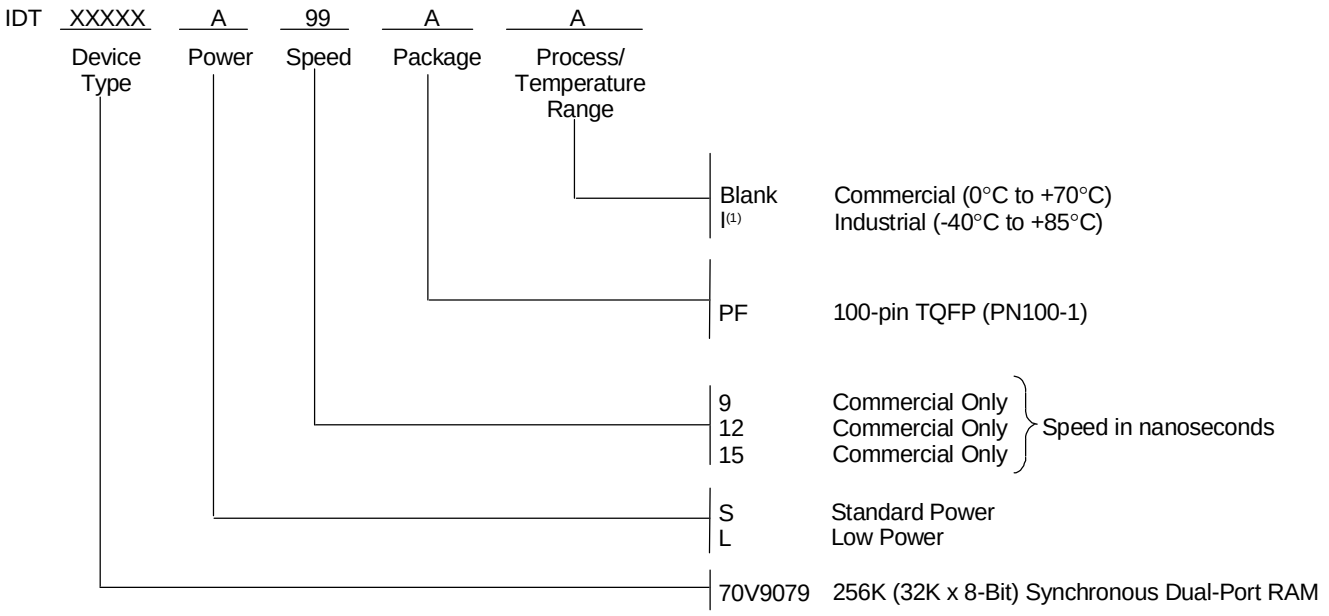



**Figure 4. Depth and Width Expansion with IDT70V9079**

## Ordering Information




3753 drw 19

**NOTE:**
1. Industrial temperature range is available.
   For specific speeds, packages and powers contact your sales office.

## Preliminary Datasheet: Definition

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

## Datasheet Document History

| | |
|---|---|
| 1/12/99: | Initiated datasheet document history |
| | Converted to new format |
| | Cosmetic and typographical corrections |
| | Added additional notes to pin configurations |
| | Page 14 Added Depth and Width Expansion section |
| 6/11/99: | Page 3 Deleted note 6 for Table II |

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