



EMIF04-MMC02F1

IPAD™

4 LINES EMI FILTER INCLUDING ESD PROTECTION

MAIN APPLICATION

- MULTIMEDIACARD™

DESCRIPTION

The EMIF04-MMC02F1 is a highly integrated array designed to suppress EMI / RFI noise for MULTIMEDIACARD™ port filtering.

The EMIF04-MMC02F1 flip-chip packaging means the package size is equal to the die size. That's why EMIF04-MMC02F1 is a very small device.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

BENEFITS

- 4 lines low-pass-filter
- High efficiency in EMI filtering
- Very low PCB space consuming: < 3.3 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

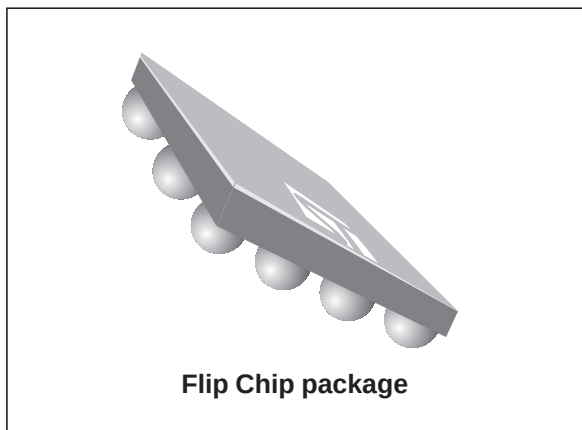
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 61000-4-2 Level 4:

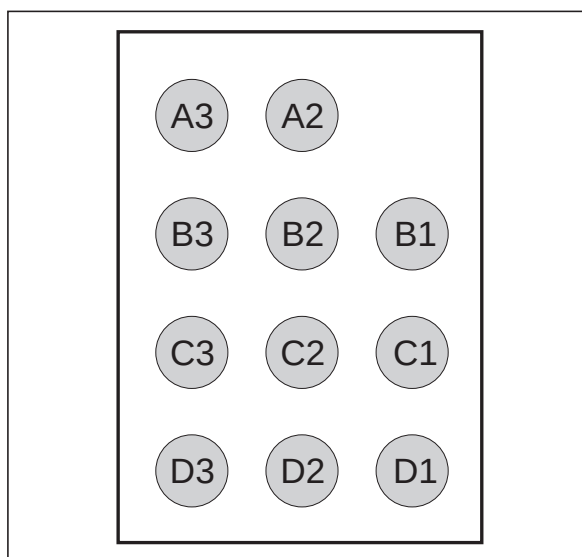
15kV (air discharge)
8 kV (contact discharge)

on input & output pins.

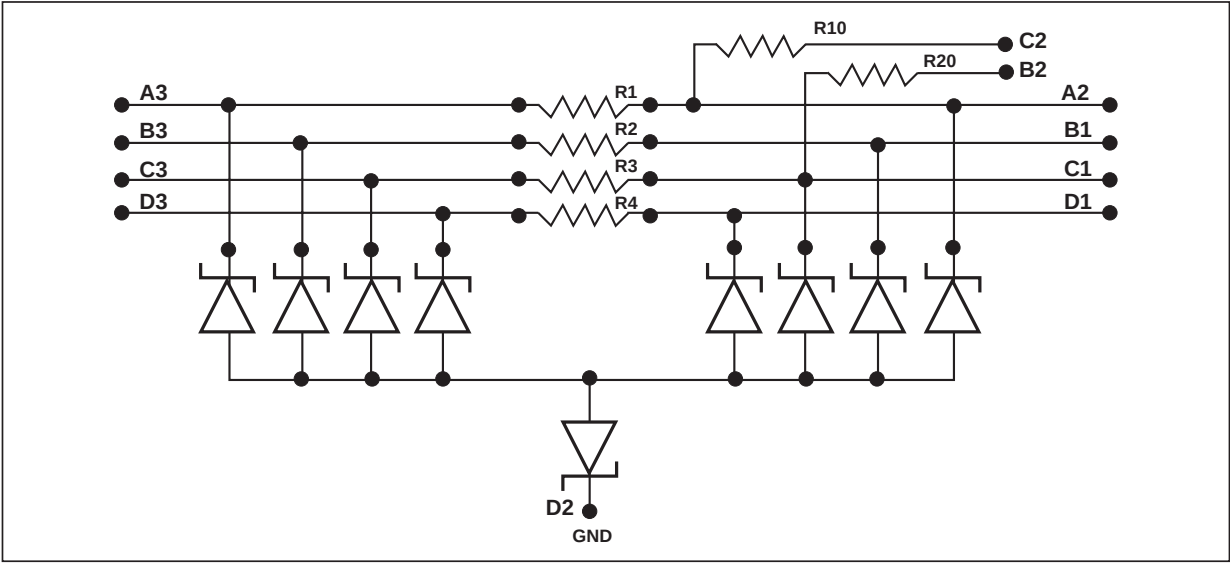
MIL STD 883E - Method 3015-6 Class 3



PIN CONFIGURATION



SCHEMATIC

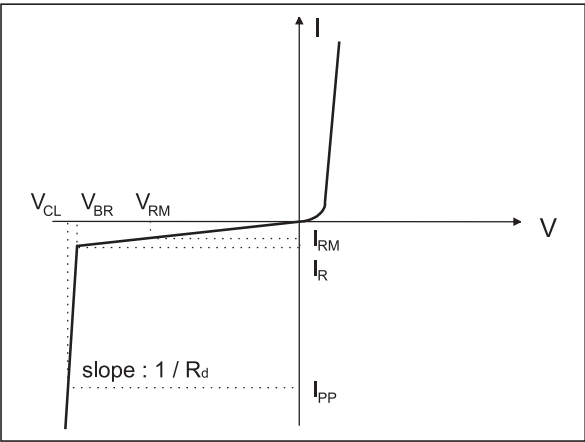


ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

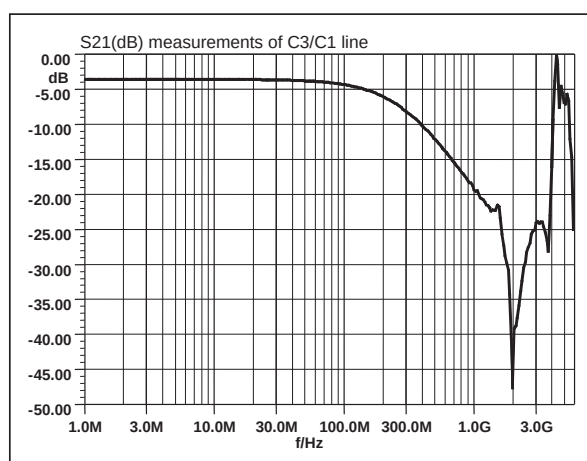
ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1 \text{ mA}$	6			V
I_{RM}	$V_{RM} = 3 \text{ V}$		0.1	0.5	μA
C_{line}	@ 0V			20	pF
R_1, R_2, R_3, R_4	Tolerance $\pm 5\%$		47		Ω
R_{10}	Tolerance $\pm 5\%$		13		$\text{k}\Omega$
R_{20}	Tolerance $\pm 5\%$		56		$\text{k}\Omega$
P				70	mW

Fig. 1: Filtering measurements



Note: spikes at high frequencies are induced by the PCB layout.

Fig. 2: Cross talk measurements

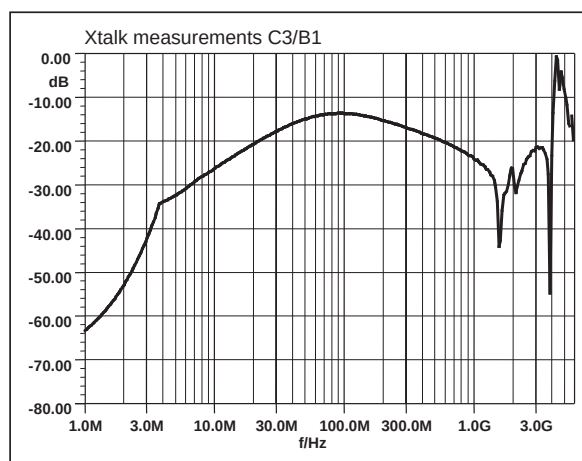


Fig. 3: Line capacitance versus reverse applied voltage.

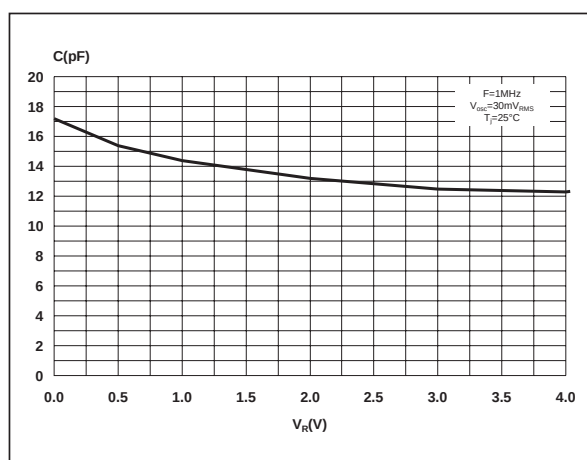
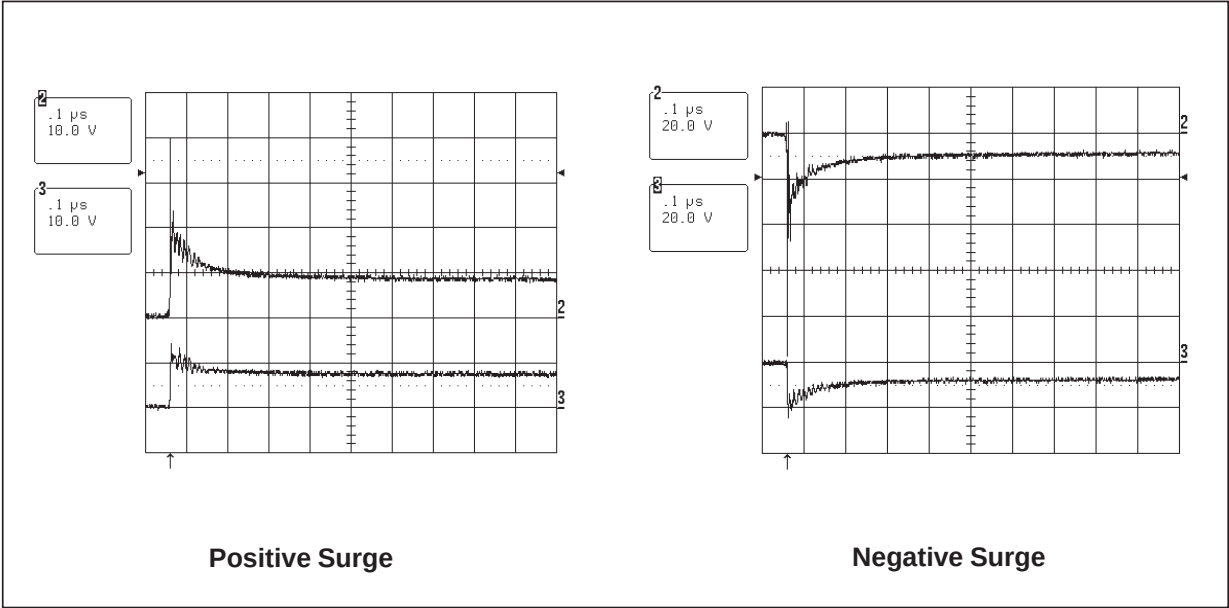


Fig. 4: ESD response to IEC61000-4-2 (+15kV contact discharge).



APLAC MODEL

Fig. 5: Device structure

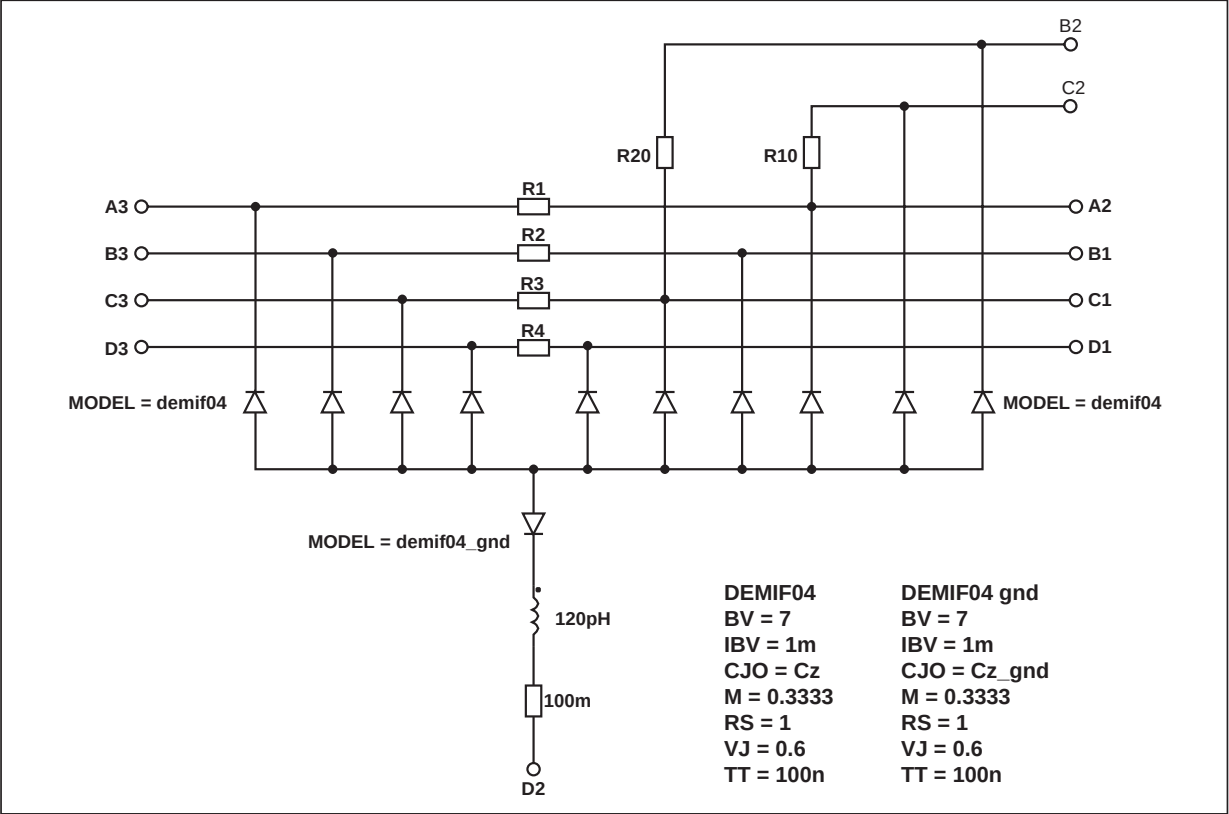
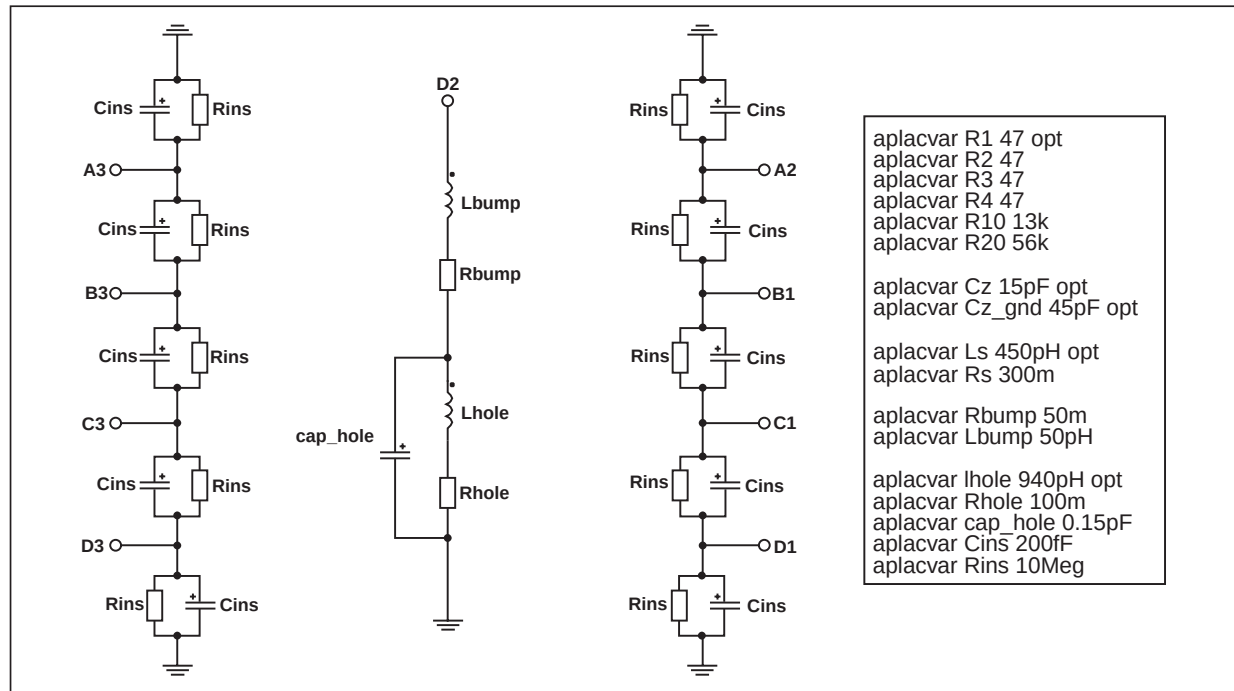
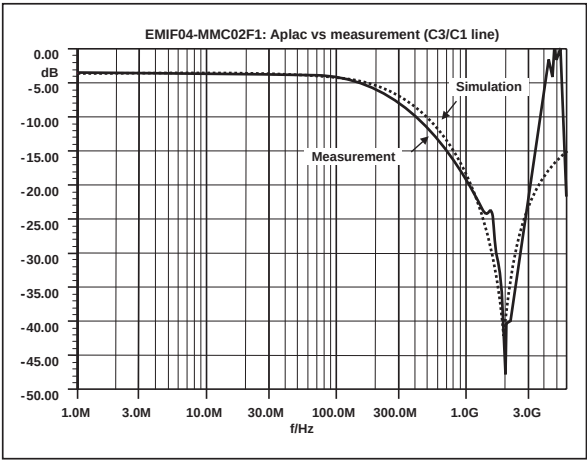


Fig. 6: Aplac model connections

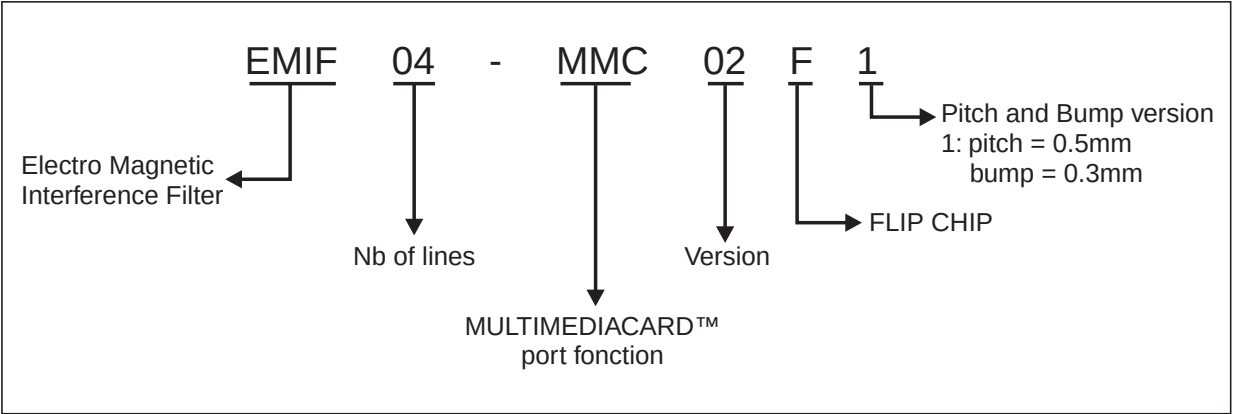


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Fig. 7: Aplac simulation versus frequency measurement.



ORDER CODE



PACKAGE MECHANICAL DATA

