



1. FEATURE

Host Interface

- PCMCIA 2.1 and PC Card ATA standard compatible.
 - Memory mapped or I/O operation.
- Compatible with all PC Card Services and Socket Service.
- Fast ATA host-to-buffer burst transfer rates up to 20MB/sec. which support PIO mode 4(16.6MB/sec) and DMA mode 2(16.6MB/sec).
- Automatic sensing of PCMCIA or True IDE host interface.
- Integrated PCMCIA attribute memory of 256 bytes (CIS)
 - CIS and Buffer RAM use same SRAM area to simplify internal bus design
- PCMCIA card configuration register support.
- Polarity control for Host reset signal.
- PCMCIA twin card support.
- PCMCIA based ATA address decode support.
- Emulate the IBM task file for PC/AT.
- Separate status for Host reset signal and Host program reset.
- Separate Host and Disk interrupt pins.

Flash Memory Interface

- Support all the control signals to execute read/ write/ erase operation for flash memory.
- Flexible Disk Capacity Configuration for series type or linear type flash memory
 - Upto 32MB(unformatted) capacity for 16 pcs. 16Mbit linear type flash memory.
 - Upto 1GB(unformatted) capacity for 32 pcs. 256Mbit series type flash memory.
- Flash Memory Power Down or write protect control support.
- Flash Memory Ready/Busy status detect.
- Inverted data bus control to reduce flash memory program/erase operation in DOS FAT and ECC code field.
- Optional store firmware in flash memory array w/o external ROM while MXIC's MX29F1610(linear type) used.
 - Allow code fetch in Shadow ROM during flash memory program or erase.

Buffer RAM Manager

- Dual port circular Buffer RAM control
- 1KB data Buffer RAM.
- Automatically correct error data in Buffer RAM.
 - Single word error correct and double word detect.
- Provide logic to speed up Buffer RAM access.
- Support 8 bit as well as 16 bit transfer on host bus.

DSP core

- High performance MX93011 DSP (21Mips) core.
- 4KB Internal RAM(direct access).
- 2KB Internal expansion RAM(indirect access) for store data or shadow ROM space.
- ICE debugging mode supported to ease system verification.
- Lower power and automatic power saving operation.
 - Automatic Standby Mode. (Operating Current < 10mA, VCC=5.5V), wake-up by interrupt signal.
 - Very Low Operating Current Sleep Mode. (<1mA, VCC=5.5V), wake-up by Host reset signal or Host program reset or ATA command asserted by host.

Technology

- 128 pin LQFP(14X14X1.4 mm³)
- 0.6um Low-power, High-speed CMOS technology.
- 5Volt \pm 10% or 3.3Volt \pm 5%.

Utility Support

- Provide integrated test environment with 82365SL-compatible adaptor.
- Firmware upload from host and allows easy upgrade for custom feature.
- Physical devices test cover basic PCB test after assembly and more detail analysis.
- Logical sector test cover SSD functionality and data transfer test.

2. GENERAL DESCRIPTION

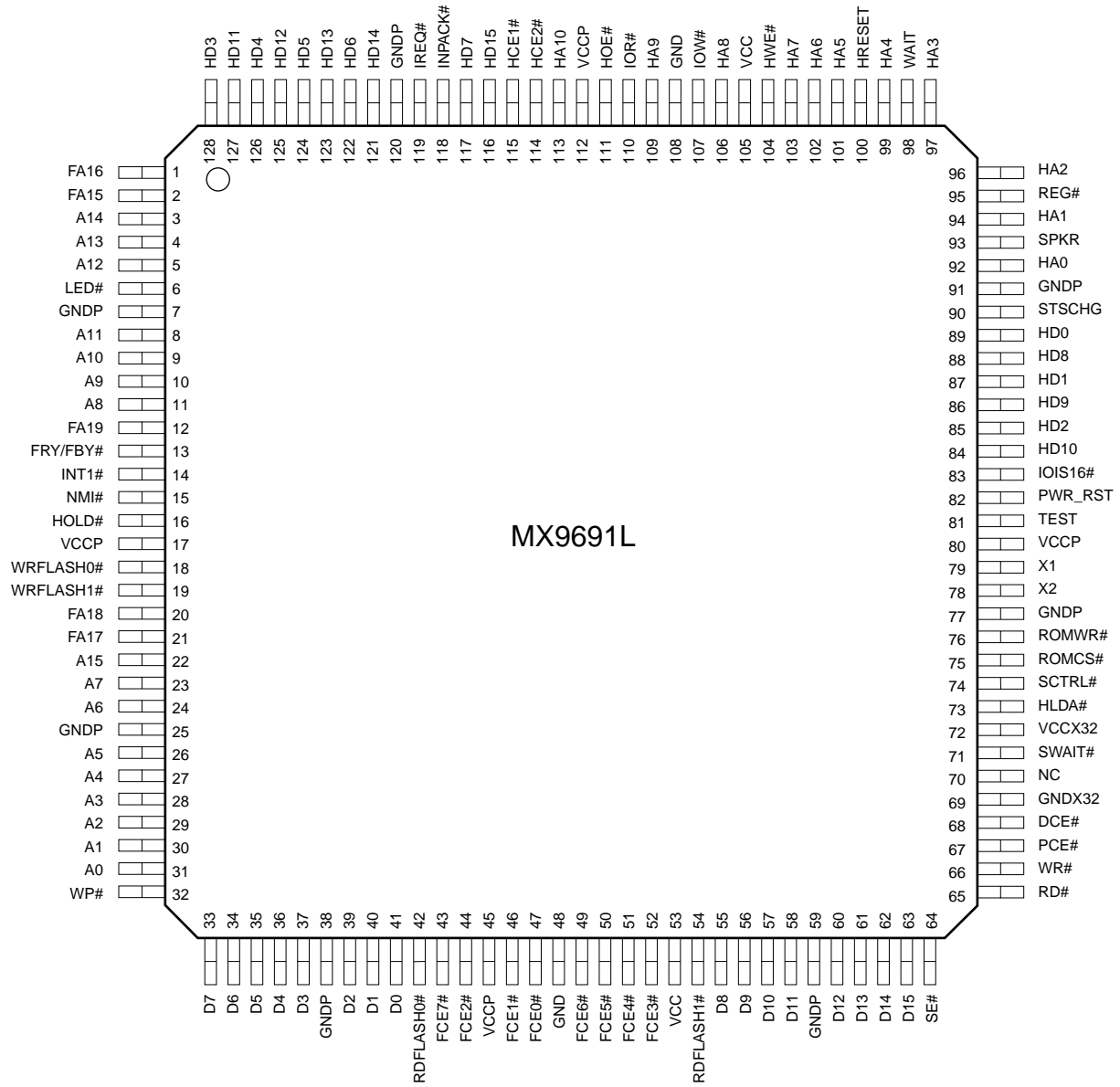
The Macronix's Solid State Disk controller **MX9691L** is a wide-range supply voltage(3.3Volt~5Volt) and fully integrated flash memory controller that provides all the control logic for PCMCIA/True IDE host and flash memory. The **MX9691L** combines 1KB dual-port buffer and buffer manager, integrated MX93011 DSP core, and a complete host interface for both the PC Card ATA and True IDE standard.

The **MX9691L** provides flexible disk capacity configuration and supports all the control signals to execute read/write/erase operation for linear type or series type flash memory chip. It is typically configured with up to 32MB(unformatted) capacity for 16 pcs. 16Mbit linear flash memory or 1GB(unformatted) capacity for 32 pcs. 256Mbit series type flash memory while capacity extension mode is enabled for series type flash memory used. The **MX9691L** also provides flexible architecture to implement defect management and wear-leveling by firmware for series type or linear type flash memory.

In linear mode, the linear type 16 Mbit flash memory is supported, such as MXIC's MX29F1610 etc. In flash memory interface there are two banks of flash memory to be provided. Each bank support 8 pcs. flash memory when linear type flash memory is used. In series mode, the series type 16MBit/32Mbit/64Mbit/256Mbit flash memory is supported, such as Toshiba's TC5816FT/TR or TC58V32FT, Samsung's KM29N16000T/R or KM29N32000TS/RS etc. Each bank support or 16 pcs. flash memory when series type flash memory is used.

The **MX9691L** is fully compliant with the PC Card ATA specification. It includes 256 bytes of integrated attribute memory(for the required Card Information Structure) and four Card Configuration registers. The PCMCIA device driver can access the **MX9691L**'s ATA command block through four different modes by writing the different modes by writing the configuration index of the attribute memory configuration option register.

3. PIN CONFIGURATION



4. PIN DESCRIPTION
Host Interface

Symbol	No.	Type	Description
HA[10:0]	92,94, 96-97,99 101-103, 106,109, 113	I (CMOS)	Host address line 10-0. These pins include internal pull-up resistors.
HD[15:0]	84-89, 116-117, 121-128	I/O (TTL)	Host data line 15-0. These pins include internal bus holder circuit that keep previous state when tri-state.
HOE#,HWE#	104,111	I (CMOS)	Host memory read/write/mode select : Both pins include internal pull-up resistors that is default in PCMCIA mode.
IOR#,IOW#	107,110	I (CMOS)	Host I/O access. Both pins include internal pull-up resistor.
HRESET/HRESET#	100	I (CMOS)	The host reset signal, when active, initializes the control/status registers and stops any command in process. In PCMCIA mode, the signal is active high. In True IDE mode, this signal is active low. This signal include internal pull-down resistor.
WAIT/ IOCHRDY	98	O,OD (CMOS)	WAIT or INPUT CHANNEL READY : In both PCMCIA and True IDE modes, this signal holds host transfers until the controller is ready to respond.
RDY/BSY#/ IREQ#/ HOSTINT	119	O, Z (CMOS)	READY/BUSY or HOST INTERRUPT : In PCMCIA mode, this signal has two functions. In PCMCIA common memory mode, this signal is ready/busy. It is asserted busy by the reset logic, and can be deasserted by the DSP or represents the ready/busy bit of ATA status register. In PCMCIA I/O mode, this signal is IREQ#. In True IDE mode, this active high signal is HOSTINT, which, when enable, send an interrupt to the host.



Symbol	No.	Type	Description
WP/IOCS16#	83	O,OD (CMOS)	WRITE PROTECT or 16-bit I/O TRANSFER : In PCMCIA mode, this bit has two functions. In PCMCIA common-memory mode, this signal indicates write protect. In PCMCIA I/O mode, when IOIS16# is asserted low, it indicates that a 16-bit data transfer is active on PCMCIA bus. In True IDE mode, the IOCS16# signal indicates that a 16-bit buffer transfer is active on the host bus. This open drain signal is only driven on assertion(low).
REG#/DACK#	95	I (CMOS)	Attribute memory and I/O select : In PCMCIA mode, this signal is used to select attribute memory and I/O space. In True IDE mode, this signal is used during DMA with the DREQ, IOR# and IOW# signals to transfer data between the host and the MX9691L. This pin includes an internal pull-up resistor.
HCE1#/ CS1FX#	115	I (CMOS)	Card enable 1 or Chip select 0:In PCMCIA mode, this signal is card enable 1. This signal can enable either even or odd numbered-address bytes onto HD7:0. In True IDE mode, this signal accesses the MX9691 command block registers. This input is ignored during DMA data transfer, i.e. when the DACK# signal is low. This pin includes an internal pull-up resistor.
HCE2#/ CS3FX#	114	I (CMOS)	Card enable 2 or Chip select 1: In PCMCIA mode, this signal is card enable 2. This signal can enable odd numbered-address bytes onto HD15:8. In True IDE mode, this signal accesses the MX9691L control block registers. This pin includes an internal pull-up resistor.
INPACK#/ DREQ	118	O (CMOS)	Input Acknowledge or DMA request :In PCMCIA mode, this signal is asserted when the MX9691 is configured to respond to I/O card read cycles at all addresses. In True IDE mode, this signal is DREQ and is issued during DMA transfers to indicate that the MX9691L is ready for DMA transfer.
SPKR/DASP#	93	I/O (CMOS)	Speaker or slave present : In PCMCIA mode, the output-enable for this signal is controlled by the card configuration registers. In True IDE mode, this signal is used as the slave-present detector.
STSCHG/ PDIAG#	90	I/O (CMOS)	Status change or pass diagnostics :In PCMCIA mode, this signal is used to indicate changes in the RDY/BSY#, WP signals in card configuration registers. In True IDE mode, this active low signal is used between two embedded ATA drive to indicate that the drive in slave mode has passed diagnostics.

External Memory Bus Interface

Symbol	No.	Type	Description
D[15:0]	33-37,39-41, 55-58,60-63	I/O (CMOS)	DSP IO/RAM/ROM/FLASH memory array external data bus. These pins include internal pull- up resistors.
A[15:0]	3-5,8-11, 22-24,26-31	I/O (CMOS)	In Free-run mode, these signals are output that used as DSP IO/RAM/ROM external address. A14-A0 are used for flash memory array address also. In upgrade mode, these address are used for ROM address that controlled by CYH,CYL registers. In ICE-debugging mode,these address are input, asserted by DSP ICE(external MX93011 DSP). And the internal DSP is disabled at this time. These pins include internal pull-up resistors.
PCE#	67	I/O (TTL)	In Free-run mode, this signal is output that is used as external program chip enable. In upgrade mode, this signal is driven to high. In ICE-debugging mode, this signal is input, asserted by DSP ICE(external MX93011 DSP). And the internal DSP is disabled at this time. This pin includes a bus holder circuit.
DCE#	68	I/O (TTL)	In Free-run mode, this signal is output that is used as external data chip enable. In upgrade mode, this signal is driven to high. In ICE-debugging mode, this signal is input, asserted by DSP ICE(external MX93011 DSP). And the internal DSP is disabled at this time. This pin includes a bus holder circuit.
RD#	65	I/O (TTL)	In Free-run mode, this signal is output that is used as DSP IO/RAM/ROM external read. In upgrade mode, this signal is output and asserted when the data register is read in host interface. In ICE-debugging mode, this signal is input, as serted by DSP ICE(external MX93011 DSP). And the internal DSP is disabled at this time. This pin includes a bus holder circuit.
WR#	66	I/O (TTL)	In Free-run mode, this signal is output that is used as DSP IO/RAM/ROM external write. In upgrade mode, this signal is driven to high. In ICE-debugging mode, this signal is input, asserted by DSP ICE(external MX93011 DSP). And the internal DSP is disabled at this time. This pin includes a bus holder circuit.
NMI#	15	I (CMOS)	Non maskable interrupt pin. This pin includes an pull-up resistor.
INT1#	14	I/O (CMOS)	In Free-run mode, this signal is input that is used as interrupt pin. Interrupt will be internally asserted also when data transfer done, or command end. In ICE-debugging mode, this signal is output and asserted when data transfer done, or command end. This pin includes an pull-up resistor.

Symbol	No.	Type	Description
HOLD#	16	I/O (CMOS)	In Free-run mode, this signal is input that is used as holding DSP clock down and release bus. Bus hold will be internally asserted also when upgrade mode enable. In ICE-debugging mode, this signal is output and asserted when upgrade mode enable. This pin includes an pull-up resistor.
HLDA#	73	I/O (CMOS)	In Free-run mode, this signal is output that is used as ack to HOLD# signal. This signal will be internally sent to PCMCIA/ATA interface also when upgrade mode enable. In ICE-debugging mode, this signal is input and ack to HOLD# when upgrade mode enable.
XF#/SCTRL#	74	O (CMOS)	Sleep control, this pin can be directly asserted to low while power down bit is set by DSP. This pin is connected to external RC circuit. Default inactive (Logic High). In ICE-debugging mode, this signal is used to reset DSP.

Flash Memory Interface

Symbol	No.	Type	Description
FA19/CLE	12	O (CMOS)	In linear mode, this signal is used as flash memory chip high address line 19. In series mode, this signal is used as flash memory chip command latch enable.
FA18/ALE/ ICEMODE	20	I/O (CMOS)	In linear mode, this signal is used as flash memory chip high address line 18. In series mode, this signal is used as flash memory chip address latch enable. This signal is also used to select whether the MX9691 initializes in Free-run mode or in ICE-debugging mode at power-on reset. If this pin go high, then the MX9691L will switch to Free-run mode at power-on reset, and if this pin remains low, then the MX9691L will initialize in ICE-debugging mode. This pin includes an internal pull-up resistor. ICE-debugging mode select : ICEMODE=1 → Free-run mode. ICEMODE=0 → ICE-debugging mode.
FA17/EROM	21	I/O(CMOS)	This signal is used as flash memory chip high address line 17. This signal is also used to select whether the firmware store in linear type flash memory array or in separate external ROM at power-on reset. If this pin go high, then the firmware will be executed in linear type flash memory array, and if this pin remains low, then the firmware will be executed in separate external ROM. Store firmware in external ROM or linear type Flash memory array select: EROM = 0 → Store in External ROM. EROM = 1 → Store in flash memory array. This pin includes an internal pull-up resistor.

Symbol	No.	Type	Description												
FA[16:15]/ ATADET[1:0]	1-2	I/O (CMOS)	<p>This signal is used as flash memory chip high address line 16-15. These signals are also used to select configuration in True IDE mode at power-on reset. ATADET1 is connected to DSP's IPT1. ATADET0 is connected to DSP's IPT0. VDD is connected to IPT2.</p> <p>Master/Slave selection in True IDE mode :</p> <table border="0"> <tr> <td>ATADET1</td> <td>ATADET0</td> <td>mode selected</td> </tr> <tr> <td>1</td> <td>1</td> <td>one drive</td> </tr> <tr> <td>0</td> <td>0</td> <td>master of two drives</td> </tr> <tr> <td>1</td> <td>0</td> <td>slave of two drives</td> </tr> </table> <p>This power-on configuration can be accessed from PCMCIA/ATA port 601Ch bit3-2. These pins include internal pull-up resistors.</p>	ATADET1	ATADET0	mode selected	1	1	one drive	0	0	master of two drives	1	0	slave of two drives
ATADET1	ATADET0	mode selected													
1	1	one drive													
0	0	master of two drives													
1	0	slave of two drives													
RDFLASH1#	54	O (CMOS)	<p>Flash memory output enable 1 for bank1: This signal will be asserted by flash memory read operation when flash memory read address latch, port 601Dh bit 8 = 1(i.e. FA23=1). Note: Flash memory access window is mapped to 32KW data and code space 8000h~ffffh.</p>												
RDFLASH0#	42	O (CMOS)	<p>Flash memory output enable 0 for bank0: This signal will be asserted by flash memory read operation when flash memory read address latch, port 601Dh bit 8 = 0(i.e. FA23=0).</p>												
WRFLASH1#	19	O (CMOS)	<p>Flash memory write enable 1 for bank1: This signal will be asserted by flash memory write operation when flash memory write address latch, port 601Fh bit 8 = 1(i.e. FA23=1).</p>												
WRFLASH0#	18	O (CMOS)	<p>Flash memory write enable 0 for bank0: This signal will be asserted by flash memory write operation when flash memory write address latch, port 601Fh bit 8 = 0(i.e. FA23=0).</p>												

Symbol	No.	Type	Description																																			
FCE[7:0]#	43-44,	O	Flash memory chip enable 7-0 :																																			
	46-47 49-52	(CMOS)	In linear mode, These signals are decoded from port 601Dh bit 7-5 when flash memory read or port 601Fh bit 7-5 when flash memory write. Decoding combination : <table style="margin-left: 40px; border-collapse: collapse;"> <tr> <td style="padding-right: 5px;">bit7</td> <td style="padding-right: 5px;">bit6</td> <td style="padding-right: 5px;">bit5</td> <td style="padding-left: 10px;">FCE[7:0]#</td> </tr> <tr> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">0</td> <td style="padding-left: 10px;">11111110</td> </tr> <tr> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">1</td> <td style="padding-left: 10px;">11111011</td> </tr> <tr> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">0</td> <td style="padding-left: 10px;">11101111</td> </tr> <tr> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">1</td> <td style="padding-left: 10px;">10111111</td> </tr> <tr> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">0</td> <td style="padding-left: 10px;">11111101</td> </tr> <tr> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">0</td> <td style="padding-right: 5px;">1</td> <td style="padding-left: 10px;">11110111</td> </tr> <tr> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">0</td> <td style="padding-left: 10px;">11011111</td> </tr> <tr> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">1</td> <td style="padding-right: 5px;">1</td> <td style="padding-left: 10px;">01111111</td> </tr> </table>	bit7	bit6	bit5	FCE[7:0]#	0	0	0	11111110	0	0	1	11111011	0	1	0	11101111	0	1	1	10111111	1	0	0	11111101	1	0	1	11110111	1	1	0	11011111	1	1	1
bit7	bit6	bit5	FCE[7:0]#																																			
0	0	0	11111110																																			
0	0	1	11111011																																			
0	1	0	11101111																																			
0	1	1	10111111																																			
1	0	0	11111101																																			
1	0	1	11110111																																			
1	1	0	11011111																																			
1	1	1	01111111																																			
PWD0#/WP#	32	O (CMOS)	In series mode, These are decoded from port 601Dh bit 7-5 only when port 601Eh bit 2 is set. In linear mode, this signal is used as deep power-down control of flash memory chips of bank0. PWD0# is active low and also locks out erase or program operation providing data protection during power transitions. Power down pin PWD0# will be active if FA23=1. In series mode, this signal is used to protect the device from inadvertent programming or erasing. WP# is active low.																																			
PWD1#/SE#	64	O (CMOS)	In linear mode, this signal is used as deep power-down control of flash memory chips of bank1. PWD1# is active low and also locks out erase or program operation providing data protection during power transitions. Power down pin PWD0# will be active if FA23=0. In series mode, this signal is used to spare area control. SE# is active low.																																			
FRY/FBY#	13	I (CMOS)	Flash memory Ready/busy input: This signal indicate the state of erase or program operation in flash memory chips. This pin includes an internal pull-up resistor.																																			

Control ROM interface

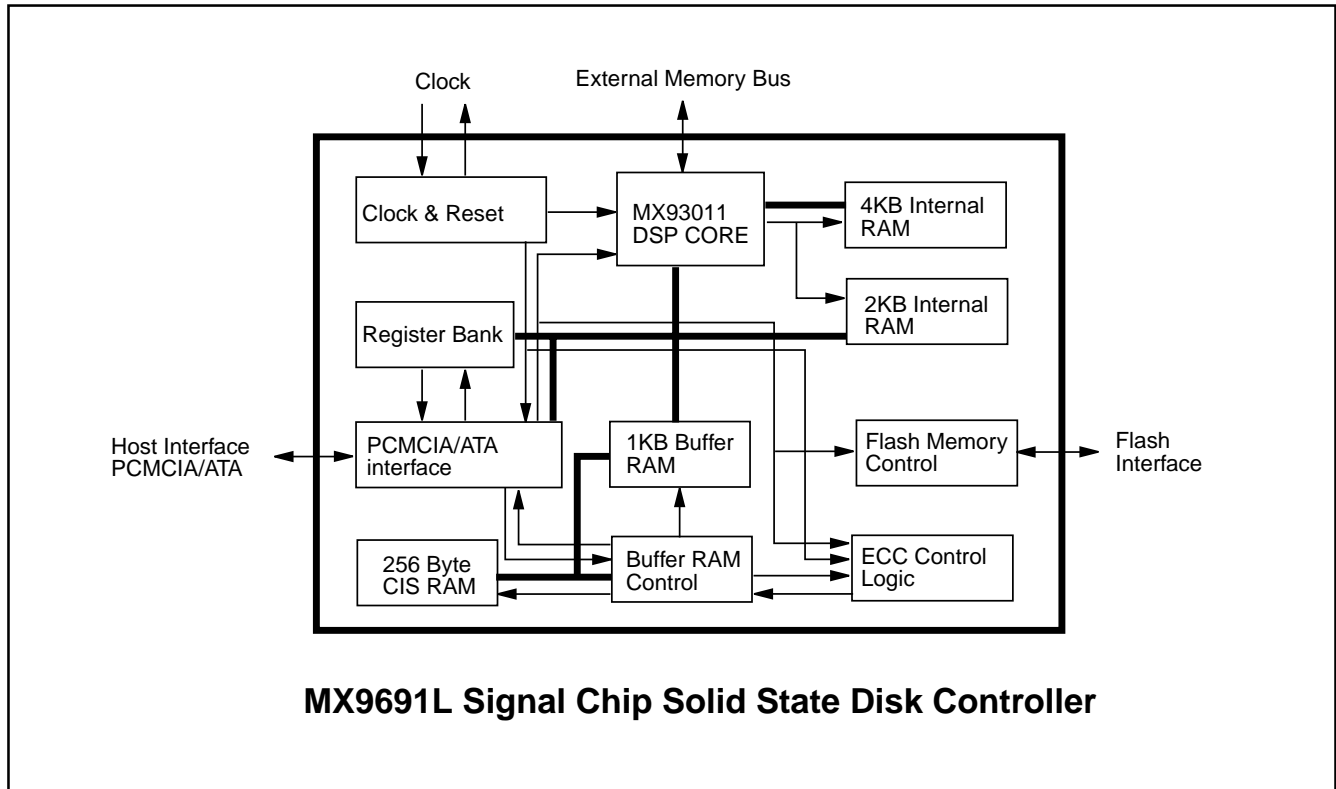
Symbol	No.	Type	Description
ROMCS#/ FWIN#	75	O (CMOS)	ROM chip select/Flash memory data buffer enable : In Free-run mode, this signal is used as ROM chip enable if firmware that stored in external ROM. In ICE-debugging mode, this signal is used as flash memory data buffer (74640) enable if firmware that stored in flash memory array.
ROMWR#/FDIR	76	O (CMOS)	ROM write enable/Flash memory data buffer direction control: In Free-run mode, this signal is used as ROM write enable if firmware that stored in external ROM. In ICE-debugging mode, this signal is used as flash memory data buffer (74640) direction control if firmware that stored in flash memory array.

Miscellaneous

Symbol	No.	Type	Description
X1	79	I	Crystal input.
X2	78	O	Crystal output.
SWAIT#	71	I(CMOS Schmitt)	Sleep wait, this pin is connected to external RC circuit.
N.C.	70	O	No connect.
TEST	81	I (CMOS)	This signal is used to select the main system clock, either from external clock source if this signal is high or from internal PLL circuit if this signal is low. This pin includes an internal pull-up resistor.
PWR_RST#	82	I(CMOS Schmitt)	Power on reset, CMOS Schmite-triggered: The MX9691L include debouncing circuit to stabilize internal DSP reset signal.
LED#	6	O (CMOS)	LED output: This signal is connected to external LED in debugging system to indicate system status. The LED will be turn-on during reset. The control firmware will turn off the LED after H/W initialization and pass diagnostics. If system fail, the control firmware will flash the LED to indicate some error occur. This signal will be high if port 601Ch bit0 set to 1 or OPTR bit2 set to 1.
VCC	17,45,53, 72,80,105, 112		5 or 3.3 volt Power pin
GND	7,25,38, 48,59,69, 77,91,108, 120		Ground pin

5. Functional and Operation Description

5-1. Block Diagram



5-2. System Memory Map

Data Space :

Address	Function & Usage
0000h~007fh	Internal RAM (128W) to store control variables
0080h~07ffh	Internal RAM(1920W) for flash memory algorithm usage
0800h~5fffh	User define (22kW)
6000h~63ffh	I/O range(1kW): ATA CTL. use I/O range (6000h~601fh)
6400h~6fffh	User define (3kW)
7000h~73ffh	User define (1kW)
7400h~77ffh	Internal RAM (1kW) for expansion RAM or shadow ROM space
7800h~7fffh	ROM Data space(2kW)
8000h~ffffh	Flash memory access windows(32kW)

Program Space :

Address	Function & Usage
0000h~77ffh	ROM program space (32kW)
7800h~7fffh	Unused
8000h~ffffh	Flash memory access windows(32kW)

5-3. Power-on detection

* Store firmware in external ROM or Flash memory array :

FA17/EROM = 0 → Store in External ROM
 FA17/EROM = 1 → Store in flash memory array

* Master/Slave selection in True IDE mode :

FA16/ATADET1	FA15/ATADET0	mode selected
1	1	one drive
0	0	master of two drives
1	0	slave of two drives

Note : For some customers design the master/slave selection is selected by only one jumper that may be FA16 or FA15. It need to change firmware only.

* ICE debugging mode select :

FA18/ICEMDOE = 0 ---> ICE-debugging mode
 FA18/ICEMODE = 1---> Free-run mode, DSP fetch code from external memory bus and execute it.

* Flash memory data buffer control

ROMCS# is replaced by FWIN# if ICE-debugging mode & firmware in linear type flash memory array.
 ROMWR# is replaced by FDIR if ICE-debugging mode & firmware in linear type flash memory array.

* PCMCIA mode or True IDE mode select

HOE#	Mode
0	True IDE mode
1	PCMCIA mode

To enable True IDE mode this input should be grounded by the host.

5-4. Decoding Configuration of all registers in Host interface
*** Common Momory Mode Decode**

Register Address						Register Read Enable	Register Write Enable
CE1#	CE2#	REG#	HA10	HA9:4	HA3:0	HOE# =0	HWE# = 0
0	0	1	0	xh	000xb	Read Data Register HD[15:0]	Write Data Register HD[15:0]
0	1	1	0	xh	0000b	Read Data HD[7:0] Even & Odd byte	Write Data HD[7:0] Even & Odd byte
1	0	1	0	xh	0000b	Error Status HD[15:8]	Features HD[15:8]
0	1	1	0	xh	0001b	Error Status HD[7:0]	Features HD[7:0]
1	0	1	0	xh	0001b	Error Status HD[15:8]	Features HD[15:8]
0	0	1	0	xh	001xb	Sector Count HD[7:0] Sector Number HD[15:8]	Sector Count HD[7:0] Sector Number HD[15:8]
0	1	1	0	xh	0010b	Sector Count HD[7:0]	Sector Count HD[7:0]
0	1	1	0	xh	0011b	Sector Number HD[7:0]	Sector Number HD[7:0]
1	0	1	0	xh	0011b	Sector Number HD[15:8]	Sector Number HD[15:8]
0	0	1	0	xh	010xb	Cyl. Low HD[7:0] Cly. High HD[15:8]	Cyl. Low HD[7:0] Cly. High HD[15:8]
0	1	1	0	xh	0100b	Cyl. Low HD[7:0]	Cyl. Low HD[7:0]
0	1	1	0	xh	0101b	Cly. High HD[7:0]	Cly. High HD[7:0]
1	0	1	0	xh	0101b	Cly. High HD[15:8]	Cly. High HD[15:8]
0	0	1	0	xh	011xb	Drive/Head HD[7:0] Ctl. Status HD[15:8]	Drive/Head HD[7:0] Command HD[15:8]
0	1	1	0	xh	0110b	Drive/Head HD[7:0]	Drive/Head HD[7:0]
0	1	1	0	xh	0111b	Ctl. Status HD[7:0]	Command HD[7:0]
1	0	1	0	xh	0111b	Ctl. Status HD[15:8]	Command HD[15:8]
0	0	1	0	xh	100xb	Read Data Register HD[15:0] (Duplicate)	Write Data Register HD[15:0] (Duplicate)
0	1	1	0	xh	1000b	Read Data HD[7:0] Even & Odd byte (Duplicate)	Write Data HD[7:0] Even & Odd byte (Duplicate)
1	0	1	0	xh	1001b	Read Data HD[15:8] Odd byte (Duplicate)	Write Data HD[15:8] Odd byte (Duplicate)
0	1	1	0	xh	1001b	Read Data HD[7:0] Odd byte (Duplicate)	Write Data HD[7:0] Odd byte (Duplicate)
0	0	1	0	xh	110xb	Undefined HD[7:0] Error Status HD[15:8] (Duplicate)	Undefined HD[7:0] Features HD[15:8] (Duplicate)
0	1	1	0	xh	1101b	Error Status HD[7:0] (Duplicate)	Features HD[7:0] (Duplicate)
0	0	1	0	xh	111xb	Alternate Ctl. Status HD[7:0] Drive/Head HD[15:8]	Device Ctl. HD[7:0] Undefined HD[15:8]
0	1	1	0	xh	1110b	Alternate Ctl. Status HD[7:0]	Device Ctl. HD[7:0]



Register Address						Register Read Enable	Register Write Enable
0	1	1	0	xh	1111b	Drive/Head HD[7:0]	Not Used
1	0	1	0	xh	1111b	Drive/Head HD[15:8]	Not Used
0	0	1	1	xh	xxxxb	Read Data Register HD[15:0]	Write Data Register HD[15:0]
0	1	1	1	xh	xxx0b	Read Data HD[7:0] Even & Odd byte	Write Data HD[7:0] Even & Odd byte
0	1	1	1	xh	xxx1b	Read Data HD[7:0]Odd byte	Write Data HD[7:0]Odd byte
1	0	1	1	xh	xxx0b	Read Data HD[15:8] Odd byte	Write Data HD[15:8] Odd byte
1	0	1	1	xh	xxx1b	Read Data HD[15:8] Odd byte	Write Data HD[15:8] Odd byte

*** Independent I/O Mode Decode**

Register Address					Register Read Enable	Register Write Enable
CE1#	CE2#	REG#	HA9:4	HA3:0	IOR# =0	IOW# = 0
0	0	0	xh	0000b	Read Data Register HD[15:0]	Write Data Register HD[15:0]
0	1	0	xh	0000b	Read Data HD[7:0] Even & Odd byte	Write Data HD[7:0] Even & Odd byte
1	0	0	xh	0000b	Error Status HD[15:8]	Features HD[15:8]
0	1	0	xh	0001b	Error Status HD[7:0]	Features HD[7:0]
1	0	0	xh	0001b	Error Status HD[15:8]	Features HD[15:8]
0	1	0	xh	0010b	Sector Count HD[7:0]	Sector Count HD[7:0]
0	1	0	xh	0011b	Sector Number HD[7:0]	Sector Number HD[7:0]
1	0	0	xh	0011b	Sector Number HD[15:8]	Sector Number HD[15:8]
0	1	0	xh	0100b	Cyl. Low HD[7:0]	Cyl. Low HD[7:0]
0	1	0	xh	0101b	Cly. High HD[7:0]	Cly. High HD[7:0]
1	0	0	xh	0101b	Cly. High HD[15:8]	Cly. High HD[15:8]
0	1	0	xh	0110b	Drive/Head HD[7:0]	Drive/Head HD[7:0]
0	1	0	xh	0111b	Ctl. Status HD[7:0]	Command HD[7:0]
1	0	0	xh	0111b	Ctl. Status HD[15:8]	Command HD[15:8]
0	0	0	xh	1000b	Read Data Register HD[15:0](Duplicate)	Write Data Register HD[15:0](Duplicate)
0	1	0	xh	1000b	Read Data HD[7:0] Even & Odd byte (Duplicate)	Write Data HD[7:0] Even & Odd byte (Duplicate)
1	0	0	xh	1001b	Read Data HD[15:8] Odd byte (Duplicate)	Write Data HD[15:8] Odd byte (Duplicate)
0	1	0	xh	1001b	Read Data HD[7:0] Odd byte (Duplicate)	Write Data HD[7:0] Odd byte (Duplicate)
0	1	0	xh	1101b	Error Status HD[7:0](Duplicate)	Features HD[7:0](Duplicate)
0	1	0	xh	1110b	Alternate Ctl. Status HD[7:0]	Device Ctl. HD[7:0]
0	1	0	xh	1111b	Drive/Head HD[7:0]	Not Used
1	0	0	xh	1111b	Drive/Head HD[15:8]	Not Used



* Primary ATA Mode Decode

Register Address				Register Read Enable	Register Write Enable
CE1#	CE2#	REG#	HA9:0	IOR# =0	IOW# = 0
0	0	0	1F0h	Read Data Register HD[15:0]	Write Data Register HD[15:0]
0	1	0	1F0h	Read Data HD[7:0]Even & Odd byte	Write Data HD[7:0]Even & Odd byte
1	0	0	1F0h	Error Status HD[15:8]	Features HD[15:8]
0	1	0	1F1h	Error Status HD[7:0]	Features HD[7:0]
1	0	0	1F1h	Error Status HD[15:8]	Features HD[15:8]
0	1	0	1F2h	Sector Count HD[7:0]	Sector Count HD[7:0]
0	1	0	1F3h	Sector Number HD[7:0]	Sector Number HD[7:0]
1	0	0	1F3h	Sector Number HD[15:8]	Sector Number HD[15:8]
0	1	0	1F4h	Cyl. Low HD[7:0]	Cyl. Low HD[7:0]
0	1	0	1F5h	Cly. High HD[7:0]	Cly. High HD[7:0]
1	0	0	1F5h	Cly. High HD[15:8]	Cly. High HD[15:8]
0	1	0	1F6h	Drive/Head HD[7:0]	Drive/Head HD[7:0]
0	1	0	1F7h	Ctl. Status HD[7:0]	Command HD[7:0]
1	0	0	1F7h	Ctl. Status HD[15:8]	Command HD[15:8]
0	1	0	3F6h	Alternate Ctl. Status HD[7:0]	Device Ctl. HD[7:0]
0	1	0	3F7h	Drive/Head HD[7:0]	Not Used
1	0	0	3F7h	Drive/Head HD[15:8]	Not Used

* Secondary ATA Mode Decode

Register Address				Register Read Enable	Register Write Enable
CE1#	CE2#	REG#	HA9:0	IOR# =0	IOW# = 0
0	0	0	170h	Read Data Register HD[15:0]	Write Data Register HD[15:0]
0	1	0	170h	Read Data HD[7:0]Even & Odd byte	Write Data HD[7:0]Even & Odd byte
1	0	0	170h	Error Status HD[15:8]	Features HD[15:8]
0	1	0	171h	Error Status HD[7:0]	Features HD[7:0]
1	0	0	171h	Error Status HD[15:8]	Features HD[15:8]
0	1	0	172h	Sector Count HD[7:0]	Sector Count HD[7:0]
0	1	0	173h	Sector Number HD[7:0]	Sector Number HD[7:0]
1	0	0	173h	Sector Number HD[15:8]	Sector Number HD[15:8]
0	1	0	174h	Cyl. Low HD[7:0]	Cyl. Low HD[7:0]
0	1	0	175h	Cly. High HD[7:0]	Cly. High HD[7:0]
1	0	0	175h	Cly. High HD[15:8]	Cly. High HD[15:8]
0	1	0	176h	Drive/Head HD[7:0]	Drive/Head HD[7:0]
0	1	0	177h	Ctl. Status HD[7:0]	Command HD[7:0]
1	0	0	177h	Ctl. Status HD[15:8]	Command HD[15:8]
0	1	0	376h	Alternate Ctl. Status HD[7:0]	Device Ctl. HD[7:0]
0	1	0	377h	Drive/Head HD[7:0]	Not Used
1	0	0	377h	Drive/Head HD[15:8]	Not Used

5-5. Automatic Power Saving Mode

There are four power saving modes defined in solid state disk(SSD) system. These four power saving modes are executed by firmware which use DSP's soft-hold and power down function and addition logic circuit to implement it.

Active mode : In Active mode the SSD is capable of execution to file read and write operation.

Idle mode : In Idle mode the SSD polls the events that include `command_in` or `time_out` events. If read/write command is asserted then the SSD will enter the Active mode.

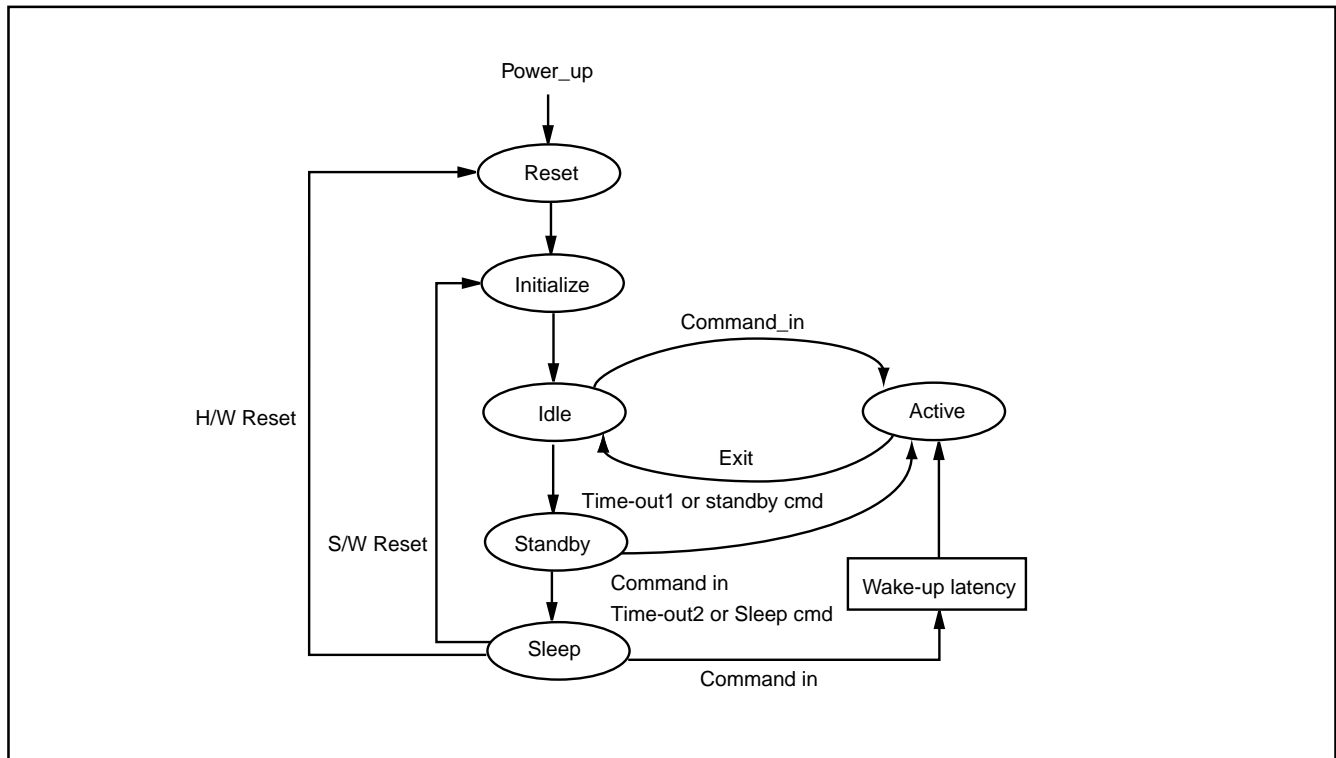
Standby mode : The SSD will enter the Standby mode after `time_out`(1.25ms) event occurs or standby command is asserted. The SSD controller MX9691L will enter `soft_hold` condition. The MX9619 will stop program execution and shut off most circuit activities to save many

power consumption. The MX9691L will automatically wake up and enter the Active mode if any command is asserted.

Sleep mode : The SSD will enter the Sleep mode after sleep command is asserted. This is most power saving mode. The SSD controller MX9691L will enter `soft_hold` condition and stop main clock and then the all system activities will stop. This mode can be waked up by H/W reset, S/W reset or ATA command asserted. The H/W reset will reset all h/w circuits and the Host must reconfigure the SSD before any command is asserted. The S/W reset will set the busy status until the SSD is ready for accepting command, the Host don't need any h/w reinitialization. The duration of H/W and S/W reset must keep enough for main clock stabilization.

The ATA command asserted to wake-up latency need the external RC circuit delay for clock stabilization while the Solid State Disk(SSD) had entered sleep mode.

Power Saving Flow



5-6. Registers definition*** Registers List**

Type of Register	Location
PCMCIA/ATA Interface	6000h, 6001h, 6002h, 6003h, 6004h, 6005h, 6006h, 6007h, 600Bh, 6010h, 6011h, 6012h, 6013h, 6019h, 601Ah, 601Bh, 601Ch
PC INTERRUPT CONTROL	6009h, 600Ah
BUFFER MANAGER AND DMA	6008h, 6014h, 6015h, 6016h, 6017h, 6018h
ECC Control	600Ch, 600Dh, 600Eh, 600Fh
Flash Memory Interface	601Dh, 601Eh, 601Fh

*** Register Description**

Port 6000h :

Bit	Function Description
	AT CONTROL/STATUS REGISTER Default reset value : 01h
7	R/W: DRIVE READY (drive 0)
6	R/W: DRIVE SEEK COMPLETE (drive 0)
5	R/W: CORRECTED DATA
4	R: ATA INT. ENABLE
3	R: AT SOFTWARE RESET
2	R/W: HOST INTERRUPT
1	R/W: ERROR BIT
0	R/W: BUSY BIT

Port 6001h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: ERROR REGISTER (map to command block 1f1h)

Port 6002h :

Bit	Function Description
	Default reset value : 01h
7:0	R/W: SECTOR COUNT REGISTER (map to command block 1f2h)

Port 6003h :

Bit	Function Description
	Default reset value : 01h
7:0	R/W: SECTOR NUMBER REGISTER (map to command block 1f3h)

Port 6004h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: CYCLINDER LOW REGISTER (map to command block 1f4h)

Port 6005h :

Bit	Function Description
	Default reset value : 00h
7:0	R/W: CYCLINDER HIGH REGISTER (map to command block 1f5h)

Port 6006h :

Bit	Function Description
	Default reset value : A0h
7:0	R/W: DRIVE/HEAD REGISTER (map to command block 1f6h)

Port 6007h :

Bit	Function Description
	Default reset value : 00h
7:0	R: COMMAND REGISTER (map to command block 1f7h)

Port 6008h :

Bit	Function Description
	BUFFER RAM SIZE CONTROL REGISTER
	Default reset value : 40h
7	R/W: TEST MODE 1 for HAP/DAP test 0 : DISABLE 1 : ENABLE
6	R/W: BIT WRITE GATE STATE OF DRIVE 0 : ENABLE 1 : DISABLE
5	R: PCMCIA or True IDE mode 0 : True IDE mode 1 : PCMCIA mode
4	R/W: Auto DAP increment 0 : Disable 1 : Enable
3	R/W: Shadow ROM control 0 : Disable 1 : Enable
2:0	R/W: BUFFER RAM SIZE CONTROL 00x : 32KW 010 : 16KW 011 : 8KW 100 : 4KW 101 : 2KW 110 : 1KW

111 : 512W

Port 6009h :

Bit	Function Description
	HOST INTERRUPT STATUS Default reset value : 00h
7	R: Power-Down timer time-out detected
6	R: Card configuration register write detected
5	R: CIS accessed detected
4	R: Hreset detected
3	R: PC SRST(or PCMCIA SRST) DETECTED
2	R: PC STATUS READ DETECTED
1	R: PC SELECTION
0	R: PC TRANSFER DONE

Port 600Ah :

Bit	Function Description
	HOST INTERRUPT ENABLE Default reset value : 00h
7	R/W: Power-Down timer time-out detected enable.
6	R/W: Card configuration register write detected enable
5	R/W: CIS accessed detected enable
4	R/W: Hreset detected enable
3	R/W: PC SRST(PCMCIA SRST) DETECTED ENABLE
2	R/W: PC STATUS READ DETECTED ENABLE
1	R/W: PC SELECTION ENABLE
0	R/W: PC TRANSFER DONE ENABLE

Port 600Bh :

Bit	Function Description
	Default reset value : 00h
7:0	R: Feature register (map to command block 1f1h)

Port 600Ch :

Bit	Function Description
	ECC CONTROL REGISTER Default reset value : 00h
7	R/W: ECC FUNCTION SUSPEND 0 : NORMAL 1 : SUSPEND
6	R/W: CORRECTION SPEED SELECT 0 : FULL SPEED (Max. Clock frequency) 1 : HALF SPEED (1/2 Max. Clock frequency)
5	R/W: ENCODE/DECODE FUNCTION SELECTION 0 : ENCODE 1 : DECODE
4	R/W: RESET ECC CIRCUIT 0 : RESET 1 : NORMAL
3	R: UNCORRECTABLE ERROR FLAG
2	R: CORRECTABLE ERROR FLAG
1	R: CORRECTION DONE FLAG
0	R/W: START ECC CORRECT FUNCTION ENABLE/DISABLE 0 : DISABLE 1 : ENABLE

Port 600Dh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 0 REGISTER

Port 600Eh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 1 REGISTER

Port 600Fh :

Bit	Function Description
	Default reset value : 0000h
15:0	R/W : ECC 2 REGISTER

Port 6010h :

Bit	Function Description
	Default reset value : 00h

7:0 R: Configuration Option register (map to attribute memory 200h)

Port 6011h :

Bit Function Description

Default reset value : 00h

7:0 R: Card Configuration and status register (map to attribute memory 202h)

Port 6012h :

Bit Function Description

Default reset value : 0Ch

7:0 R: Pin replacement register (map to attribute memory 204h)

Port 6013h :

Bit Function Description

Default reset value : 00h

7:0 R: Socket and copy register (map to attribute memory 206h)

Port 6014h :

Bit Function Description

Default reset value : 0000h

15:0 R/W : HOST ADDRESS POINTER

Port 6015h :

Bit Function Description

Default reset value : 00ffh

15:0 R/W : AT STOP POINTER

Port 6016h :

Bit Function Description

Default reset value : 0000h

15:0 R/W : DISK ADDRESS POINTER

Port 6017h :

Bit Function Description

DMA CONTROL REGISTER

Default reset value : 08h

7 R/W: DRIVE READY (drive 1)

6 R/W: DRIVE SEEK COMPLETE (drive 1)

5 R/W: set BSY upon XFER done

0 : DISABLE

1 : ENABLE

4 R/W: ENABLE AUTO INTERRUPTS - AT ONLY

0 : DISABLE

1 : ENABLE

Port6017h:

Bit	Function Description
3	R/W: BUFFER RAM CHIP ENABLE 0 : ENABLE 1 : DISABLE
2	R/W: HOST BUS DIRECTION 0 : START BUFFER ---> AT BUS 1 : START AT BUS ---> BUFFER WHEN SET
1	R: A COMPLETION OF AT DMA XFER
0	R/W: START DATA TRANSFER BETWEEN AT BUS AND BUFFER RAM 0 : DISABLE 1 : ENABLE

Port 6018h :

Bit	Function Description
15:0	R/W : ACCESS PORT INTO BUFFER RAM

Port 6019h :

Bit	Function Description
	PCMCIA control register
7	R: True IDE mode
6	R: Common memory mode
5	R: I/O mode
4	R/W: host ready
3	R/W: no drive address
2	R/W: Internal registers write pulse width 0 : 2 system clock 1 : 1 system clock
1	R/W: Reserved.

0 R/W: Reserved.

Port 601Ah :

Bit	Function Description
	Auxi_ctl_1 reg. Default reset value : 00h
7	R/W : DASP
6	R/W : Host Interrupt level mode or pulse mode select 0: Level mode 1: Pulse mode
5	R/W : PDIAG
4	R/W : DASP output enable
3	R/W: write protect enable 0: Disable 1: Enable
2	R/W: PDIAG output enable
1	R/W: master/slave mode enable 0: Disable 1: Enable
0	R/W: master/salve of True IDE mode 0: master 1: slave

Port 601Bh :

Bit	Function Description
	Auxi_ctl_2 reg. Default reset value : 00h
7:4	Reserved.
3	R/W: Reserved.
2	R/W: Deep power down control for automatic wake-up function from sleep mode. 0 : Disable 1 : Enable
1	R/W: Reserved.
0	R/W: Disk interrupt polarity 0: Low active

1: High active

Port 601Ch :

Bit	Function Description
	Auxi_ctl_3 reg. Default reset value : 0000h
15	Reserved.
14	R/W : Test mode 2 for timer 0 : Normal mode 1 : Test mode enable
13	R : DRQ
12	R : Time out status 1 : Time out event occurrence
11	R/W: Timer enable/disable 0 : Disable 1 : Enable
10:9	R/W: Power-down timer time-out select for 25MHz main clock 00 : 16 x 1.28 = 20.48 sec. 01 : 8 x 1.28 = 10.24 sec. 10 : 4 x 1.28 = 5.12 sec. 11 : 2 x 1.28 = 2.56 sec.
8	R : ICE-debugging mode detected 0 : ICE-debugging mode 1 : Free-run mode.
7	R/W : Inverted data bus for access flash memory. 0 : Inverted. 1 : Non-inverted.
6	R: External ROM detect. 0: Firmware stored in external ROM. 1: Firmware stored in linear type flash memory array.
5:4	R/W: Shadow ROM space control 00 : 512 bytes, Range: 7400h ~ 74ffh 01 : 1Kbytes, Range: 7400h ~ 75ffh 10 : 1.5Kbytes, Range: 7400h ~ 76ffh 11 : 2Kbytes, Range: 7400h ~ 77ffh
3:2	R : Master/Slave mode detect in True IDE mode 00 : Master of two drives 10 : Slave of two drives 11 : One drive
1	R/W: PIO/DMA mode select 0: PIO mode.

1: DMA mode.

0 R/W: LED output

Port 601Dh :

Bit	Function Description
-----	----------------------

Default reset value : 0000h

9:0 R/W : Flash memory Read address FA[24:15] latch in linear mode When data space 8000h ~ ffffh is read, the output of the flash memory read address latch will be used.

The definitions for this register in series mode

Default reset value : 0000h

9 Reserved.

8 Bank select in capacity extension mode

0 : Bank0 selected.

1 : Bank1 selected.

7:5 R/W: FCE select for series mode

000: FCE0

001: FCE2

010: FCE4

011: FCE6

100: FCE1

101: FCE3

110: FCE5

111: FCE7

4 R/W: Command latch enable (FA19/CLE)

0 : Disable

1 : Enable

3 R/W: Address latch enable (FA18/ALE)

0 : Disable

1 : Enable

2:0 Reserved

Port 601Eh :

Bit	Function Description
-----	----------------------

Flash memory control register

Default reset value : 08Ah

7 R/W: Flash memory deep power down control 0 in linear mode or Write protect in series mode

0 : Enable

1 : Disable

6 R : Ready / Busy status

0 : BUSY
1 : READY

Port 601Eh :

Bit	Function Description
5:4	R/W: Flash memory type select 00 : Reserved. 01 : 16M flash memory /Bank 1 select in linear mode or capacity extension mode selected in series mode. 10 : Reserved 11 : Reserved
3	R/W: Flash memory deep power down control 1 in linear mode or Spare area enable in series mode. 0 : Enable 1 : Disable
2	R/W: CE# enable for series mode 0 : Disable 1 : Enable
1	R/W: Series or linear mode select 0 : linear mode 1 : Series mode
0	R/W: Flash memory write pulse width control 0 : 1 system clock 1 : 2 system clock

Port 601Fh :

Bit	Function Description
9	Default reset value : 0000h R/W : Flash memory Write address FA[24:15] latch in linear mode When data space 8000h ~ ffffh is write or program space 8000h ~ ffffh is read, the output of the flash memory write address latch will be used. The definitions for this register in series mode Reserved.
8	Bank select in capacity extension mode 0 : Bank0 selected. 1 : Bank1 selected.
7:0	Reserved.

6. ELECTRICAL SPECIFICATIONS
6-1. DC Characteristics 1 : Ta = 0 °C to 70 °C, VCC = 5V±10%

Symbol	Parameter	Min	Max	Units	Conditions
VCC	Power Supply voltage	4.5	5.5	V	
VIL1	Input Low voltage (TTL)		0.8	V	VCC=5V
VIH1	Input High voltage (TTL)	2.0		V	VCC=5V
VIL2	Input Low voltage (CMOS)		1.2	V	VCC=5V
VIH2	Input High voltage (CMOS)	3.5		V	VCC=5V
VOL	Output Low voltage		0.4	V	IOL=8mA
VOH	Output High voltage	2.5		V	IOH=-8mA
ICC1	Supply Current 1		40	mA	f=25Mhz, Active mode, CL=0pf, VCC=5.5Volt, Temperature= 0°C
ICC2	Supply Current 2		30	mA	f = 25Mhz, Idle mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
ICC3	Supply Current 3		12	mA	f = 25Mhz, Standby mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
ICC4	Supply Current 4		1	mA	f = 0Mhz, Sleep mode, CL = 0pf, VCC=5.5Volt, Temperature= 0°C
IL	Input Leakage		±10	uA	0 < VIN < VCC
CIN	Input Capacitance		14	pf	VIN=0V
COUT	Output Capacitance		16	pf	VOUT=0V

Note : During transitions, inputs may undershoot to -2.0V for periods less than 20ns and overshoot to VCC + 2.0V for periods less than 20ns.

6-2. DC Characteristics 2 : Ta = 0 °C to 70 °C, VCC = 3.3V±5%

Symbol	Parameter	Min	Max	Units	Conditions
VCC	Power Supply voltage	3.1	3.5	V	
VIL1	Input Low voltage(TTL)		0.8	V	VCC=3.3V
VIH1	Input High voltage(TTL)	2.0		V	VCC=3.3V
VIL2	Input Low voltage(CMOS)		0.9	V	VCC=3.3V
VIH2	Input High voltage(CMOS)	2.7		V	VCC=3.3V
VOL	Output Low voltage		0.4	V	IOL=4mA
VOH	Output High voltage	2.2		V	IOH=-4mA
ICC1	Supply Current 1		20	mA	f=16Mhz, Active mode, CL=0pf, VCC=3.5Volt, Temperature= 0°C
ICC2	Supply Current 2		15	mA	f = 16Mhz, Idle mode, CL = 0pf, CC=3.5Volt, Temperature= 0°C
ICC3	Supply Current 3		5	mA	f = 16Mhz, Standby mode, CL = 0pf, VCC=3.5Volt, Temperature= 0°C
ICC4	Supply Current 4		0.5	mA	f = 0Mhz, Sleep mode, CL = 0pf, VCC=3.5Volt, Temperature= 0°C
IL	Input Leakage		±10	uA	0 < VIN < VCC
CIN	Input Capacitance		14	pf	VIN=0V
COUT	Output Capacitance		16	pf	VOUT=0V

Note : During transitions, inputs may undershoot to -2.0V for periods less than 20ns and overshoot to VCC + 2.0V for periods less than 20ns.

6-3. AC Characteristics

Condition : Ta=0°C to 70 °C, VCC = 5V±10% or VCC = 3.3V±5%

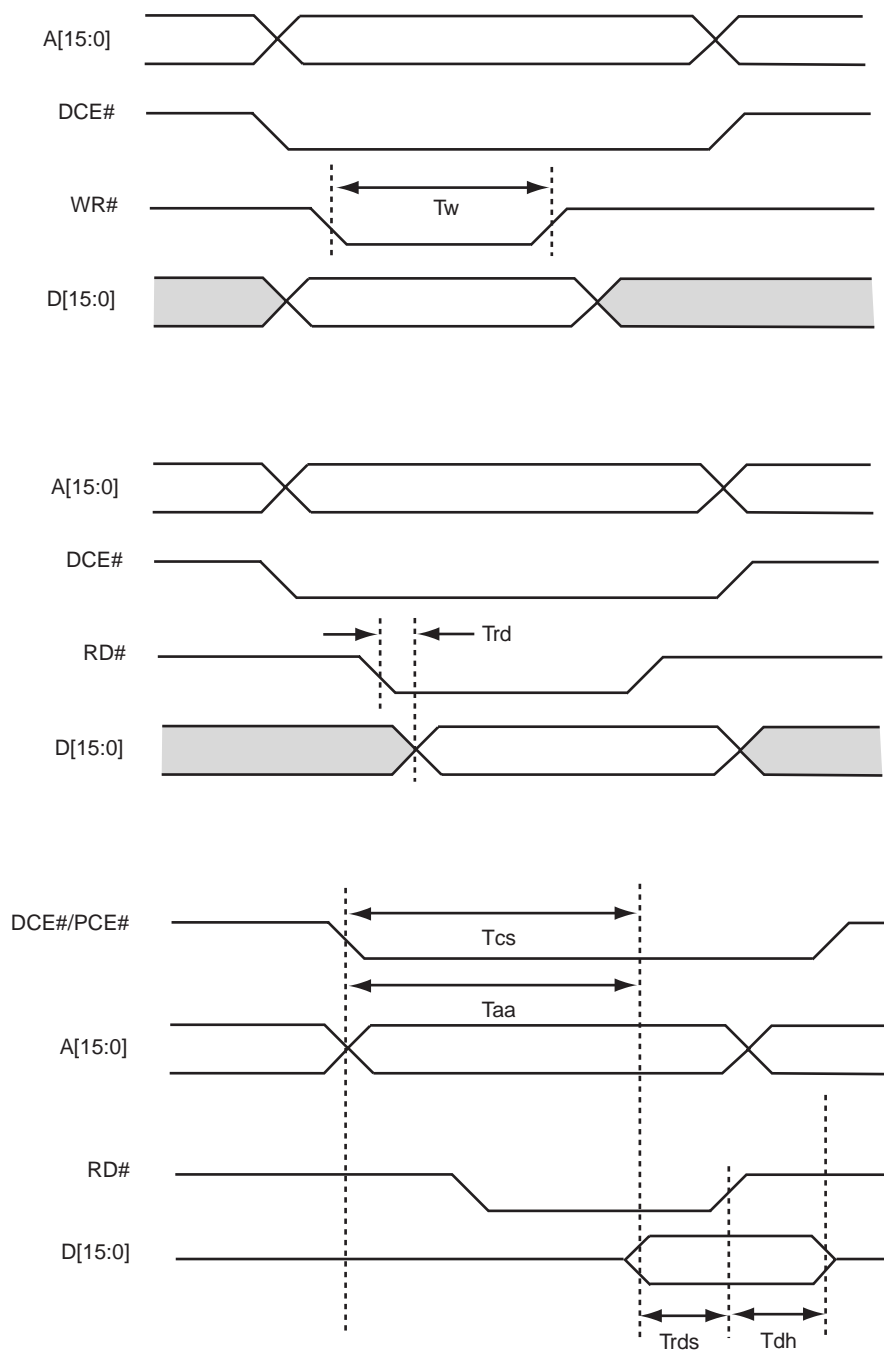
(1). DSP Interface Timing :

VCC = 5V±10%

Symbol	Description	Min.	Typ.	Max.	Units
Tw	In ICE mode, WR# pulse duration when the data are accessed by external DSP.	4Tc			
Trd	In ICE mode, RD# to output delay when the data are accessed by external DSP.			34	ns
Tcs	Chip select access cycle	1.5Tc		4.5Tc	ns
Taa	Address access cycle	1.5Tc		4.5Tc	ns
Trds	Data setup time before RD# high	12			ns
Tdh	Data hold time after RD# high	0			ns

VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Units
Tw	In ICE mode, WR# pulse duration when the data are accessed by external DSP.	4Tc			
Trd	In ICE mode, RD# to output delay when the data are accessed by external DSP.			34	ns
Tcs	Chip select access cycle	1.5Tc		4.5Tc	ns
Taa	Address access cycle	1.5Tc		4.5Tc	ns
Trds	Data setup time before RD# high				ns
Tdh	Data hold time after RD# high				ns



(2). Power Reset Timing
 $VCC = 5V \pm 10\%$ or $VCC = 3.3V \pm 5\%$

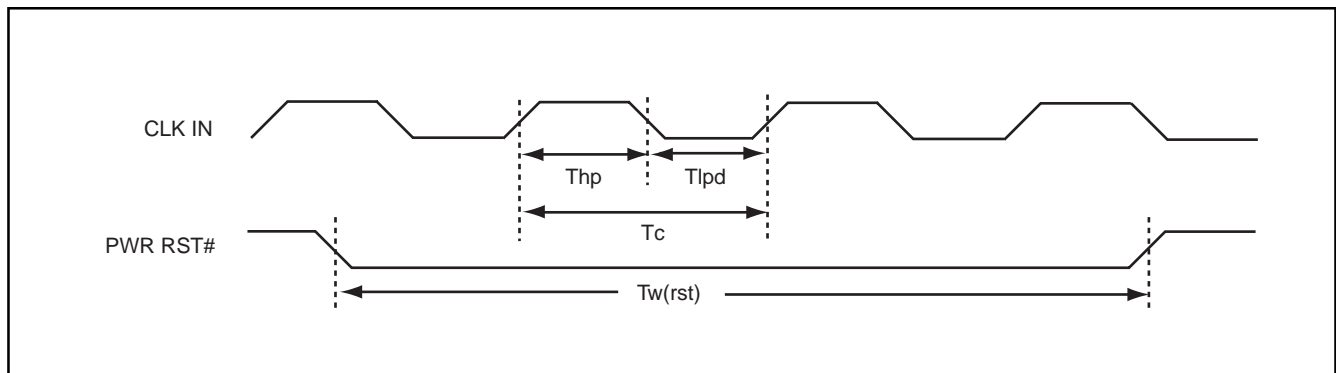
Symbol	Description	Min.	Typ.	Max.	Units
$T_{w(rst)}$	Reset low pulse width	$3T_c$			ns

(3). Clock Timing
 $VCC = 5V \pm 10\%$

Symbol	Description	Min.	Typ.	Max.	Units
$T_{c(c)}$	Clock cycle time	40			ns
$T_{lpd(c)}$	Clock low pulse duration($T_c=40ns$)	16		24	ns
$T_{hpd(c)}$	Clock high pulse duration($T_c=40ns$)	16		24	ns

 $VCC = 3.3V \pm 5\%$

Symbol	Description	Min.	Typ.	Max.	Units
$T_{c(c)}$	Clock cycle time	62.5			ns
$T_{lpd(c)}$	Clock low pulse duration($T_c=62.5ns$)	25		37.5	ns
$T_{hpd(c)}$	Clock high pulse duration($T_c=62.5ns$)	25		37.5	ns



(4). Interrupt Timing

VCC = 5V±10%

Symbol	Description	Min.	Typ.	Max.	Units
Tw	INT1# low pulse duration	1.5Tc			ns
Tf	INT1# fall time			10	ns

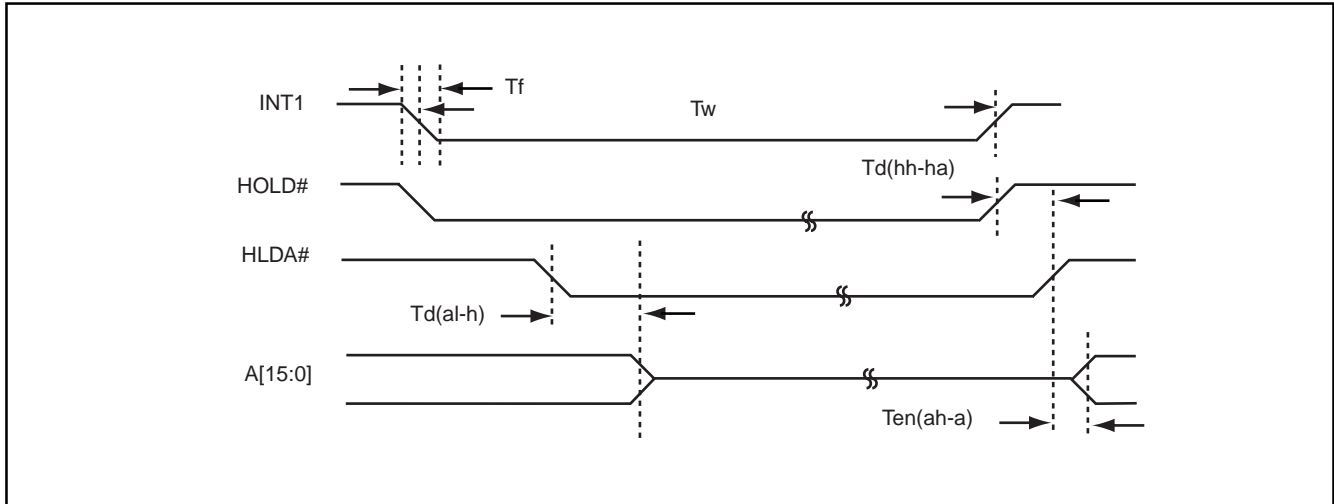
VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Units
Tw	INT1# low pulse duration	1.5Tc			ns
Tf	INT1# fall time				ns

(5). HOLD# Timing

VCC = 5V±10% or VCC = 3.3V±5%

Symbol	Description	Min.	Typ.	Max.	Units
Td(al-h)	HLDA# low to address tri-state	0			ns
Td(hh-ha)	HOLD# high to HLDA# high	0	0.5Tc	0.5Tc+10	ns
Ten(ah-a)	Address driven after HLDA# high	0.5Tc-10	0.5Tc	Tc	ns



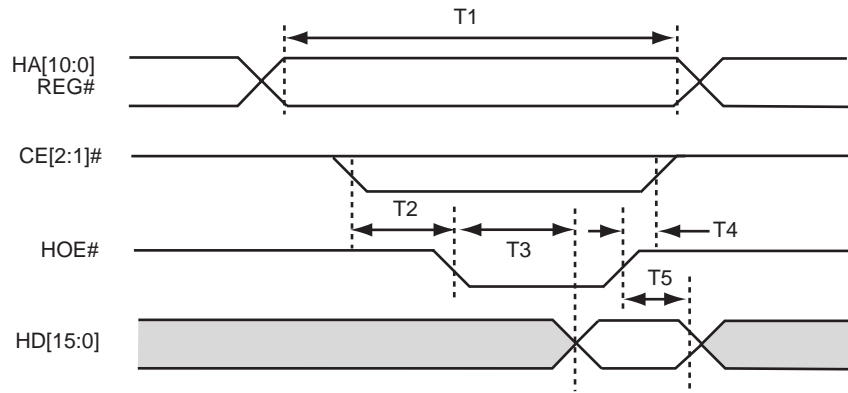
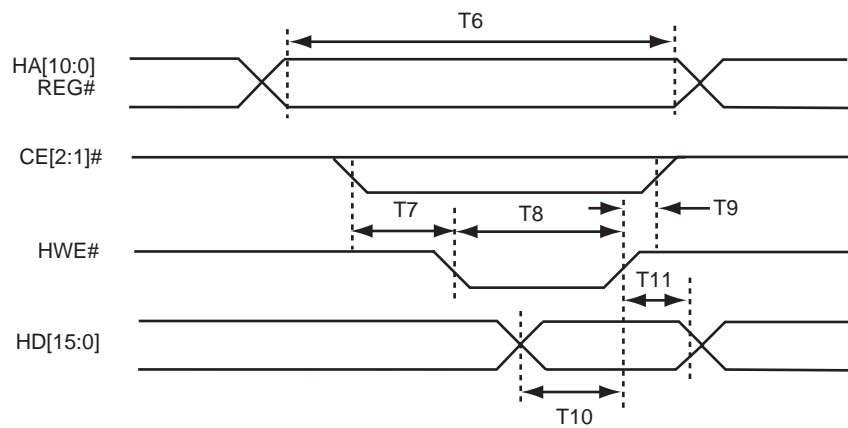
(6). PCMCIA Bus Timing 1: Common Memory and Attribute memory Access Timing

VCC = 5V±10%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Read cycle time	60	
T2	Chip enable setup time before output enable	0	
T3	Output data enable time from HOE#		31
T4	Chip disable hold time following output disable	1.5	
T5	Output data disable time following HOE#		10.5
T6	Write cycle time	60	
T7	Chip enable setup time before HWE#	0	
T8	Write pulse width of HWE#	40	
T9	Chip disable hold time following write disable	2	
T10	Data setup time before HWE#	0	
T11	Data hold time following HWE#	2.5	

VCC = 3.3V±5%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Read cycle time	90	
T2	Chip enable setup time before output enable	0	
T3	Output data enable time from HOE#		47
T4	Chip disable hold time following output disable	3	
T5	Output data disable time following HOE#		17
T6	Write cycle time	90	
T7	Chip enable setup time before HWE#	0	
T8	Write pulse width of HWE#	60	
T9	Chip disable hold time following write disable	2.5	
T10	Data setup time before HWE#	0	
T11	Data hold time following HWE#	3	

Common Memory and Attribute Memory Read Timing

Common Memory and Attribute Memory Write Timing


(7). PCMCIA Bus Timing 2: I/O mode Access Timing

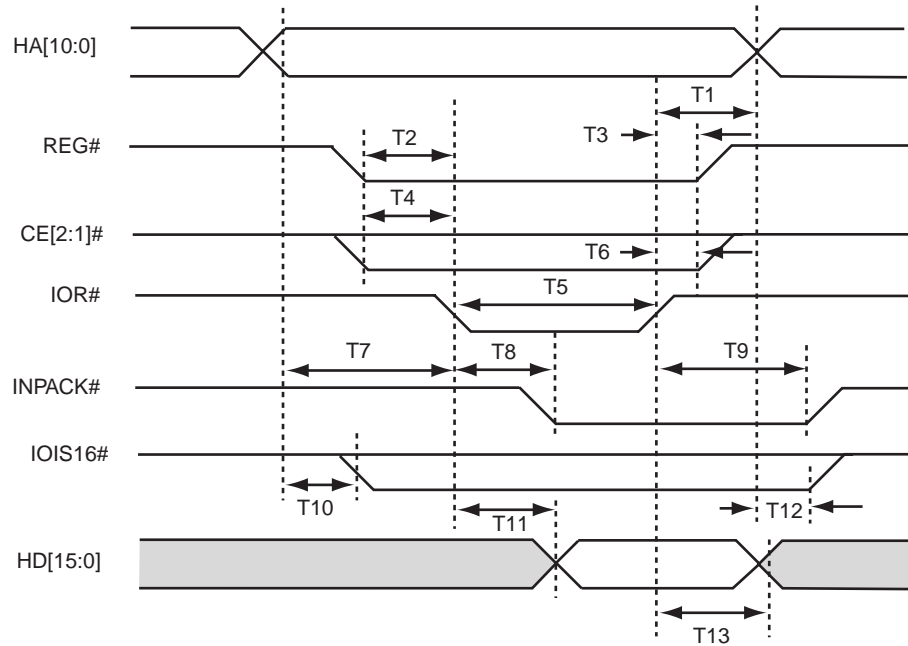
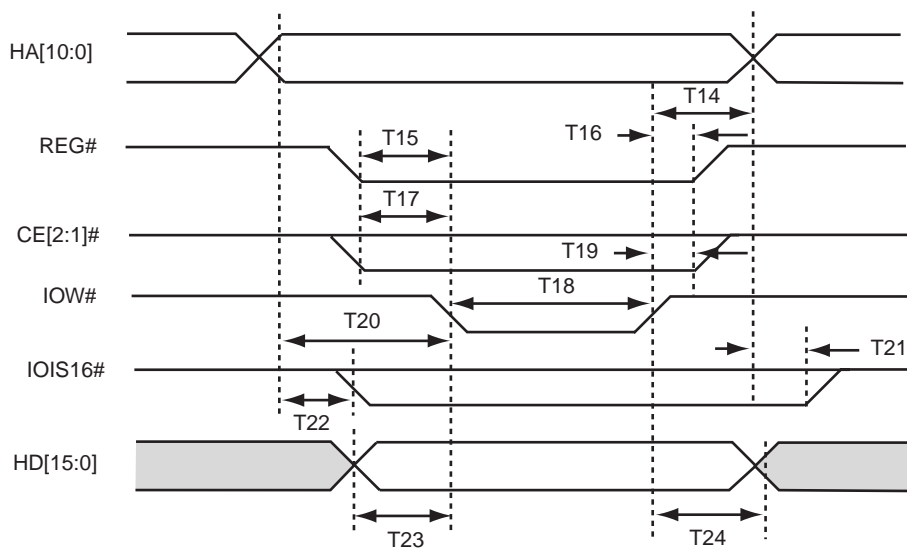
VCC = 5V±10%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Address hold time following IOR#	2	
T2	REG# setup time before IOR#	0	
T3	REG# hold time following IOR#	0	
T4	CE# setup time before IOR#	0	
T5	IOR# pulse width	60	
T6	CE# hold time following IOR#	2	
T7	Address setup time before IOR#	0	
T8	INPACK delay from IOR# falling edge		10
T9	INPACK delay from IOR# rising edge		10.5
T10	IOIS16 falling delay after Address changed		14
T11	Data delay after IOR# falling		32
T12	IOIS16 rising delay after Address changed		12.5
T13	Data hold time following IOR#		20
T14	Address hold time following IOW#	3	
T15	REG# setup time before IOW#	0	
T16	REG# hold time following IOW#	0	
T17	CE# setup time before IOW#	0	
T18	IOW# pulse with	60	
T19	CE# hold time following IOW#	2	
T20	Address setup time before IOW#	0	
T21	IOIS16 rising delay after Address changed		10.5
T22	IOIS16 falling delay after Address changed		14
T23	Data setup time before IOW#	0	
T24	Data hold time following IOW#	2.5	



VCC = 3.3V±5%

Symbol	Parameter	Min (ns)	Max (ns)
T1	Address hold time following IOR#	2	
T2	REG# setup time before IOR#	0	
T3	REG# hold time following IOR#	0	
T4	CE# setup time before IOR#	0	
T5	IOR# pulse width	90	
T6	CE# hold time following IOR#	2	
T7	Address setup time before IOR#	0	
T8	INPACK delay from IOR# falling edge		18
T9	INPACK delay from IOR# rising edge		18
T10	IOIS16 falling delay after Address changed		23.5
T11	Data delay after IOR# falling		47
T12	IOIS16 rising delay after Address changed		20
T13	Data hold time following IOR#	31	
T14	Address hold time following IOW#	4	
T15	REG# setup time before IOW#	0	
T16	REG# hold time following IOW#	0	
T17	CE# setup time before IOW#	0	
T18	IOW# pulse with	90	
T19	CE# hold time following IOW#	2.5	
T20	Address setup time before IOW#	0	
T21	IOIS16 rising delay after Address changed		20
T22	IOIS16 falling delay after Address changed		23.5
T23	Data setup time before IOW#	0	
T24	Data hold time following IOW#	3	

ID Read Timing

I/O Write Timing


(8). Flash Memory Interface Timing

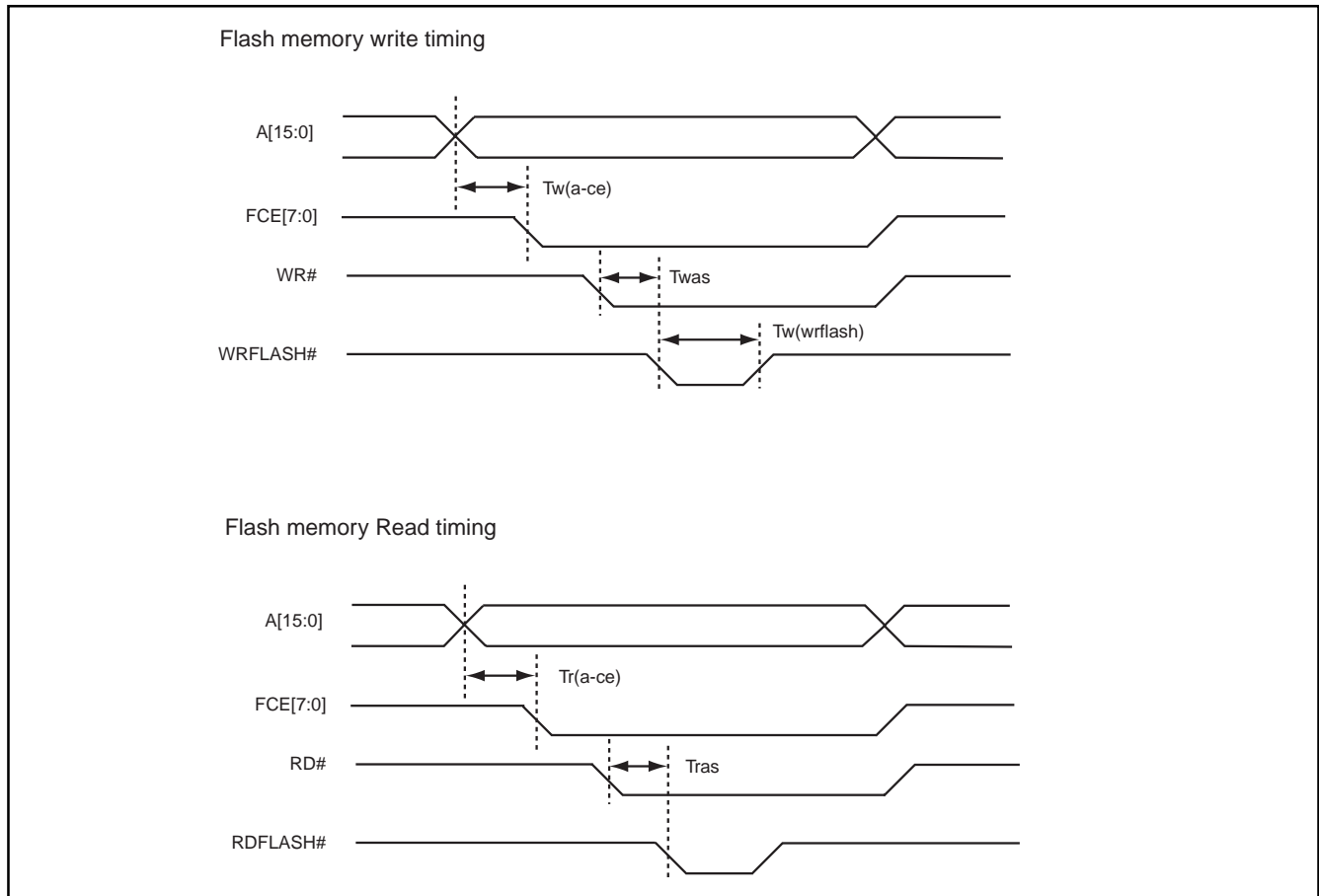
VCC = 5V±10%

Symbol	Parameter	Min	Max	Units
Tw(a-ce)	FCE# fall time after DSP address decode when write	5.5	15	ns
Twas	FCE# setup time before WRFLASH# falling edge	10	29.5	ns
Tw(wrflash)	WRFLASH# low pulse duration	1Tc *		ns
Tr(a-ce)	FCE# fall time after DSP address decode when read	5.5	15	ns
Tr(rd-oe)	RDFLASH# fall time after RD# falling edge	4.5	11.5	ns

VCC = 3.3V±5%

Symbol	Parameter	Min	Max	Units
Tw(a-ce)	FCE# fall time after DSP address decode when write	8	24.5	ns
Twas	FCE# setup time before WRFLASH# falling edge	14.5	49	ns
Tw(wrflash)	WRFLASH# low pulse duration	1Tc *		ns
Tr(a-ce)	FCE# fall time after DSP address decode when read	8	24.5	ns
Tr(rd-oe)	RDFLASH# fall time after RD# falling edge	6.5	20	ns

[* Note]: These timing are only for 1-system clock of flash memory write pulse is employed (601E[0]=0). If 2-system clock of pulse width is selected (601E[0]=1), the minimum time of Tw(wrflash) is 2Tc.



6-4. Latchup Characteristics

	Min.	Max.
Input Voltage with respect to GND on all VCC pins	-2.0V	12.0V
Input Voltage with respect to GND on all I/O pins	-2.0V	VCC+2.0V
Current	-100mA	+100mA

Includes all pins except GND. Test conditions: VCC=5.0V, one pin at a time.



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