Winbond Electronics Corp.

1M x 16 bit x 4 Banks SDRAM

Features

- 3.3V±0.3V power supply
- Comply to PC100/66 specification
- 1,048,576 words x 4 banks x 16 bits organization
- Auto Refresh and Self Refresh
- CAS latency: 2 and 3
- Burst Length: 1, 2, 4, 8 , and full page
- Sequential and Interleave burst
- Burst read, single-bit writes operation
- Byte data controlled by DQM
- Power-Down Mode
- Auto-Precharge and controlled precharge
- 4k refresh cycles / 64ms
- Interface: LVTTL
- Package: TSOP II 54 pin, 400 mil - 0.80

General Description

W986416AH is a high speed synchronous dynamic random access memory (SDRAM) , organized as 1M words x 4 banks x 16 bits. Using pipelined architecture, W986416AH delivers a data bandwidth of up to 250M bytes per second (-8H). To fully comply to the PC100/66 personal computer industrial standard, W986408AH is sorted into three speed grades: -8H, -8N/8L, and -10. The -8H is compliant to the PC100/CL2 specification, the -8N is compliant to PC100/CL3 specification, and -10 is compliant to PC/66 specification.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counrter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst legnth, latency cycle, interleave or sequential burst to maximize its performance. W986416AH is ideal for main memory in high performance applications.

Key Parameters

Symbol	Description	min/max	-8H	-8N	-10
t_{CK}	Clock Cycle Time	min	8ns	10ns	10ns
t_{AC}	Access Time from CLK	min	6ns	6ns	8ns
t_{RP}	Precharge to Active Command	min	20ns	20ns	30ns
t_{RCD}	Active to Read/Write Command	min	20ns	20ns	30ns
I_{CC1}	Operation Current (Single bank)	max	130mA	130mA	110mA
I_{CC4}	Burst Operation Current	max	210mA	210mA	190mA
I_{CC6}	Self-Refresh Current	max	2mA	2mA	2mA
I_{CC6L}	Self-Refresh Current	max	-	-	-

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BLOCK DIAGRAM
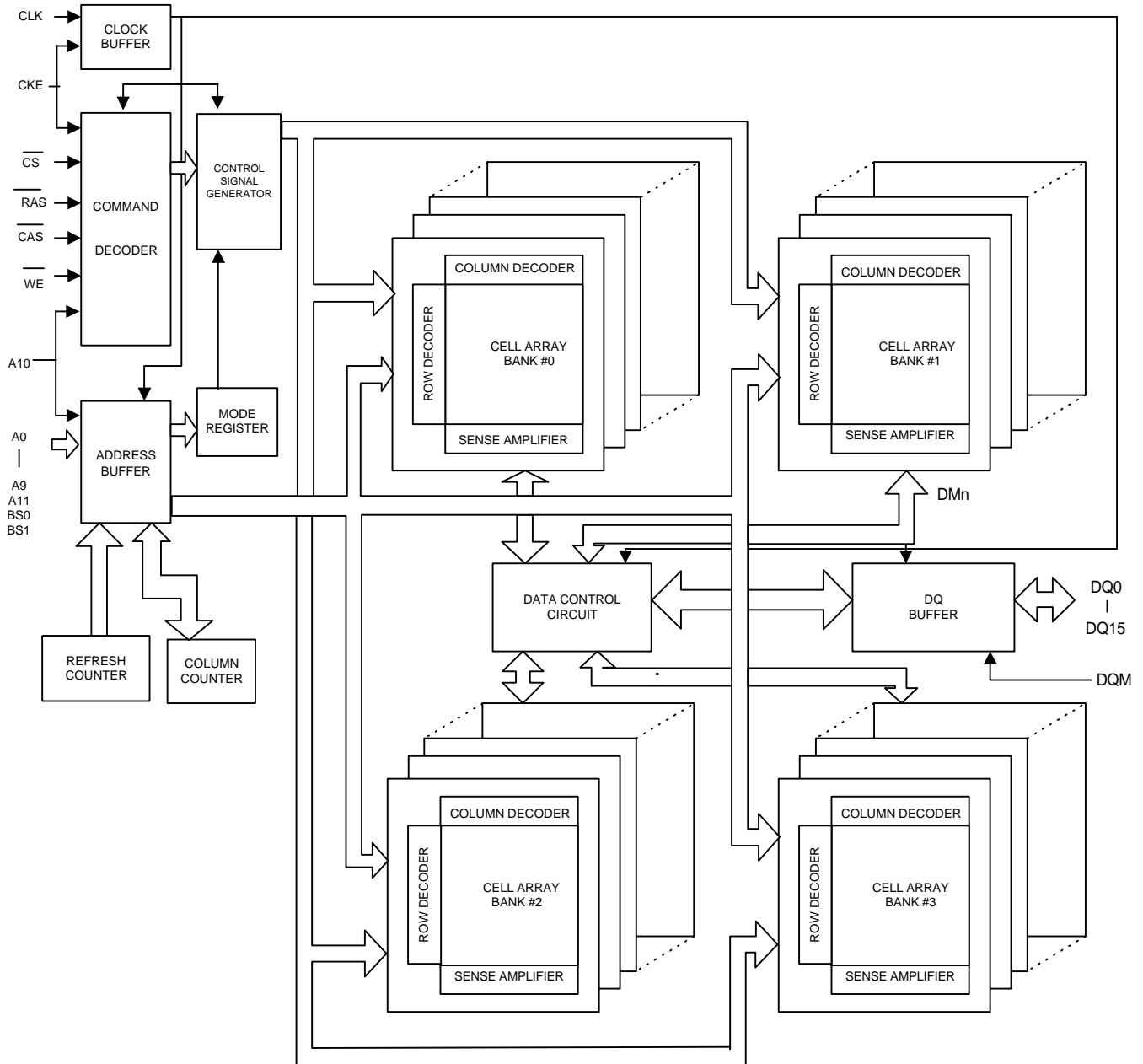
NOTE:
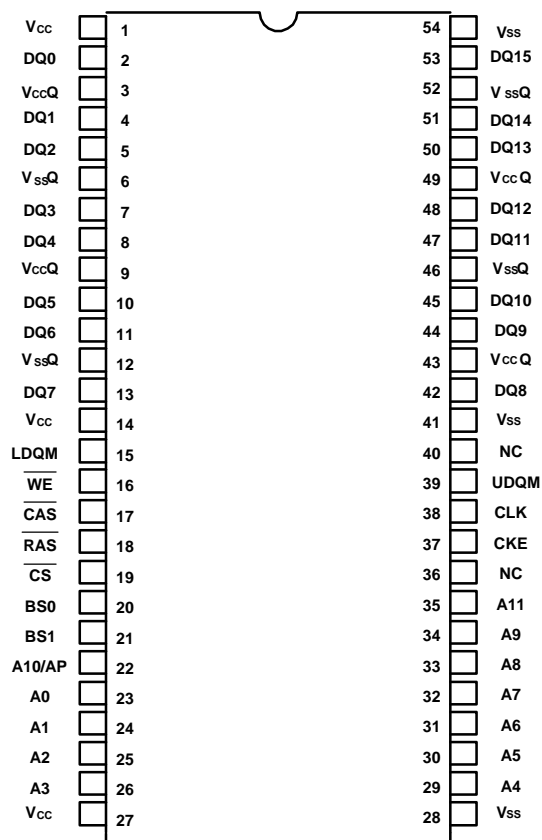The cell array configuration is 4096 * 256 * 16.

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Pin Assignment

Pin Number	Pin Name	Function	Description
23 ~ 26, 22, 29 ~35	A0~ A11	Address	Multiplexed pins for row and column address. Row address : A0 ~ A11. Column address: A0 ~ A7.
20, 21	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0 ~ DQ15	Data Input/ Output	Multiplexed pins for data output and input.
19	CS#	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
18	RAS#	Row Address Strobe	Command input. When sampled at the rising edge of the clock, RAS#, CAS# and WE# define the operation to be executed.
17	CAS#	Column Address Strobe	Referred to RAS#
16	WE#	Write Enable	Referred to RAS#
39, 15	UDQM/ LDQM	input/output mask	The output buffer is placed at Hi-Z(with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
38	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
37	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
1, 14, 27	V_{CC}	Power (+3.3 V)	Power for input buffers and logic circuit inside DRAM.
28, 41, 54	V_{ss}	Ground	Ground for input buffers and logic circuit inside DRAM.
3, 9, 43, 49	$V_{CC}Q$	Power (+ 3.3 V) for I/O buffer	Separated power from V_{CC}, used for output buffers to improve noise.
6, 12, 46, 52	$V_{ss}Q$	Ground for I/O buffer	Separated ground from V_{ss}, used for output buffers to improve noise.
36, 40	NC	No Connection	No connection

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Pin Assignment (Top View)

Left Pin	Pin #		Pin #	Right Pin
V$_{CC}$	1		54	V$_{ss}$
DQ0	2		53	DQ15
V$_{CC}$Q	3		52	V$_{ss}$Q
DQ1	4		51	DQ14
DQ2	5		50	DQ13
V$_{ss}$Q	6		49	V$_{CC}$Q
DQ3	7		48	DQ12
DQ4	8		47	DQ11
V$_{CC}$Q	9		46	V$_{ss}$Q
DQ5	10		45	DQ10
DQ6	11		44	DQ9
V$_{ss}$Q	12		43	V$_{CC}$Q
DQ7	13		42	DQ8
V$_{CC}$	14		41	V$_{ss}$
LDQM	15		40	NC
$\overline{WE}$	16		39	UDQM
$\overline{CAS}$	17		38	CLK
$\overline{RAS}$	18		37	CKE
$\overline{CS}$	19		36	NC
BS0	20		35	A11
BS1	21		34	A9
A10/AP	22		33	A8
A0	23		32	A7
A1	24		31	A6
A2	25		30	A5
A3	26		29	A4
V$_{CC}$	27		28	V$_{ss}$

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}, V_{OUT}	Input, column Output Voltage	$-0.3 \sim V_{CC}+0.3$	V	1
$V_{CC}, V_{CC}Q$	Power Supply Voltage	$-0.3 \sim 4.6$	V	1
T_{OPR}	Operating Temperature	$0 \sim 70$	°C	1
T_{STG}	Storage Temperature	$-55 \sim 150$	°C	1
T_{SOLDER}	Soldering Temperature(10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°c)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	-	$V_{CC}+0.3$	V	2
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	2

Note: $V_{IH}(max) = V_{CC}/V_{CC}Q+1.2V$ for pulse width $\leq$ 5ns
$V_{IL}(min) = V_{SS}/V_{SS}Q-1.2V$ for pulse width $\leq$ 5ns

CAPACITANCE (V_{CC}=3.3V, Af = 1MHz, Ta=25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
	Input Capacitance (A0 to A11, BS0 ,BS1, CS, RAS, CAS, WE, DQM, CKE)	-	4	pf
C_1	Input Capacitance (CLK)	-	6	pf
C_0	Input/Output capacitance	-	5	pf

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AC CHARACTERISTICS AND OPERATING CONDITION

(Vcc=3.3V±0.3V, Ta=0° to 70°C   Notes:5, 6, 7)

SYMBOL	PARAMETER		-8H MIN	-8H MAX	-8N MIN	-8N MAX	-10 MIN	-10 MAX	UNIT
t_{RC}	Ref/Active to Ref/Active Command Period		68		72		90		ns
t_{RAS}	Active to precharge Command Period		48	100000	48	100000	60	100000	ns
t_{RCD}	Active to Read/Write Command Delay Time		20		20		30		
t_{CCD}	Read/Write(a) to Read/Write(b)Command		1		1		1		cycle
t_{RP}	Precharge to Active(b) Command Period		20		20		30		
t_{RPD}	Active(a) to Active(b) Command Period		20		20		20		
t_{WR}	Write Recovery Time	CL*=2	10		12		15		
		CL*=3	8		10		10		
t_{CK}	CLK Cycle Time	CL*=2	10	1000	12	1000	15	1000	
		CL*=3	8	1000	10	1000	10	1000	
t_{CH}	CLK High Level		3		3		3		
t_{CL}	CLK Low Level		3		3		3		
t_{AC}	Access Time from CLK	CL*=2		6		7		9	
		CL*=3		6		6		8	ns
t_{OH}	Output Data Hold Time		3		3		3		
t_{HZ}	Output Data High Impedance Time		3	8	3	8	3	10	
t_{LZ}	Output Data Low Impedance Time		0		0		0		
t_{SB}	Power Down Mode Entry Time		0	8	0	8	0	10	
t_{T}	Transition Time of CLK (Rise and Fall)		0.5	10	0.5	10	0.5	10	
t_{DS}	Data-in-Set-up Time		2		2		3		
t_{DH}	Data-in Hold Time		1		1		1		
t_{AS}	Address Set-up Time		2		2		3		
t_{AH}	Address Hold Time		1		1		1		
t_{CKS}	CKE Set-up Time		2		2		3		
t_{CKH}	CKE Hold Time		1		1		1		
t_{CMS}	Command Set-up Time		2		2		3		
t_{CMH}	Command Hold Time		1		1		1		
t_{REF}	Refresh Time			64		64		64	ms
t_{RSC}	Mode register Set Cycle Time		16		16		20		ns

(CL=CAS Latency)

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DC CHARACTERISTICS (V$_{CC}$ = 3.3V ± 0.3V, Ta=0°~70°C)

ITEMS		SYMBOL	-8H/-8N		-10		UNIT	NOTES
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT t$_{CK}$=min , t$_{RC}$=min Active Precharge command cycling without Burst operation	1 bank operation	I$_{CC1}$		130		110		3
STANDBY CURRENT t$_{CK}$=min , CS#=V$_{IH}$ V$_{IH/L}$=V$_{IH(min)}$/V$_{IL(max)}$ Bank : inactive state	CKE = V$_{IH}$	I$_{CC2}$		60		50		3
	CKE = V$_{IL}$ (Power Down mode)	I$_{CC2P}$		3		3		3
STANDBY CURRENT CLK=V$_{IL}$, CS#=V$_{IH}$ V$_{IH/L}$=V$_{IH}$(min)/V$_{IL}$(max) BANK : inactive state	CKE = V$_{IH}$	I$_{CC2S}$		5		5		
	CKE = V$_{IL}$ (Power Down mode)	I$_{CC2PS}$		2		2	mA	
NO OPERATING CURRENT T$_{CK}$=min CS#=V$_{IH}$(min) BANK : active state (4 banks)	CKE = V$_{IH}$	I$_{CC3}$		90		70		3
	CKE = V$_{IL}$ (Power Down mode)	I$_{CC3P}$		8		8		
BURST OPERATING CURRENT t$_{CK}$ = min Read / Write command cycling		I$_{CC4}$		210		190		3,4
AUTO REFRESH CURRENT t$_{CK}$ = min Auto Refresh command cycling		I$_{CC5}$		150		130		3
SELF REFRESH CURRENT (-8H/-8N/-10) Self Refresh mode CKE = 0.2V		I$_{CC6}$		2		2		

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTES
INPUT LEAKAGE CURRENT (0V ≤ V$_{IN}$ ≤ V$_{CC}$, all other pins not under test = 0V)	I$_{I(L)}$	-5	5	μA	
OUTPUT LEAKAGE CURRENT (Output disable , 0V ≤ V$_{OUT}$ ≤ V$_{CCQ}$)	I$_{O(L)}$	-5	5	μA	
LVTTL OUTPUT H LEVEL VOLTAGE (I$_{OUT}$ = -2mA)	V$_{OH}$	2.4	-	V	
LVTTL OUTPUT L LEVEL VOLTAGE (I$_{OUT}$ = 2mA)	V$_{OL}$	-	0.4	V	

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NOTES:

1. Operation exceeds "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the devices.

2. All voltages are referenced to V_{SS}

3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

4. These parameters depend on the output loading conditions. Specified values are obtained with output open.

5. Power up sequence is further described in the "Functional Description" section.

6. AC TESTING CONDITIONS

Output Reference Level	1.4V/1.4V
Output Load	See diagram B below
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signal	2ns
Input Reference Level	1.4V

AC TEST LOAD (A)   AC TEST LOAD (B)
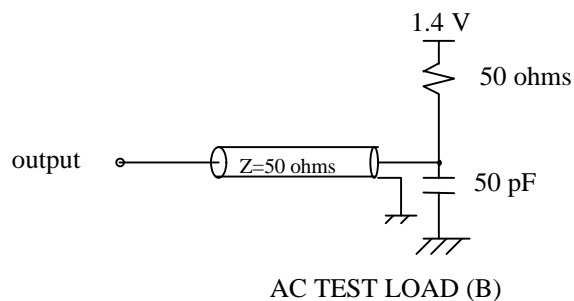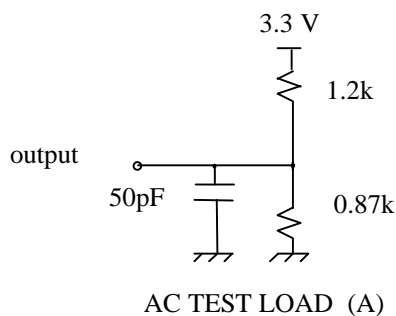
7. Transition times are measured between V_{IH} and V_{IL}.

8. t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.

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Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1 Truth Table   (note (1) , (2))

command	Device state	CKEn-1	CKEn	DQM	BS0,1	A10	A11, A9-0	$\overline{CS}$	$\overline{RA}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle	H	x	x	v	v	v	L	L	H	H
Bank Precharge	Any	H	x	x	v	L	x	L	L	H	L
Precharge All	Any	H	x	x	x	H	x	L	L	H	L
Write	Active (3)	H	x	x	v	L	v	L	H	L	L
Write with Autoprecharge	Active (3)	H	x	x	v	H	v	L	H	L	L
Read	Active (3)	H	x	x	v	L	v	L	H	L	H
Read with Autoprecharge	Active (3)	H	x	x	v	H	v	L	H	L	H
Mode Register Set	Idle	H	x	x	v	v	v	L	L	L	L
No - Operation	Any	H	x	x	x	x	x	L	H	H	H
Burst Stop	Active (4)	H	x	x	x	x	x	L	H	H	L
Device Deselect	Any	H	x	x	x	x	x	H	x	x	x
Auto - Refresh	Idle	H	H	x	x	x	x	L	L	L	H
Self - Refresh Entry	Idle	H	L	x	x	x	x	L	L	L	H
Self Refresh Exit	idle (S.R.)	L	H	x	x	x	x	H	x	x	x
		L	H	x	x	x	x	L	H	H	x
Clock suspend Mode Entry	Active	H	L	x	x	x	x	x	x	x	x
Power Down Mode Entry	Idle	H	L	x	x	x	x	H	x	x	x
	Active (5)	H	L	x	x	x	x	L	H	H	x
Clock Suspend Mode Exit	Active	L	H	x	x	x	x	x	x	x	x
Power Down Mode Exit	Any (power down)	L	H	x	x	x	x	H	x	x	x
		L	H	x	x	x	x	L	H	H	x
Data write/Output Enable	Active	H	x	L	x	x	x	x	x	x	x
Data Write/Output Disable	Active	H	x	H	x	x	x	x	x	x	x

Notes: (1) v= valid   x = Don't care   L= Low Level H= High Level
   (2) CKEn signal is input level when commands are provided.
   (3) These are state of bank designated by BS0, BS1 signals.
   (4) Device state is full page burst operation.
   (5) Power Down Mode can not be entered in the burst cycle.
       When this command asserts in the burst cycle, device state is clock suspend mode.

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Functional Description

Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs.

During power up, all V_{DD} and $V_{DD}Q$ pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed $V_{DD}+0.3V$ on any of the input pins or V_{DD} supplies. After power up, an initial pause of 200us is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of RAS, CAS, CS and WE at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to t_{RSC} has elapsed. Please refer to the next page for Mode Register Set Cycle and Operation Table.

Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The operation is similar to RAS# activate in EDO DRAM. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must not be less than the RAS to CAS delay time (t_{RCD}). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}). The maximum time that each bank can be held active is specified as t_{RAS}(max).
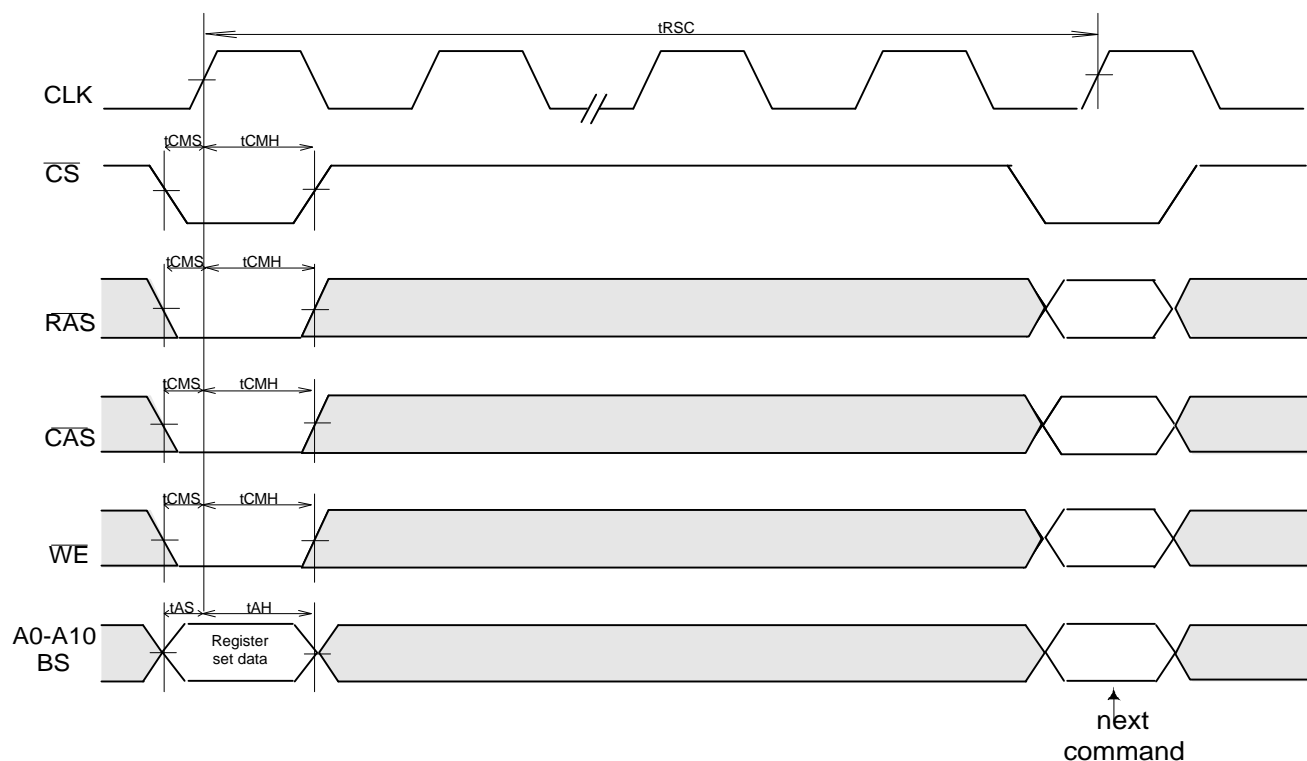
Read and Write Access Modes

After a bank has been activated , a read or write cycle can be followed. This is accomplished by setting RAS high and CAS low at the clock rising edge after minimum of t_{RCD} delay. WE pin voltage level defines whether the access cycle is a read operation (WE high), or a write operation (WE low). The address inputs determine the starting column address.

Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.

Cycle

Mode Register Set Cycle

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
A11	"0"	
BS0	"0"	
BS1	"0"	

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Burst Read Command

The Burst Read command is initiated by applying logic low level to CS and CAS while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page) during the Mode Register Set Up cycle. Table 2 and 3 in the next page explain the address sequence of interleave mode and sequence mode.

Burst Command

The Burst Write command is initiated by applying logic low level to CS, CAS and WE while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS latency from the interrupting Read Command the is satisfied.

Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having RAS and CAS high with CS and WE low at the rising edge of the clock. The data DQs go to a high impedance state after a delay which is equal to the CAS Latency in a burst read cycle interrupted by Burst Stop. If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored.

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Table 2 Address Sequence of Sequential Mode

DATA	Access Address	Burst Length
Data 0	n	BL= 2 (disturb address is A0)
Data 1	n + 1	No address carry from A0 to A1
Data 2	n + 2	BL= 4 (disturb addresses are A0 and A1)
Data 3	n + 3	No address carry from A1 to A2
Data 4	n + 4	
Data 5	n + 5	BL= 8 (disturb addresses are A0, A1 and A2)
Data 6	n + 6	No address carry from A2 to A3
Data 7	n + 7	

- Addressing Sequence of Sequential Mode

    A column access is performed by increasing the address from the column address which is input to the device. The disturb address is varied by the Burst Length as shown in Table 2.

- Addressing Sequence of Interleave Mode

    A column access is started in the input column address and is performed by inverting the address bit in the sequence shown in Table 3.

Table 3 Address Sequence of Interleave Mode

DATA	Access Address	Burst Length
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	BL = 2
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	BL = 4
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	BL = 8
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

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Auto-Precharge Command

If A10 is set to high when the Read or Write Command is issued, then the auto-precharge function is entered. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS latency.
A Read or Write Command with auto-precharge can not be interrupted before the entire burst operation is completed. Therefore, use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time (t_{RP}) has been satisfied. Issue of Auto-Precharge command is illegal if the burst is set to full page length. If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation one clock delay from the last burst write cycle. This delay is referred to as Write t_{DPL}. The bank undergoing auto-precharge can not be reactivated until t_{DPL} and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay ($t_{DAL} = t_{DPL} + t_{RP}$). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy t_{RAS}(min).

Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits, A10, A12, and A13, are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

Self Refresh Command

The Self Refresh Command is defined by having CS, RAS, CAS and CKE held low with WE high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The device will exit Self Refresh operation after CKE is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the RAS cycle time plus the Self Refresh exit time.

Power Down Mode

The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations, therefore the device can not remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on t_{CK}. The input buffers need to be enabled with CKE held high for a period equal to t_{CES}(min) + t_{CK}(min).

1M x 16 bit x 4 Banks SDRAM

No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS is low with RAS, CAS, and WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS is brought high, the RAS, CAS, and WE signals become don't cares.

Clock Suspend Mode

During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SDRAM operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

Timing Waveform

Command Input Timing
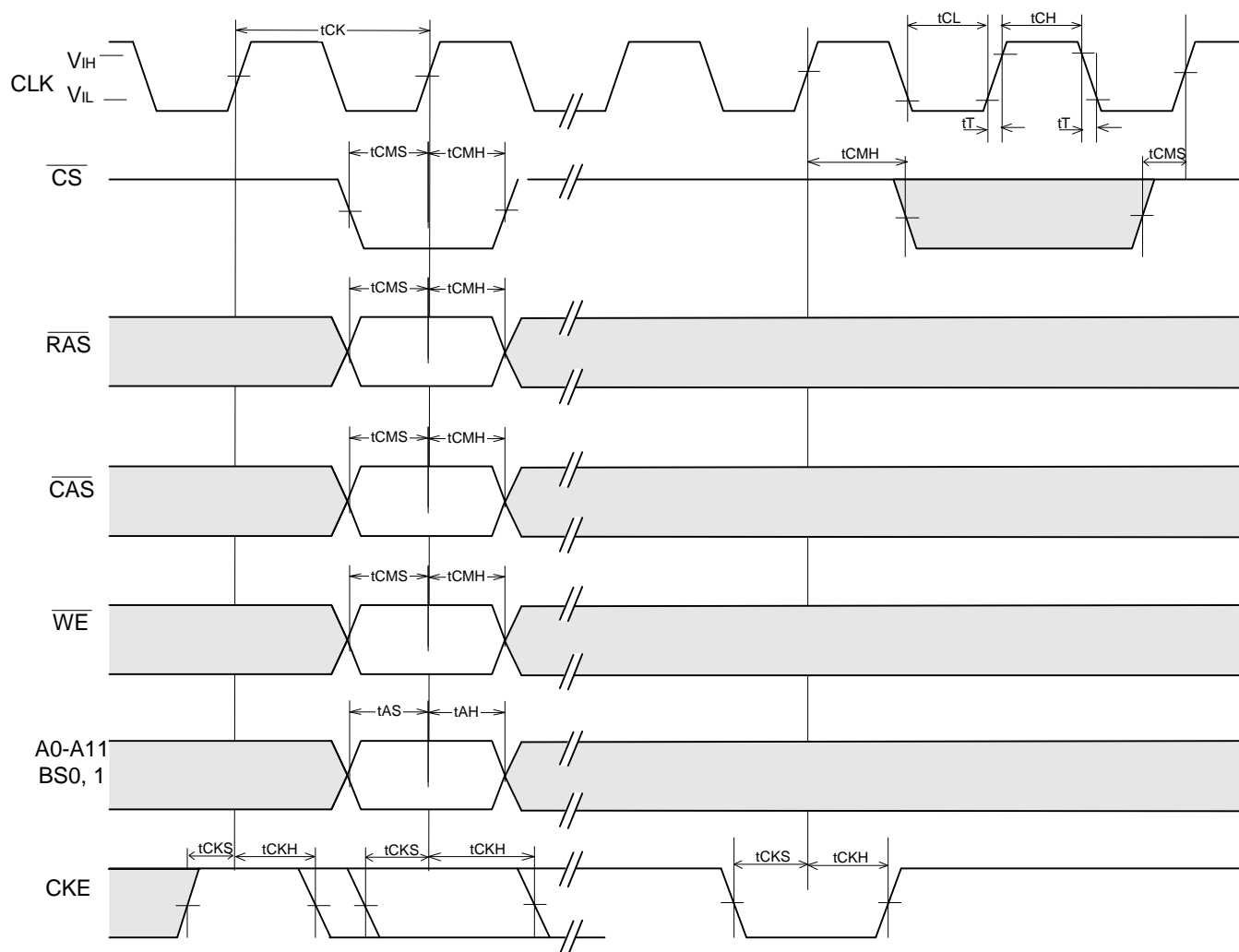
1M x 16 bit x 4 Banks SDRAM

Read Timing

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Electronics Corp.
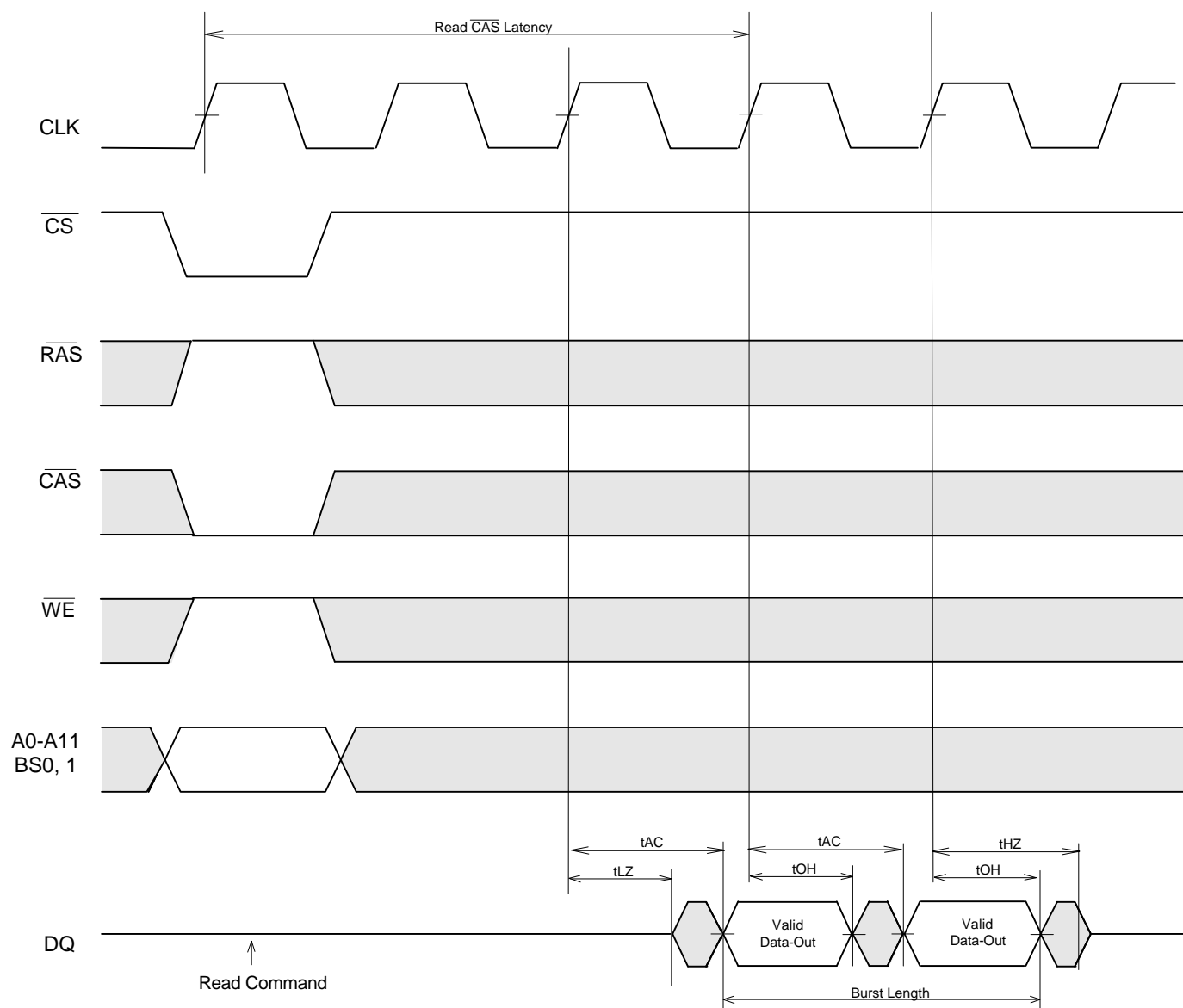
1M x 16 bit x 4 Banks SDRAM

Control Timing of Input Data

(Word Mask)

CLK

tCMH   tCMS   tCMH   tCMS

DQM

tDS   tDH   tDS   tDH   tDS   tDH   tDS   tDH

DQ0 -15   Valid Data-in   Valid Data-in   Valid Data-in   Valid Data-in

(Clock Mask)

CLK

tCKH   tCKS   tCKH   tCKS

CKE

tDS   tDH   tDS   tDH   tDS   tDH   tDS   tDH

DQ0 -15   Valid Data-in   Valid Data-in   Valid Data-in   Valid Data-in
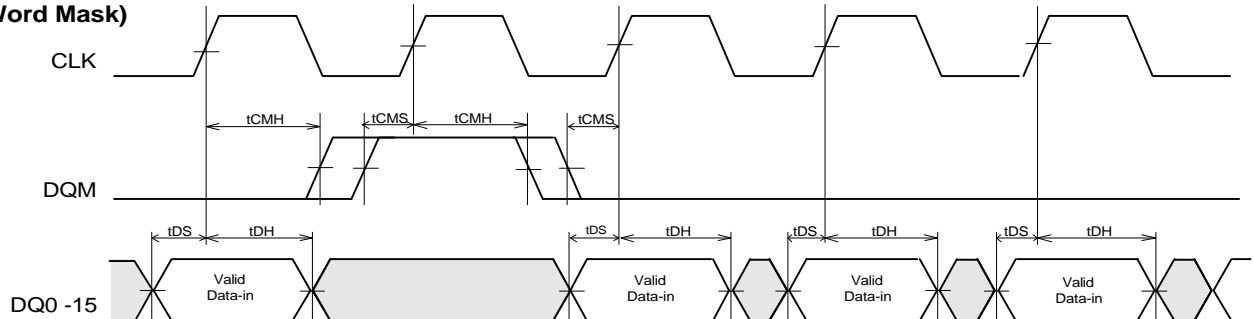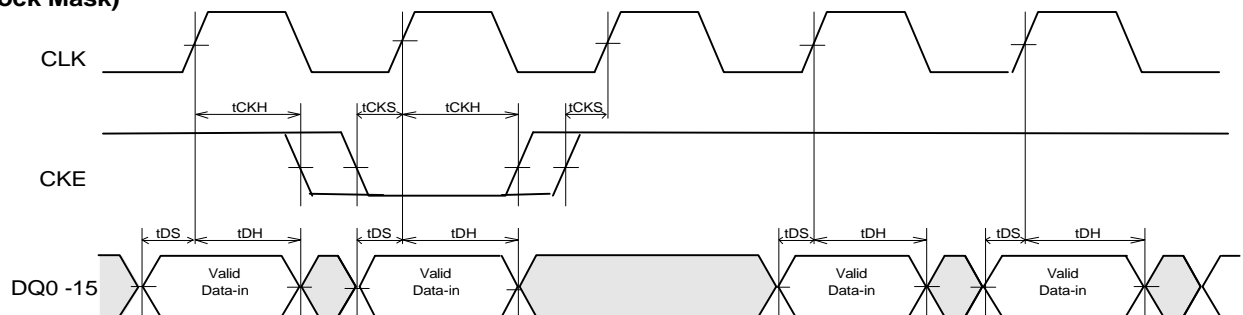
Control Timing of Output Data

(Output Enable)

CLK

tCMH   tCMS   tCMH   tCMS

DQM

tAC   tAC   tHZ   tAC   tAC
tOH   tOH   tOH   tLZ   tOH

DQ0 -15   Valid Data-Out   Valid Data-Out   OPEN   Valid Data-Out

(Clock Mask)

CLK

tCKH   tCKS   tCKH   tCKS

CKE

tAC   tAC   tAC   tAC
tOH   tOH   tOH   tOH

DQ0 -15   Valid Data-Out   Valid Data-Out   Valid Data-Out

Winbond
Electronics Corp.

Mode Register Set Cycle

A0		
A1	Burst Length	
A2		
A3	Addressing Mode	
A4		
A5	CAS Latency	
A6		
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	
A11	"0"	Reserved
BS0	"0"	
BS1	"0"	

			Burst Length	
A2	A1	A0	Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

Operating Timing Example

Interleaved Bank Read (Burst Length = 4, CAS Latency = 3)
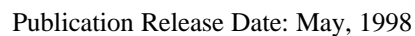
(CLK = 100 MHz)

1M x 16 bit x 4 Banks SDRAM

Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Autoprecharge)

(CLK = 100 MHz)

* AP is the internal precharge start timing

Interleaved Bank Read (Burst Length=8, CAS Latency=3)

(CLK = 100 MHz)

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1M x 16 bit x 4 Banks SDRAM

Interleaved Bank Read (Burst Length=8, CAS Latency=3, Autoprecharge)
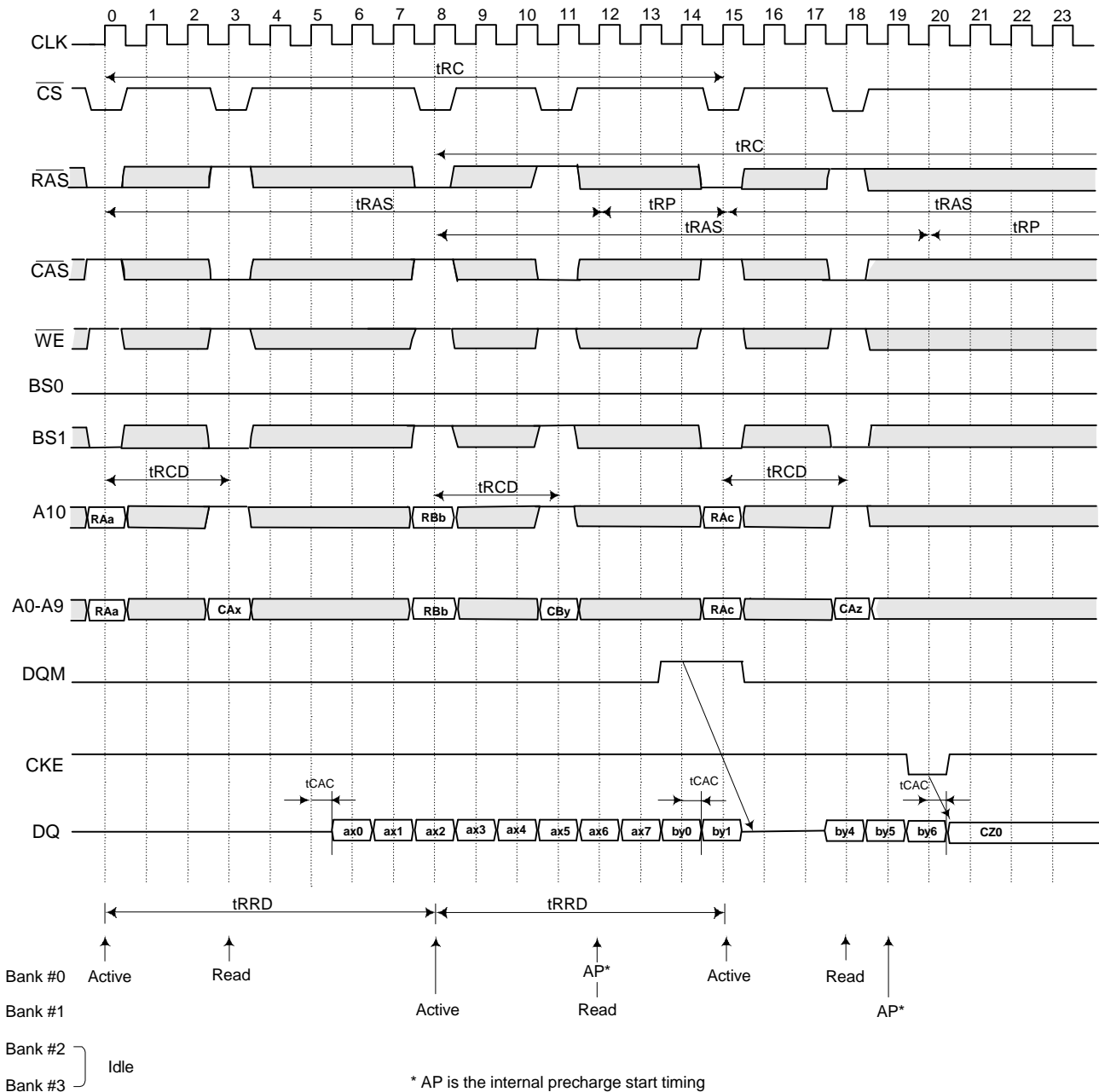
(CLK = 100 MHz)

* AP is the internal precharge start timing

Interleaved Bank Write (Burst Length=8)

(CLK = 100 MHz)

CLK

CS

RAS

tRC

tRAS tRP tRAS

tRAS tRP

CAS

tRCD tRCD tRCD

WE

BS0

BS1

A10 RAa RBb RAc

A0-A9, A11 RAa CAx RBb CBy RAc CAz

DQM

CKE

DQ ax0 ax1 ax4 ax5 ax6 ax7 by0 by1 by2 by3 by4 by5 by6 by7 CZ0 CZ1 CZ2

tRRD tRRD

Bank #0 Active Write Active Precharge Active Write

Bank #1 Active Write Precharge

Bank #2 ⎤
Bank #3 ⎦ Idle

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1M x 16 bit x 4 Banks SDRAM

Interleaved Bank Write (Burst Length=8, Autoprecharge)

(CLK = 100 MHz)

* AP is the internal precharge start timing
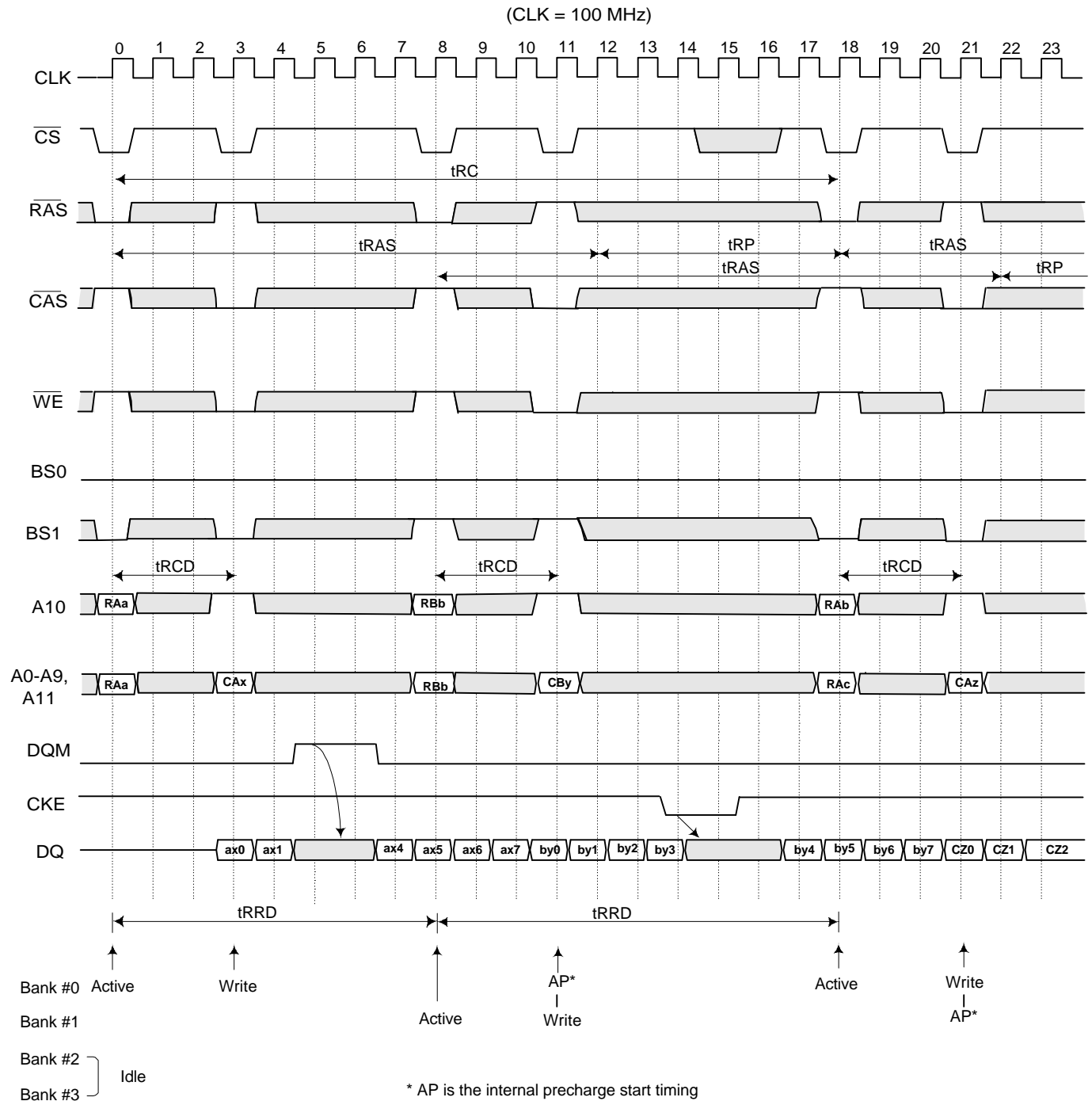
1M x 16 bit x 4 Banks SDRAM

Page Mode Read (Burst Length=4, CAS Latency=3)

(CLK = 100 MHz)

* AP is the internal precharge start timing
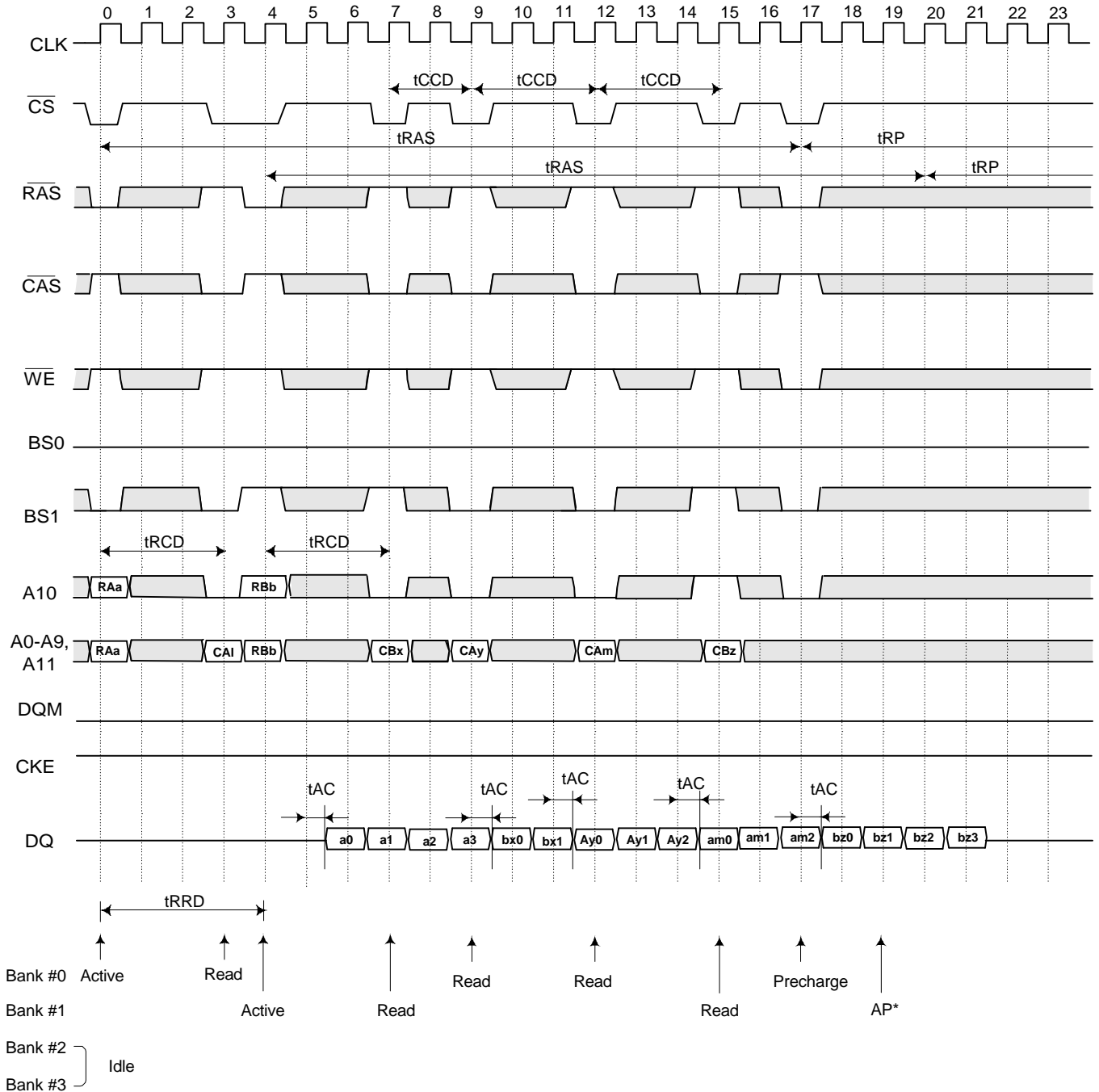
1M x 16 bit x 4 Banks SDRAM

Page Mode Read / Write (Burst Length=8, CAS Latency=3)
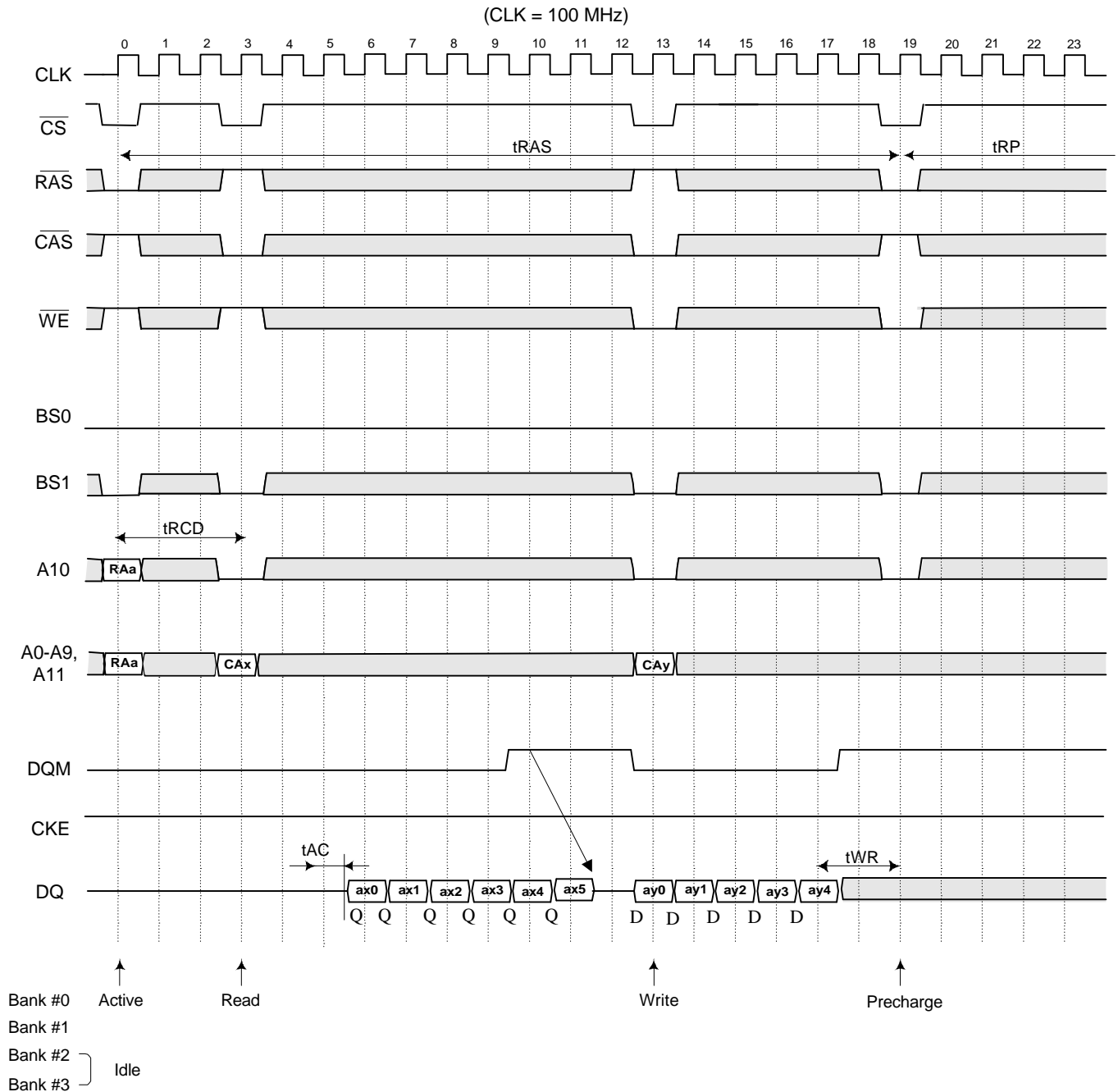
(CLK = 100 MHz)

AutoPrecharge Read (Burst Length = 4, CAS Latency = 3)

(CLK = 100 MHz)

CLK

CS

tRC   tRC

RAS

tRAS   tRP   tRAS   tRP

CAS

WE

BS0

BS1

tRCD   tRCD

A10   RAa   RAb

A0-A9, A11   RAa   CAw   RAb   CAx

DQM

CKE

tAC   tAC

DQ   aw0 aw1 aw2 aw3   bx0 bx1 bx2 bx3

Bank #0   Active   Read   AP*   Active   Read   AP*

Bank #1

Bank #2   ⎤ Idle

Bank #3   ⎦

* AP is the internal precharge start timing

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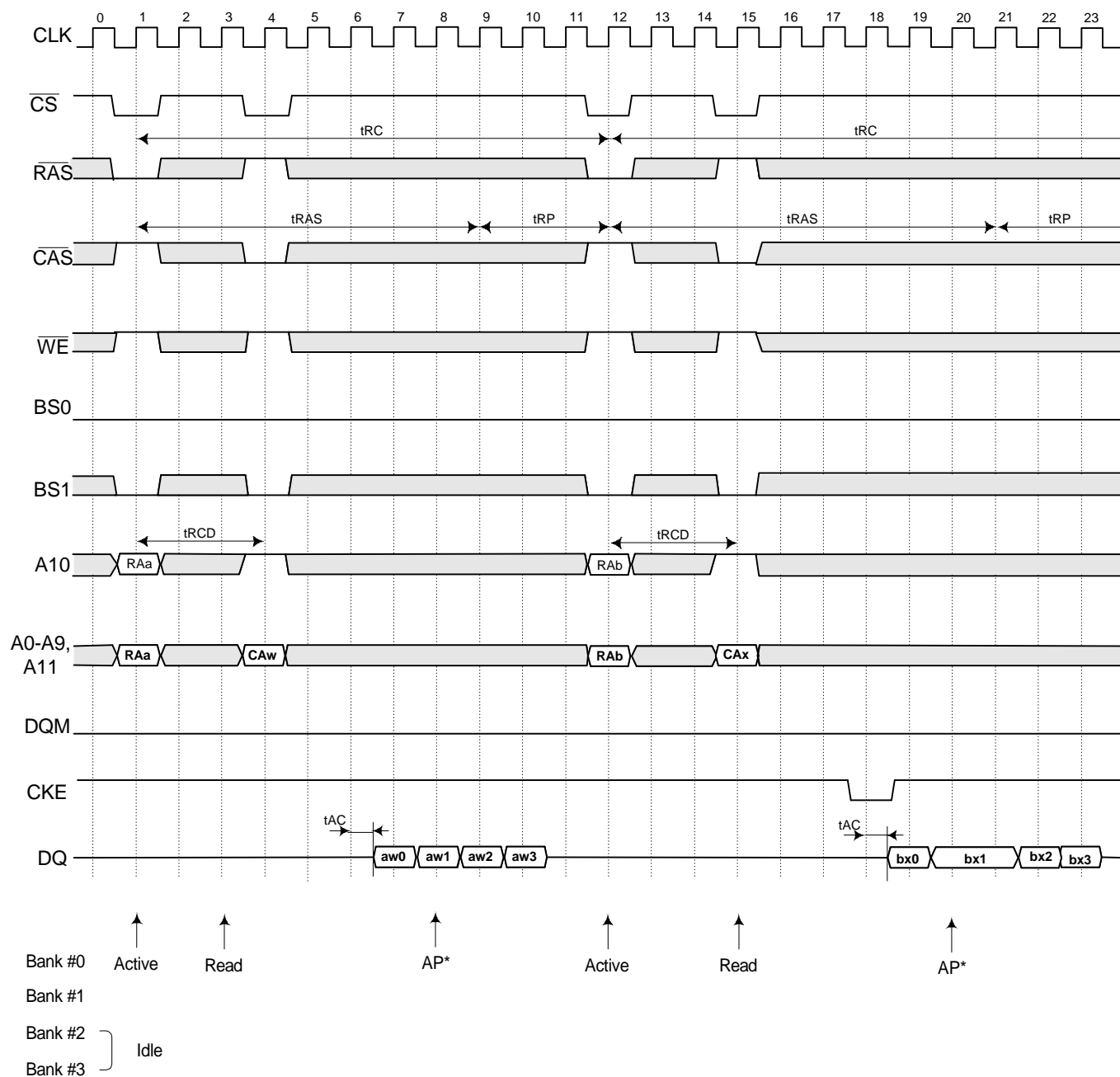
1M x 16 bit x 4 Banks SDRAM

AutoPrecharge Write (Burst Length = 4)

(CLK = 100 MHz)

Bank #0 Active Write AP* Active Write AP* Active

Bank #1

Bank #2 ⎤
         ⎬ Idle
Bank #3 ⎦

* AP is the internal precharge start timing
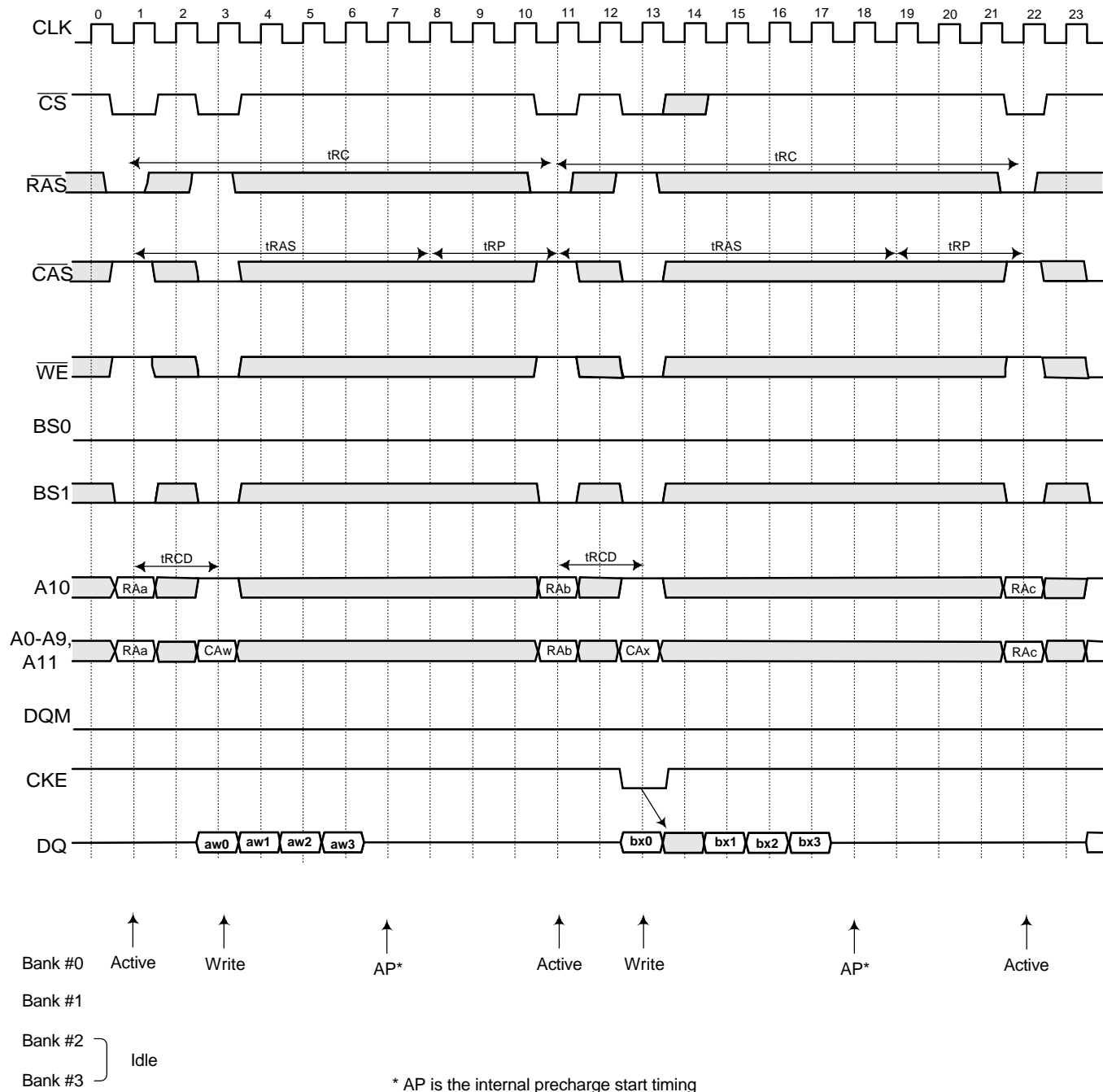
1M x 16 bit x 4 Banks SDRAM

AutoRefresh cycle

(CLK = 100 MHz)

All Banks Prechage   Auto Refresh   Auto Refresh (Arbitrary Cycle)

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Electronics Corp.
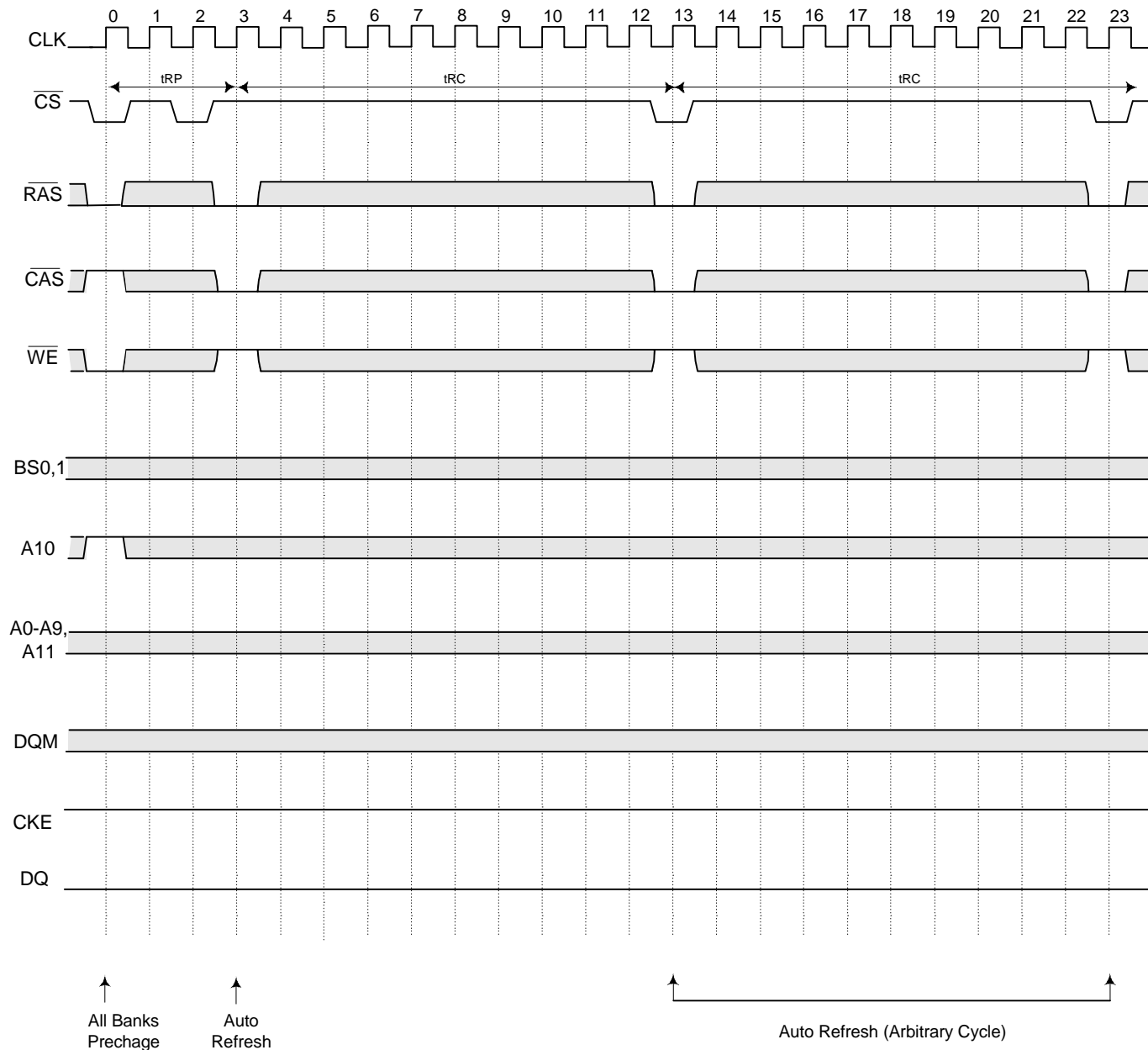
1M x 16 bit x 4 Banks SDRAM

SelfRefresh Cycle
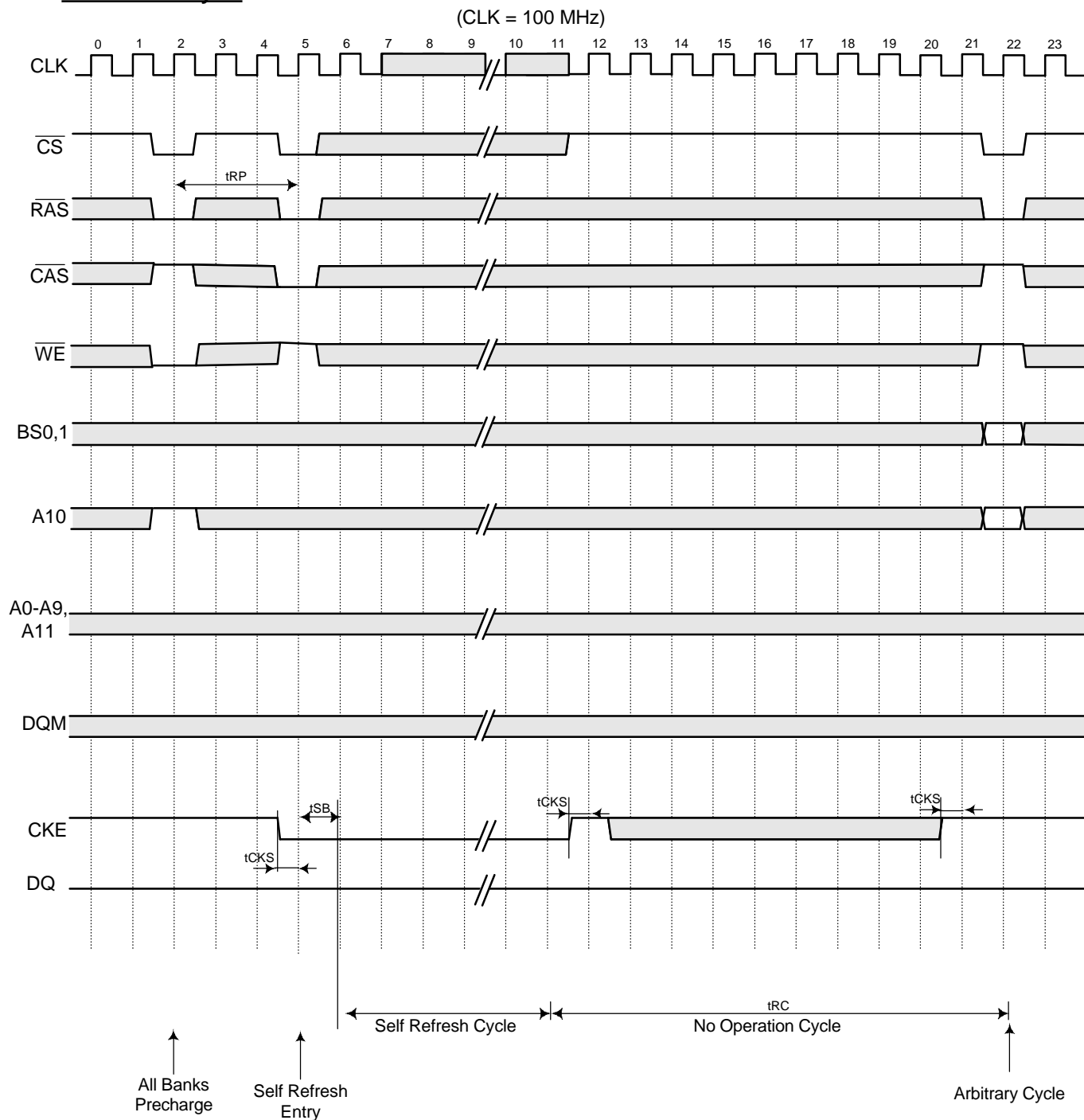
(CLK = 100 MHz)

Burst Read and Single Write (Burst Lenght = 4, CAS Latency = 3)

(CLK = 100 MHz)

Winbond
Electronics Corp.
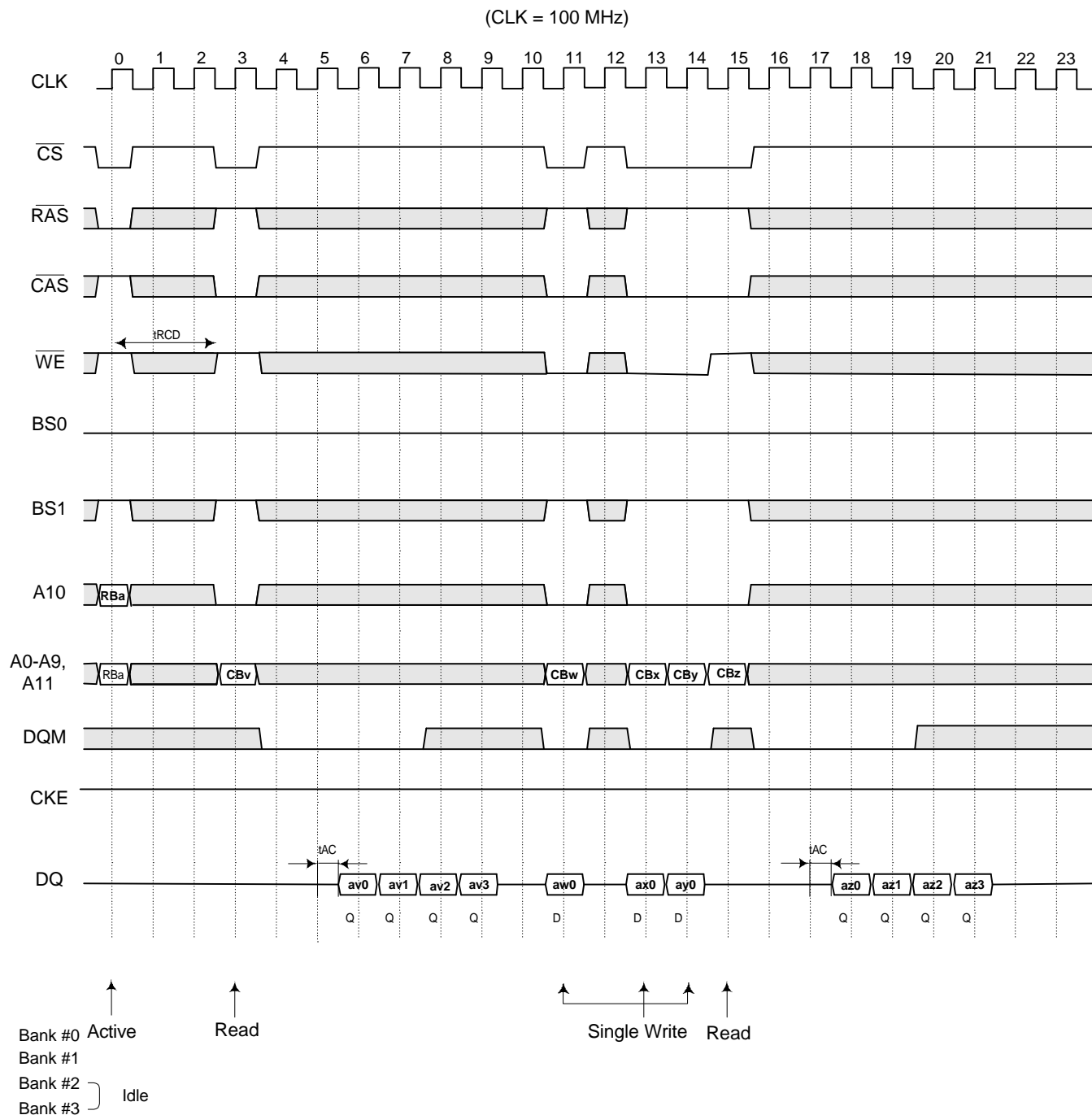
1M x 16 bit x 4 Banks SDRAM

PowerDown Mode

(CLK = 100 MHz)

CLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

CS

RAS

CAS

WE

BS

A10 — RAa — RAa

A0-A9 — RAa — CAa — RAa — CAx

DQM

CKE — tSB — tSB

DQ — ax0 ax1 ax2 ax3

tCKS tCKS tCKS tCKS

Active — NOP — Precharge — NOP Active

Active Standby
Power Down mode

Precharge Standby
Power Down mode
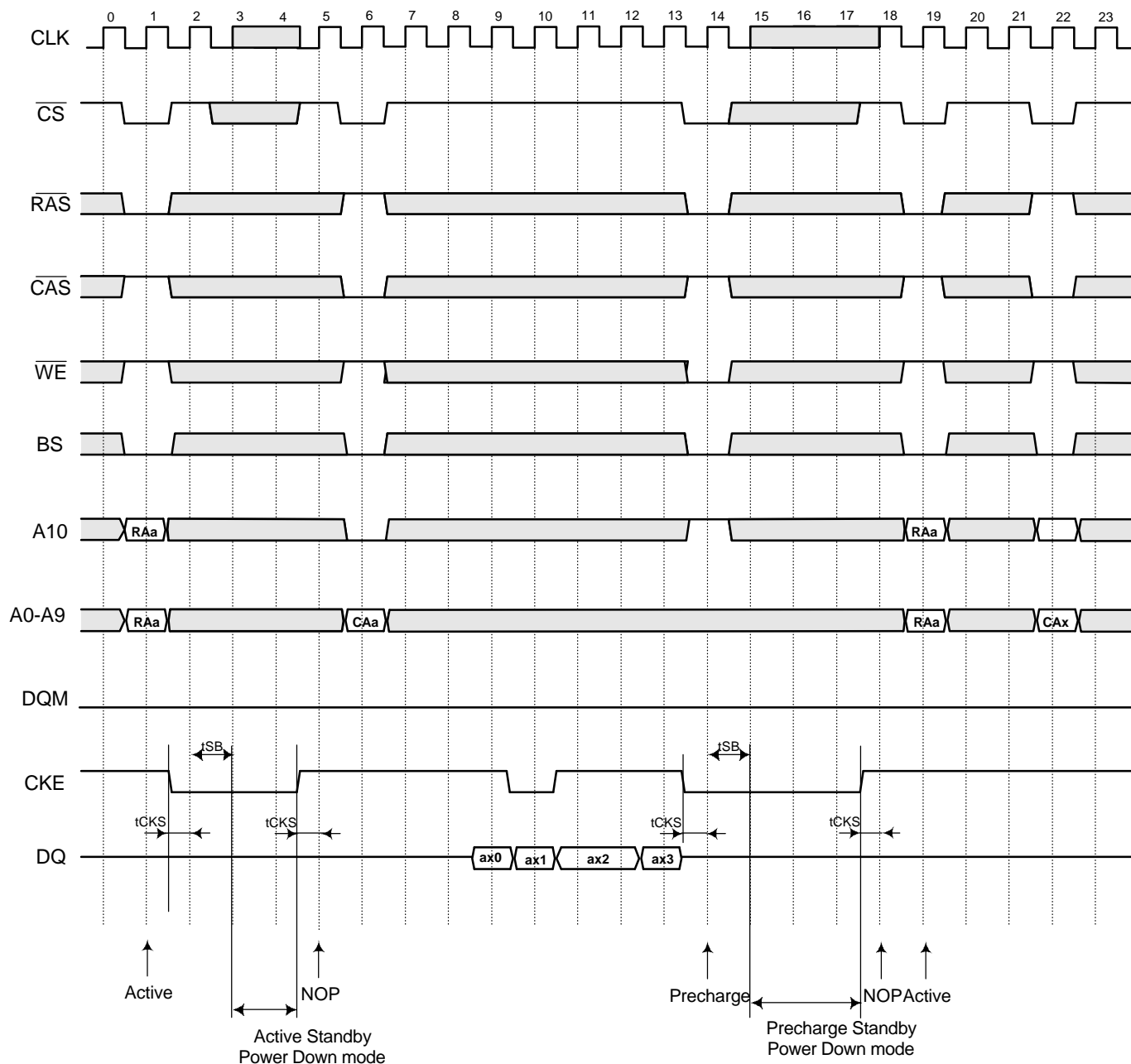
Note: The PowerDown Mode is entered by asserting CKE "low".
       All Input/Output buffers (except CKE buffers) are turned off in the PowerDown mode.
       When CKE goes high, command input must be No operation at next CLK rising edge.
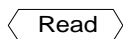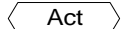
Autoprecharge Timing (Read Cycle)

Note)

⟨ Read ⟩   represents the Read with Auto precharge command.

⟨ AP ⟩   represents the start of internal precharging.

⟨ Act ⟩   represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS(min).

Autoprecharge timing (Read Cycle)
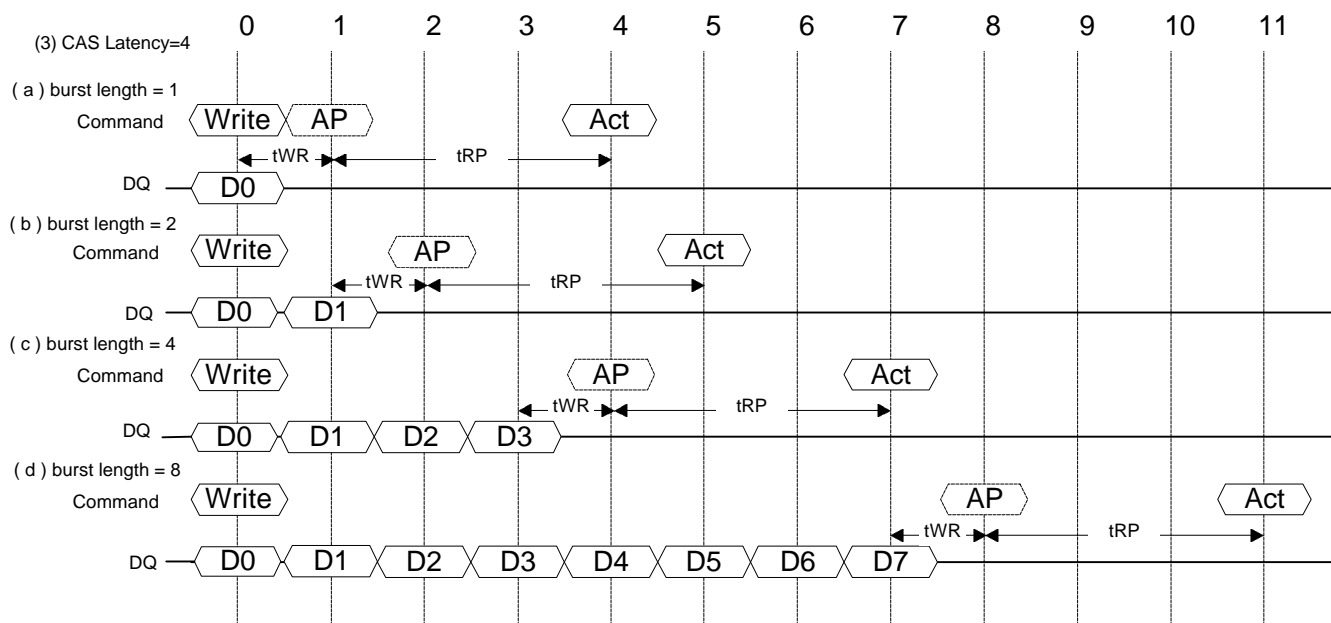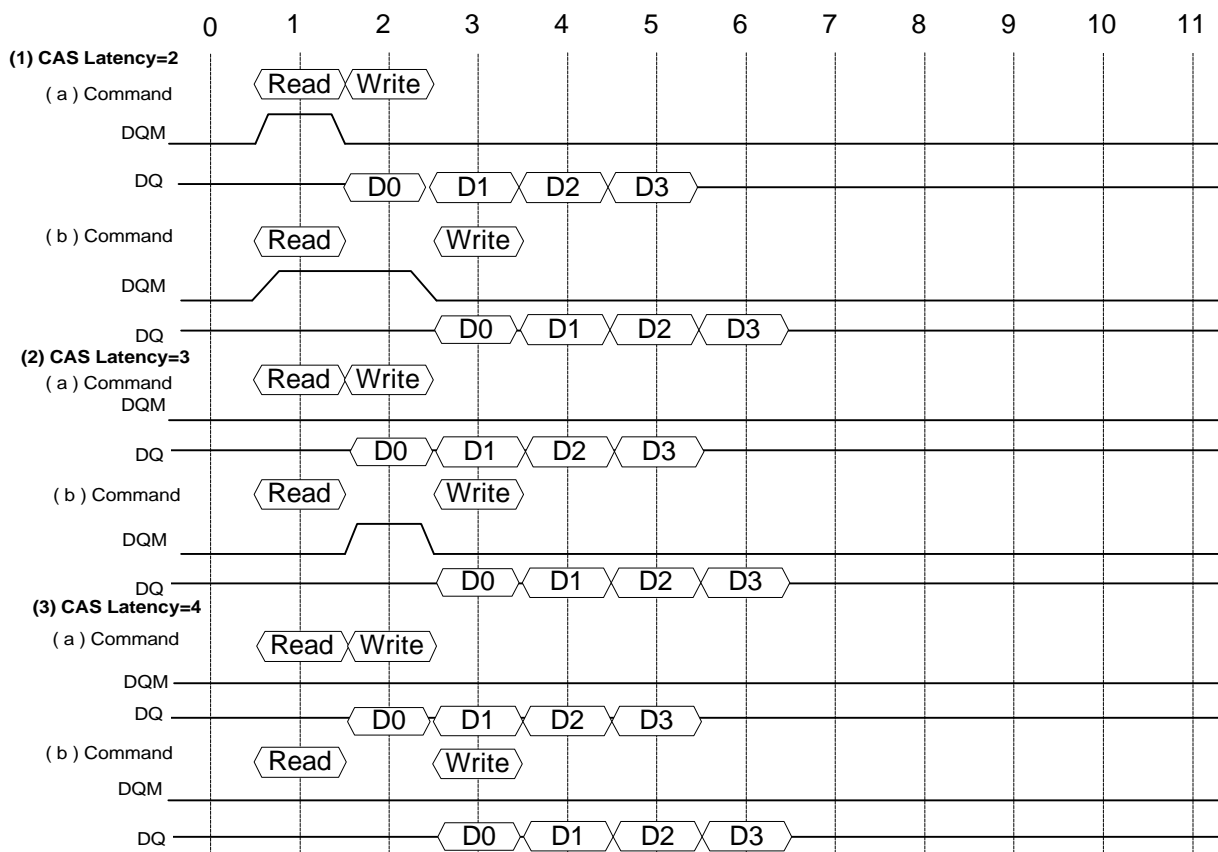

Note)

Read	represents the Read with Auto precharge command.
AP	represents the start of internal precharging.
Act	represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS(min).

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1M x 16 bit x 4 Banks SDRAM

Autoprecharge timing (Write Cycle)

Note)

| Write | represents the Write with Auto precharge command. |

| AP | represents the start of internal precharging. |

| Act | represents the Bank Activate command. |

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS(min)

Autoprecharge timing (Write Cycle)

(3) CAS Latency=4

(a) burst length = 1

(b) burst length = 2

(c) burst length = 4

(d) burst length = 8

Note)

⟨ Write ⟩   represents the Read with Auto precharge command.

⟨ AP ⟩   represents the start of internal precharging.

⟨ Act ⟩   represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least t_{RAS}(min).

Timing Chart of Read to Write cycle

In the case of Burst Length=4

Note) ¡¡E The Output data must be masked by DQM to avoid I/O conflict

Timing Chart of Write-to-Read cycle

In the case of Burst Length=4
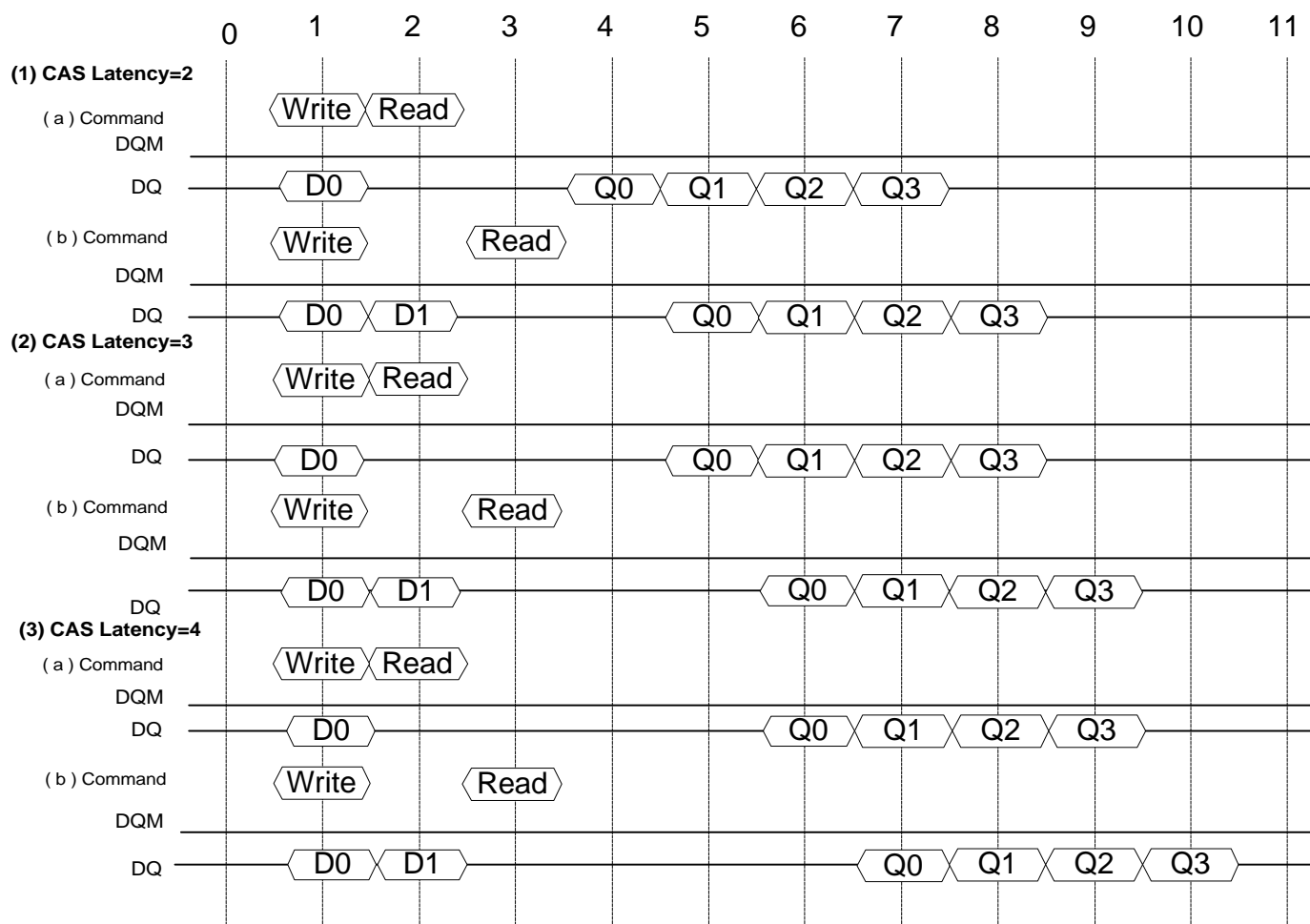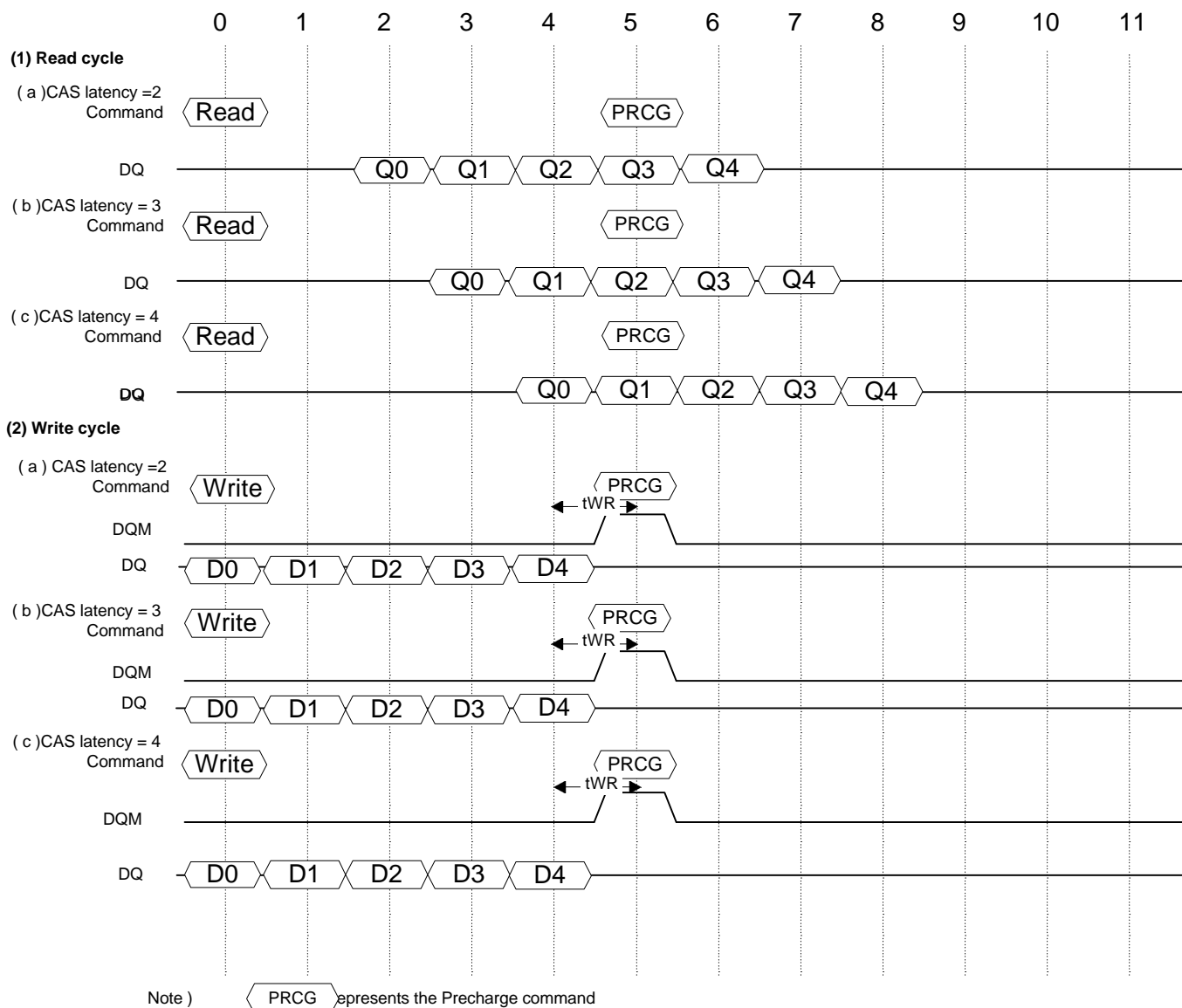
Timing chart of Burst Stop cycle (Burst stop Command)
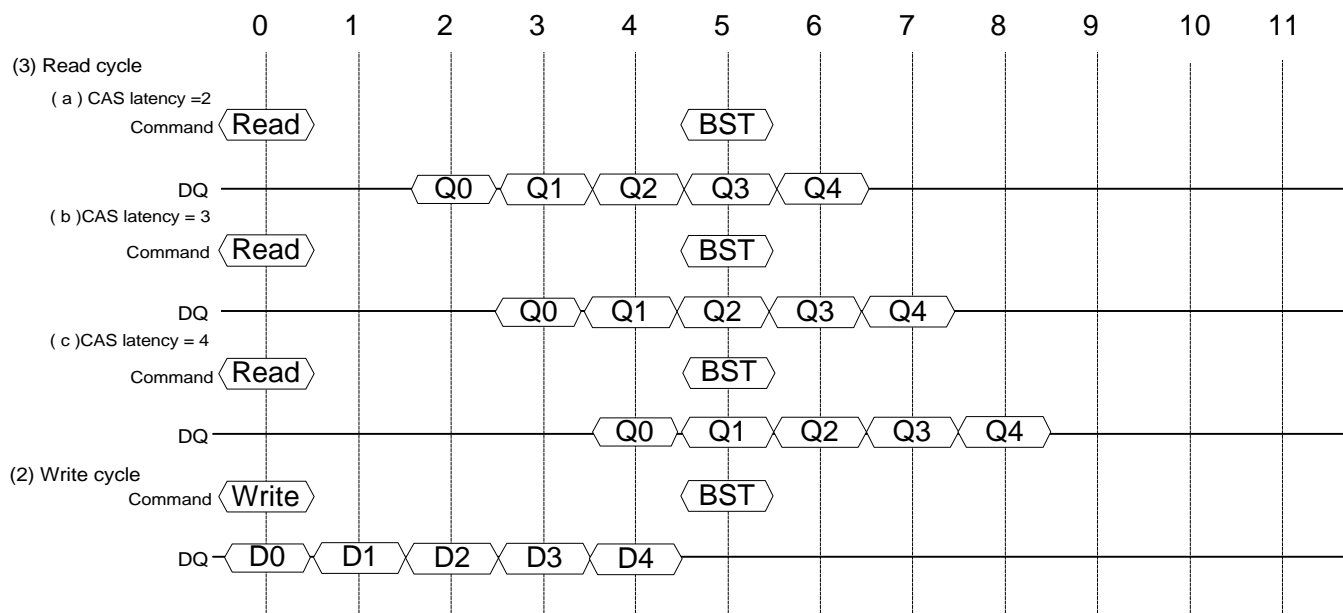

Note) 〈 BST 〉   represents the Burst stop command

Timing chart of Burst Stop cycle (Precharge Command)

In the case of Burst Lenght = 8

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

(1) Read cycle

(a)CAS latency =2
Command ⟨ Read ⟩   ⟨ PRCG ⟩

DQ   ⟨ Q0 ⟩⟨ Q1 ⟩⟨ Q2 ⟩⟨ Q3 ⟩⟨ Q4 ⟩

(b)CAS latency = 3
Command ⟨ Read ⟩   ⟨ PRCG ⟩

DQ   ⟨ Q0 ⟩⟨ Q1 ⟩⟨ Q2 ⟩⟨ Q3 ⟩⟨ Q4 ⟩

(c)CAS latency = 4
Command ⟨ Read ⟩   ⟨ PRCG ⟩

DQ   ⟨ Q0 ⟩⟨ Q1 ⟩⟨ Q2 ⟩⟨ Q3 ⟩⟨ Q4 ⟩

(2) Write cycle

(a) CAS latency =2
Command ⟨ Write ⟩   ⟨ PRCG ⟩

DQM   ←— tWR —→

DQ   ⟨ D0 ⟩⟨ D1 ⟩⟨ D2 ⟩⟨ D3 ⟩⟨ D4 ⟩

(b)CAS latency = 3
Command ⟨ Write ⟩   ⟨ PRCG ⟩

DQM   ←— tWR —→

DQ   ⟨ D0 ⟩⟨ D1 ⟩⟨ D2 ⟩⟨ D3 ⟩⟨ D4 ⟩

(c)CAS latency = 4
Command ⟨ Write ⟩   ⟨ PRCG ⟩

DQM   ←— tWR —→

DQ   ⟨ D0 ⟩⟨ D1 ⟩⟨ D2 ⟩⟨ D3 ⟩⟨ D4 ⟩

Note)   ⟨ PRCG ⟩ epresents the Precharge command

1M x 16 bit x 4 Banks SDRAM

CKE/DQM Input timing (Write cycle)

(1)

(2)

(3)

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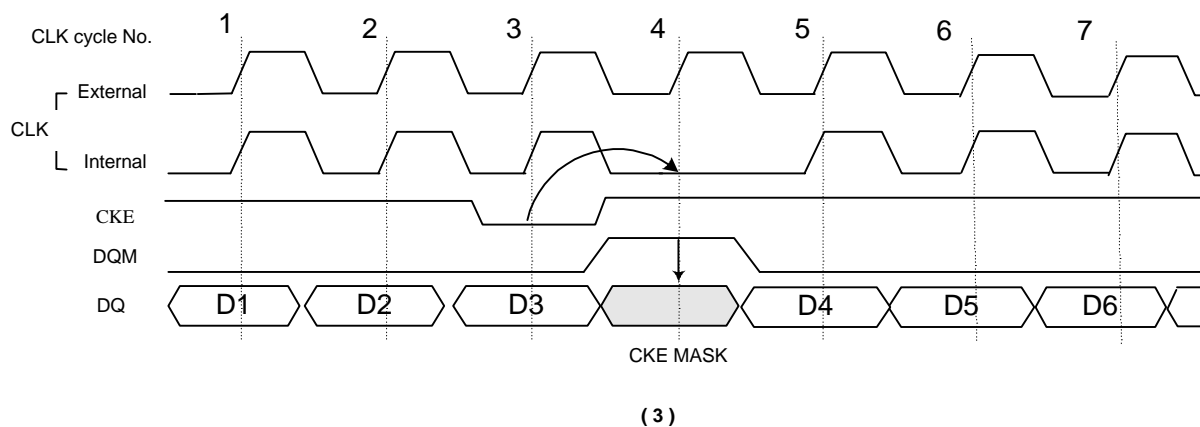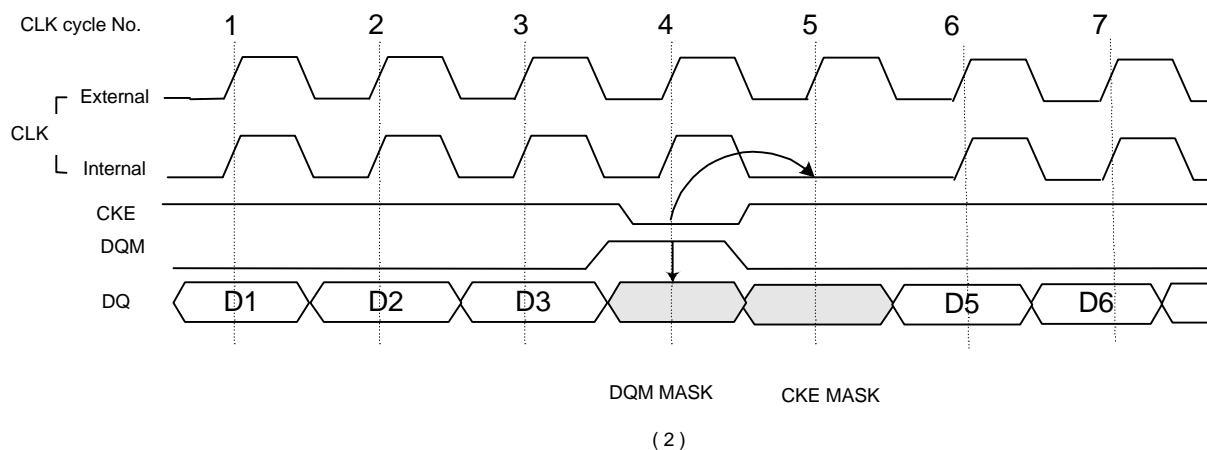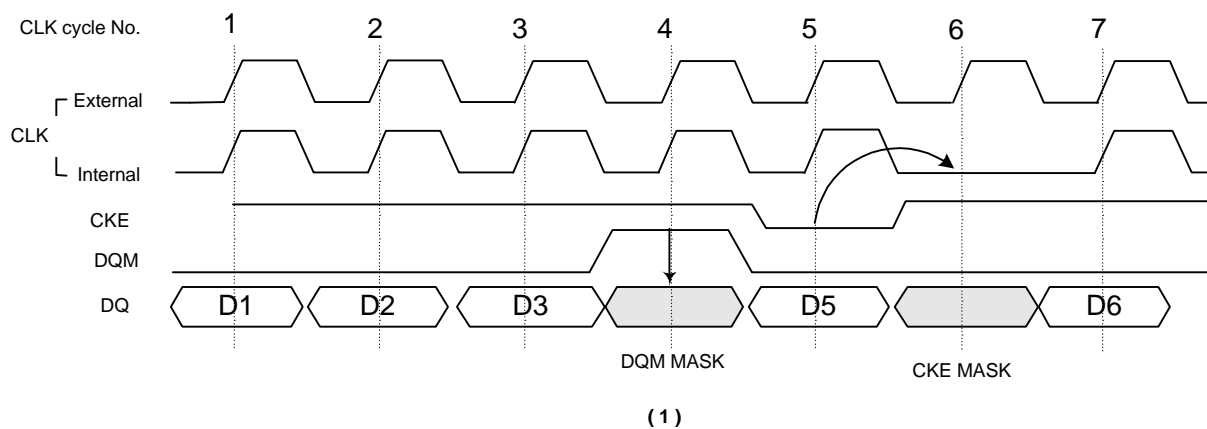
1M x 16 bit x 4 Banks SDRAM

CKE/DQM Input timing (Read cycle)
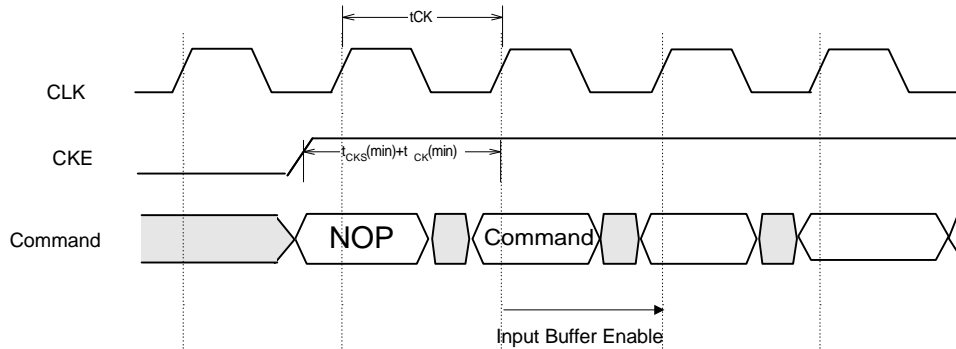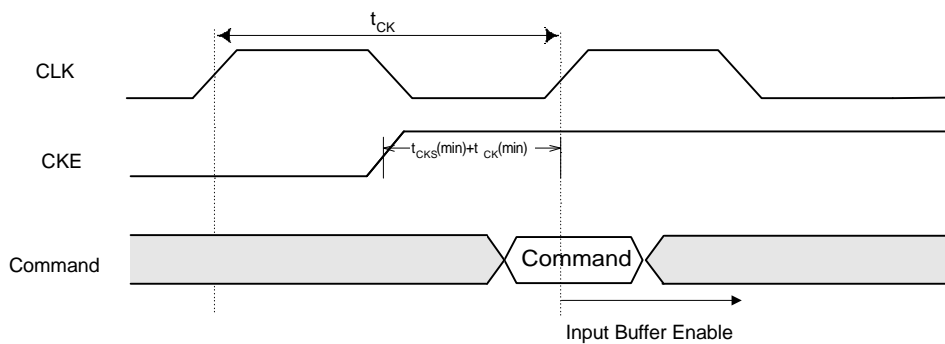

(1)

(2)

(3)
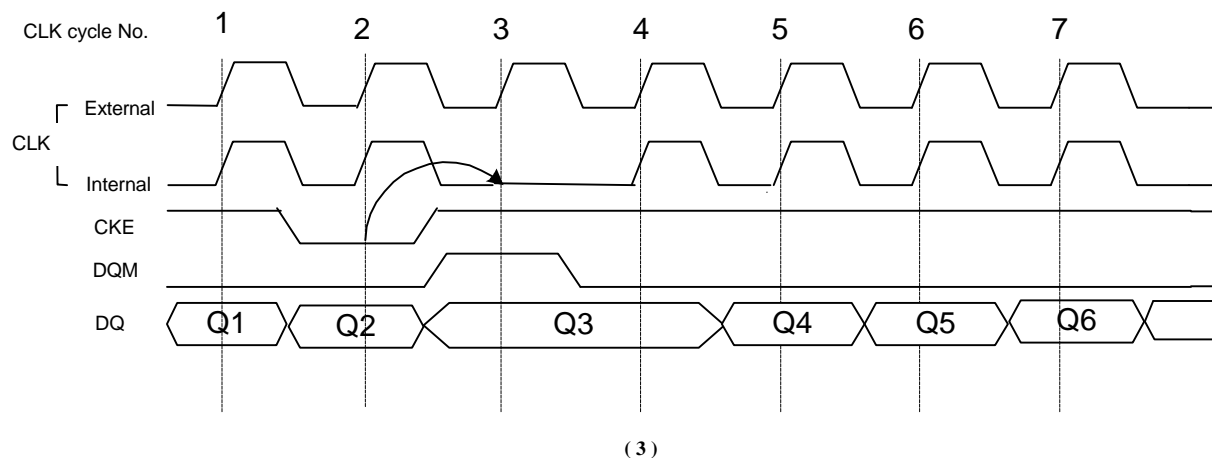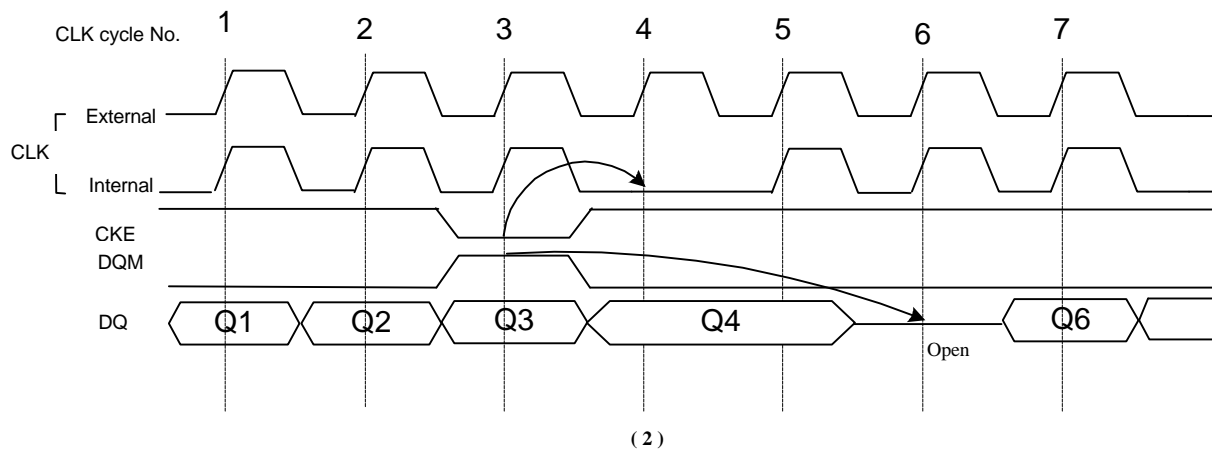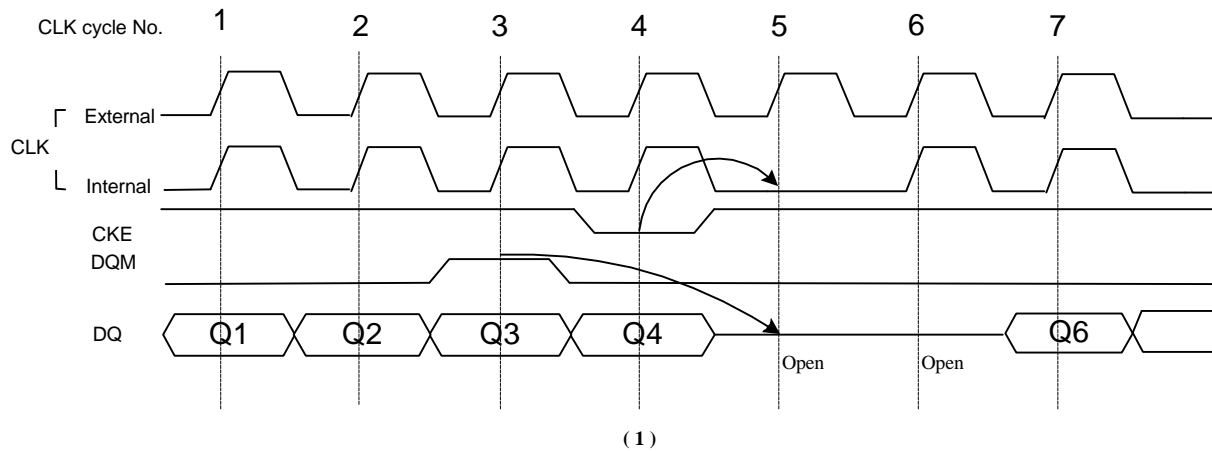
Self Refresh/Power Down Mode Exit Timing

Asynchronous Control
  Input Buffer turn on time (Power down mode exit time) is specified by tCKS(min) + tCK(min)
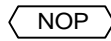
A) tCK < tCKS(min)+tCK(min)

CLK

CKE

Command

NOP

Command

Input Buffer Enable

B) tCK >= tCKS(min) + tCK (min)

CLK

CKE

Command

Command

Input Buffer Enable

Note)

All Input Buffer(Include CLK Buffer) are turned off in the Power Down mode and Self Refresh mode

NOP   Represents the No-Operation command

Command   Represents one command

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Electronics Corp.

1M x 16 bit x 4 Banks SDRAM

Package Dimension

54L TSOP (II)-400 mil
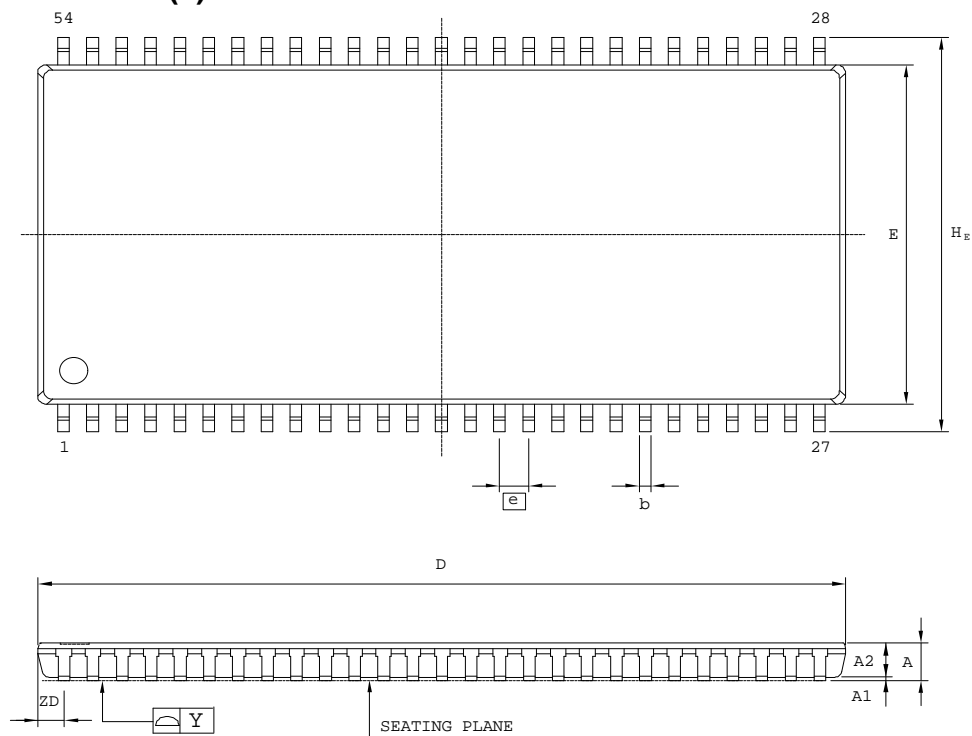
Controlling Dimension : Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	—	1.00	—	—	0.039	—
b	0.24	0.32	0.40	0.009	0.012	0.016
c	—	0.15	—	—	0.006	—
D	22.12	22.22	22.62	0.871	0.875	0.905
E	10.06	10.16	10.26	0.396	0.400	0.404
H	11.56	11.76	11.96	0.455	0.463	0.471
e	—	0.80	—	—	0.0315	—
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	—	0.80	—	—	0.032	—
Y	—	—	0.10	—	—	0.004
ZD	—	0.71	—	—	0.028	—