

DATA SHEET

BF909WR

N-channel dual-gate MOS-FET

Product specification
Supersedes data of 1995 Apr 25
File under Discrete Semiconductors, SC07

1997 Sep 05

N-channel dual-gate MOS-FET

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FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1

Top view

MAM192

s,b

g₂

g₁

d

Marking code: ME.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		—	—	7	V
I _D	drain current		—	—	40	mA
P _{tot}	total power dissipation		—	—	280	mW
T _j	operating junction temperature		—	—	150	°C
y _{fs}	forward transfer admittance		36	43	50	mS
C _{ig1-s}	input capacitance at gate 1		—	3.6	4.3	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	—	30	50	fF
F	noise figure	f = 800 MHz	—	2	2.8	dB

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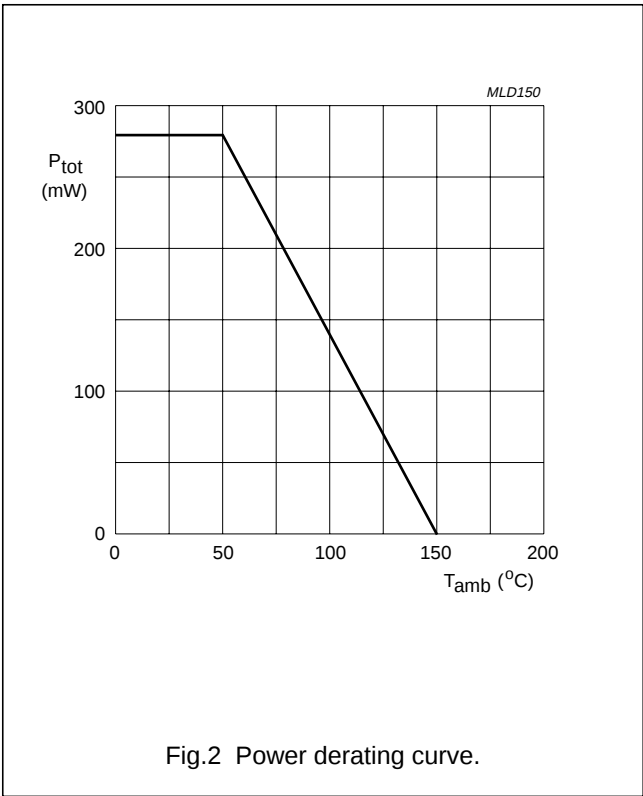
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation	up to $T_{amb} = 50\text{ }^{\circ}\text{C}$; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature range		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	+150	$^{\circ}\text{C}$

Note

- 1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point	$T_s = 91\ ^\circ\text{C}$; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\ \text{mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\ \text{mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\ \text{mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\ \text{mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 5\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 5\ \text{V}$; $R_{G1} = 120\ \text{k}\Omega$; note 1	12	20	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\ \text{V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 5\ \text{V}$	–	50	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5\ \text{V}$.

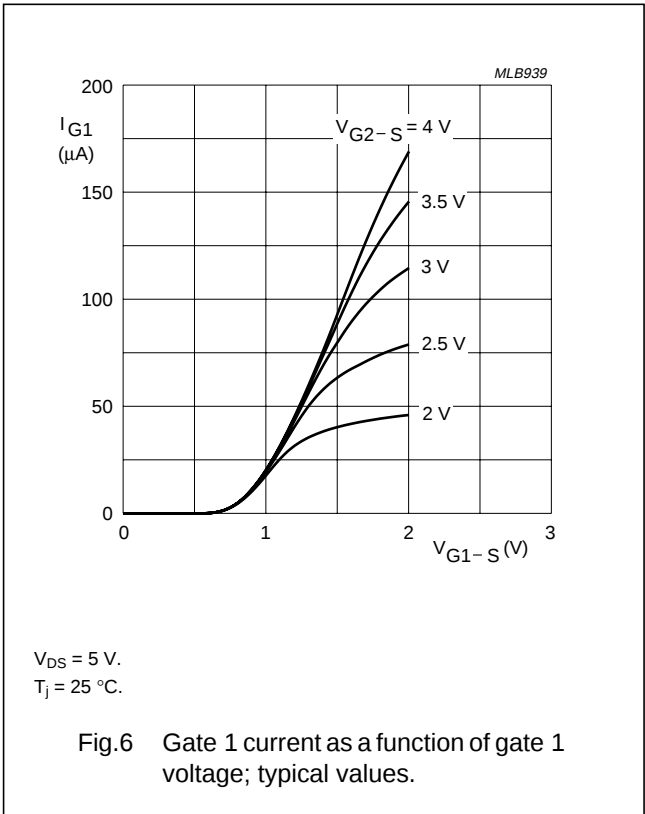
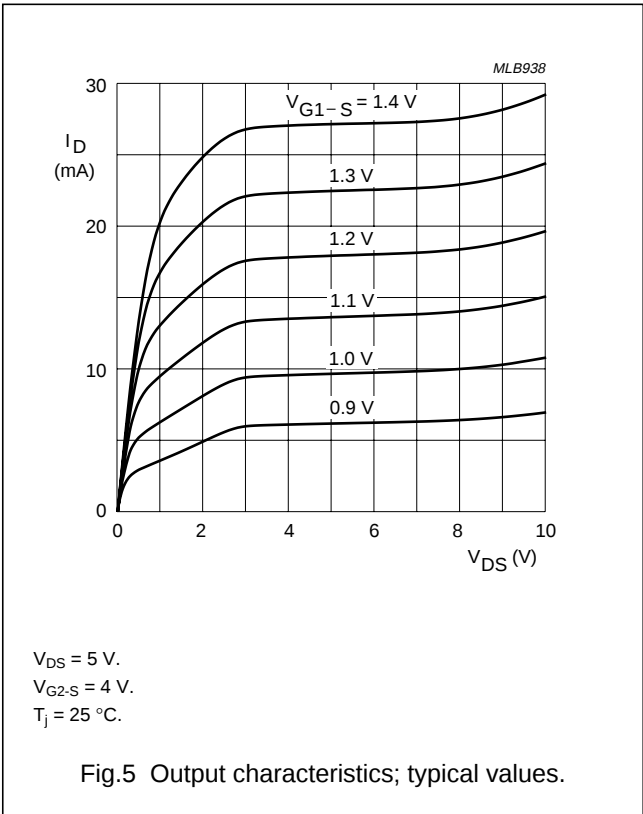
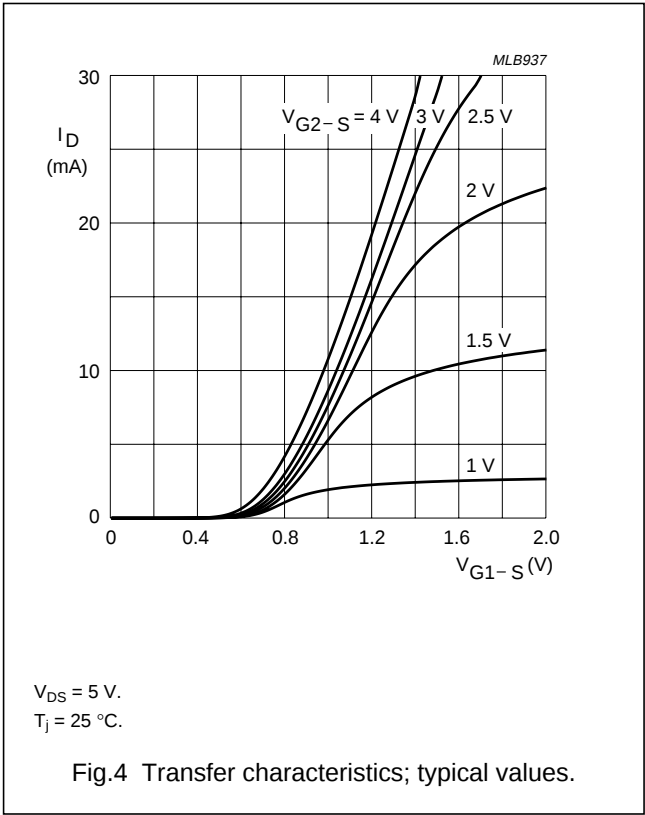
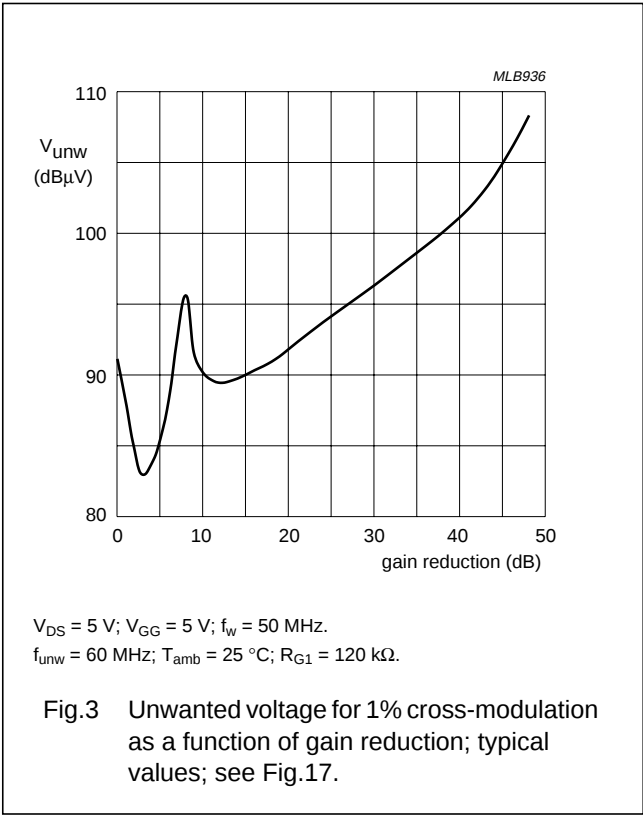
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\ ^\circ\text{C}$; $V_{DS} = 5\ \text{V}$; $V_{G2-S} = 4\ \text{V}$; $I_D = 15\ \text{mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\ ^\circ\text{C}$	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\ \text{MHz}$	–	3.6	4.3	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\ \text{MHz}$	–	2.3	3	pF
C_{os}	drain-source capacitance	$f = 1\ \text{MHz}$	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	$f = 1\ \text{MHz}$	–	30	50	fF
F	noise figure	$f = 800\ \text{MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB

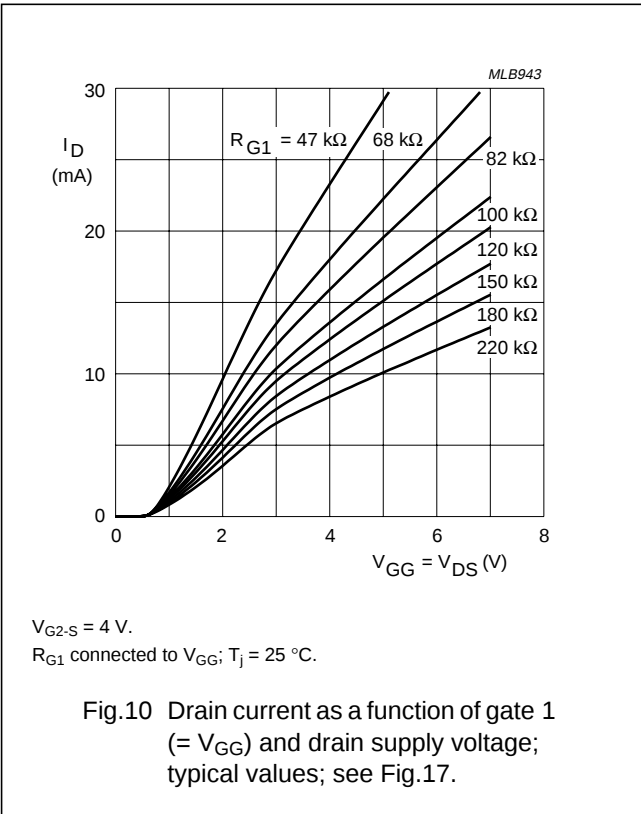
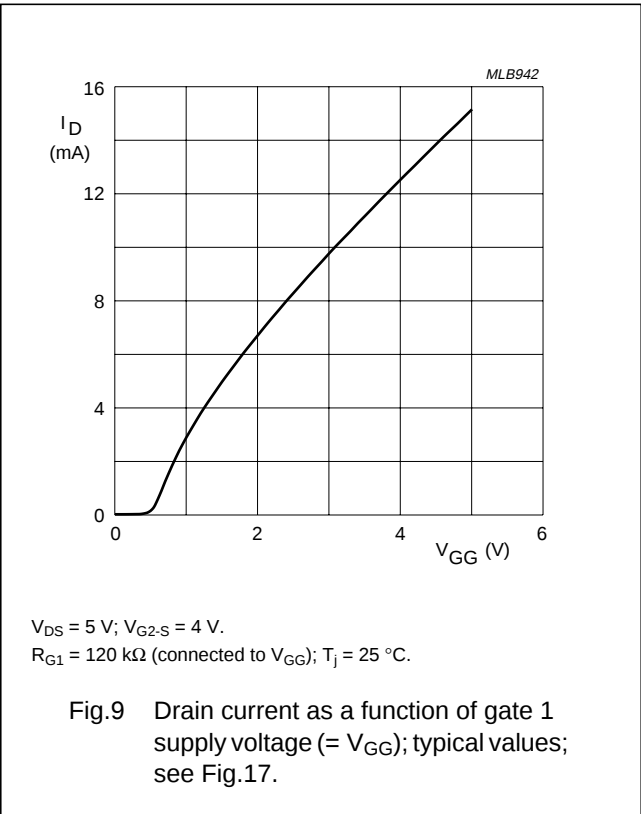
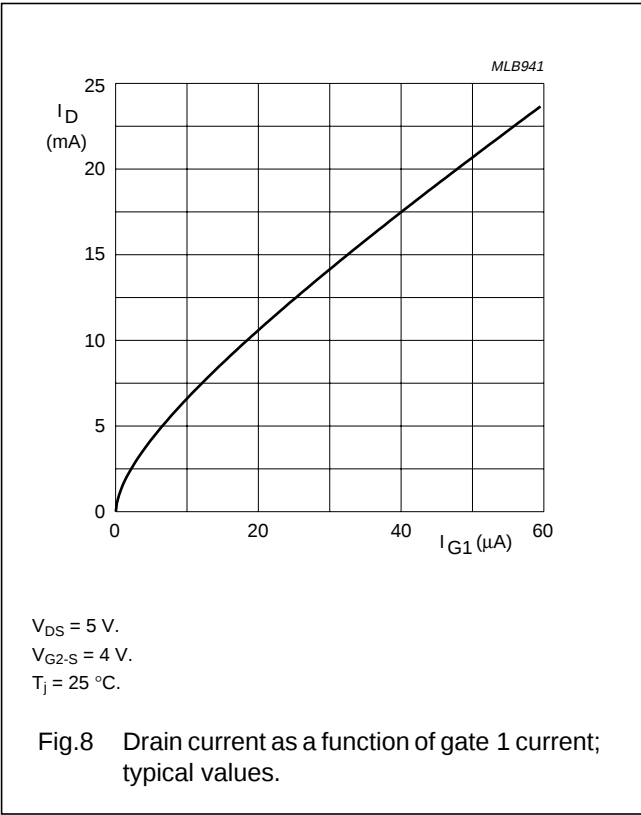
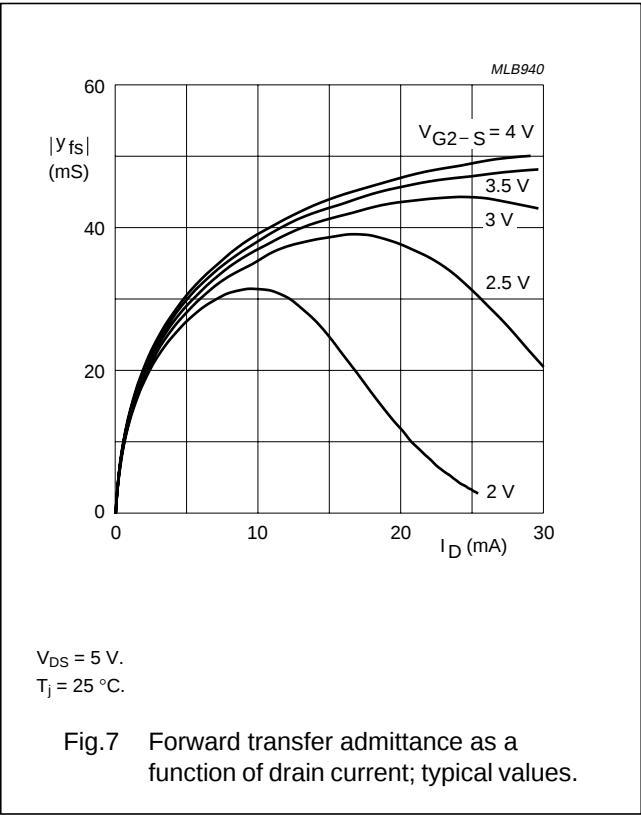
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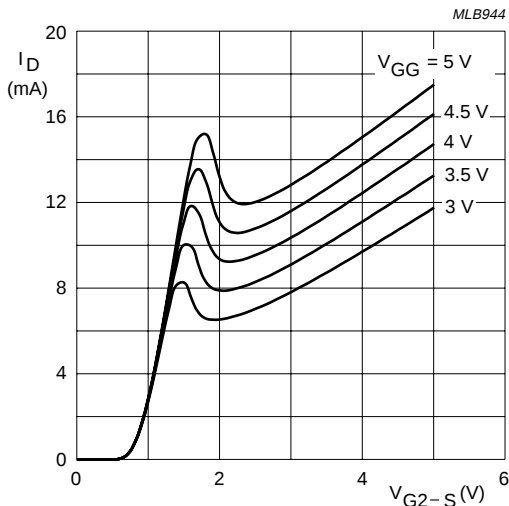
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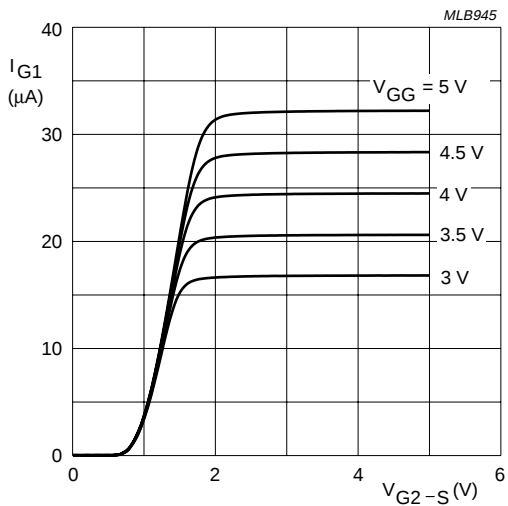
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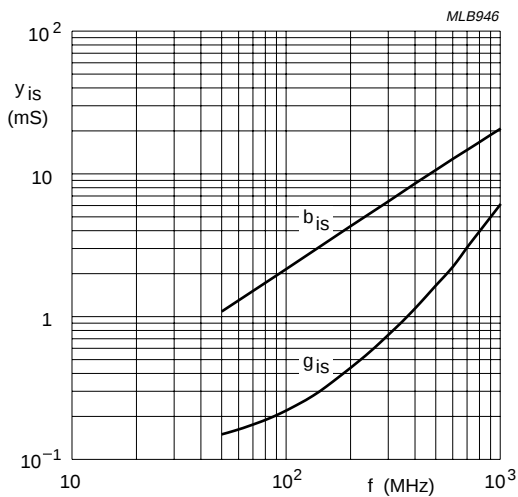
$V_{DS} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}).

Fig.11 Drain current as a function of gate 2 voltage; typical values; see Fig.17.



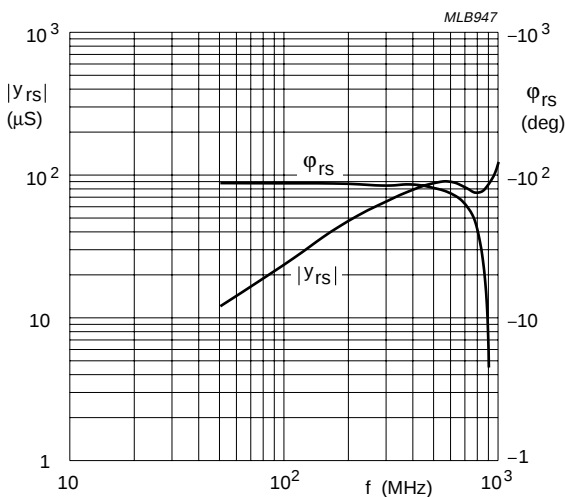
$V_{DS} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}).

Fig.12 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.17.



$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.13 Input admittance as a function of frequency; typical values.

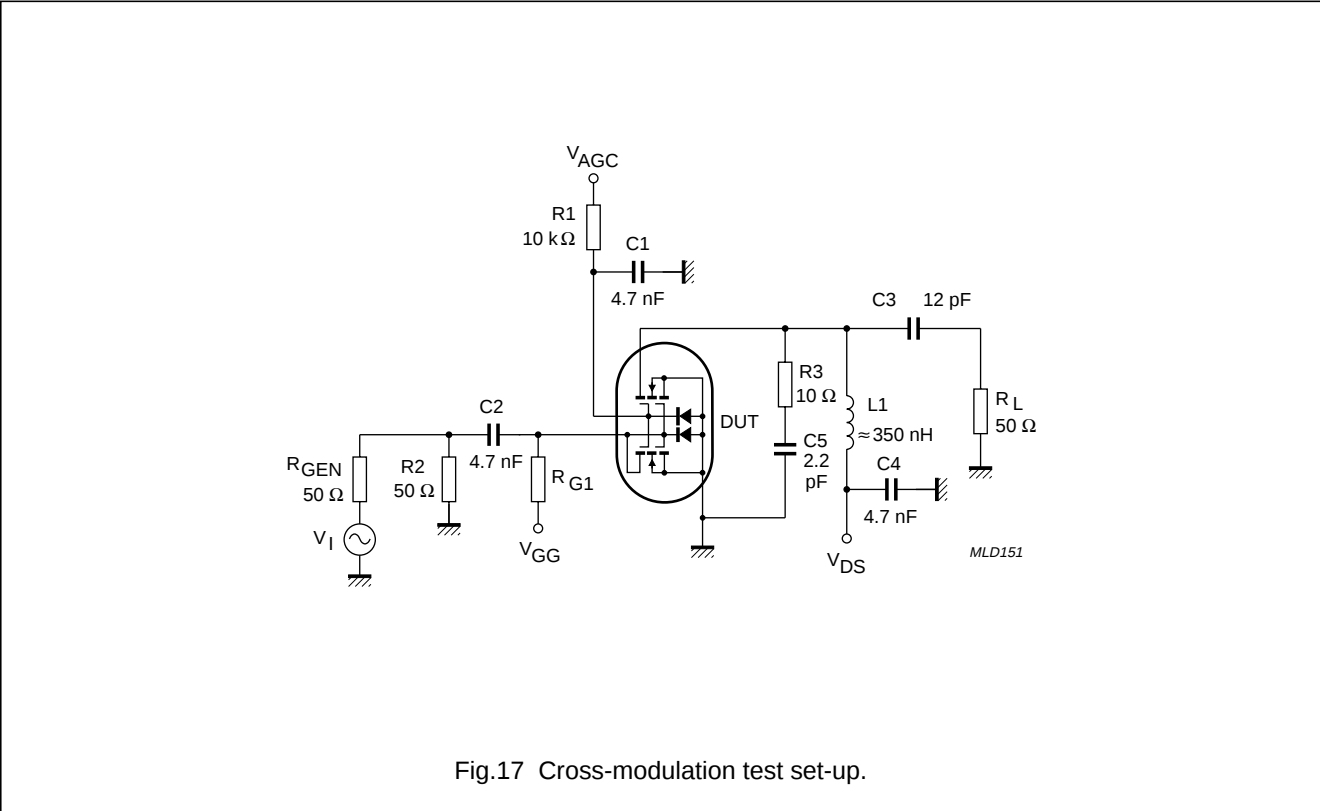
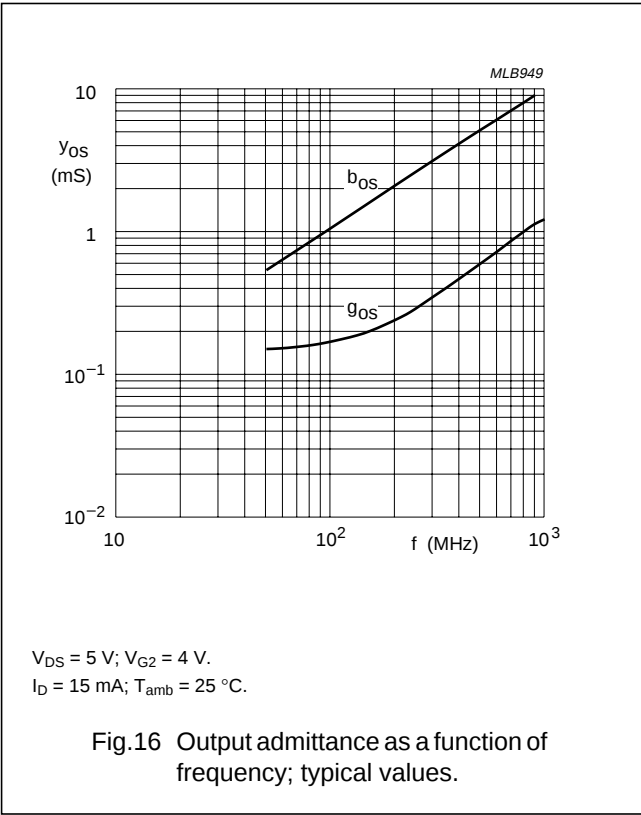
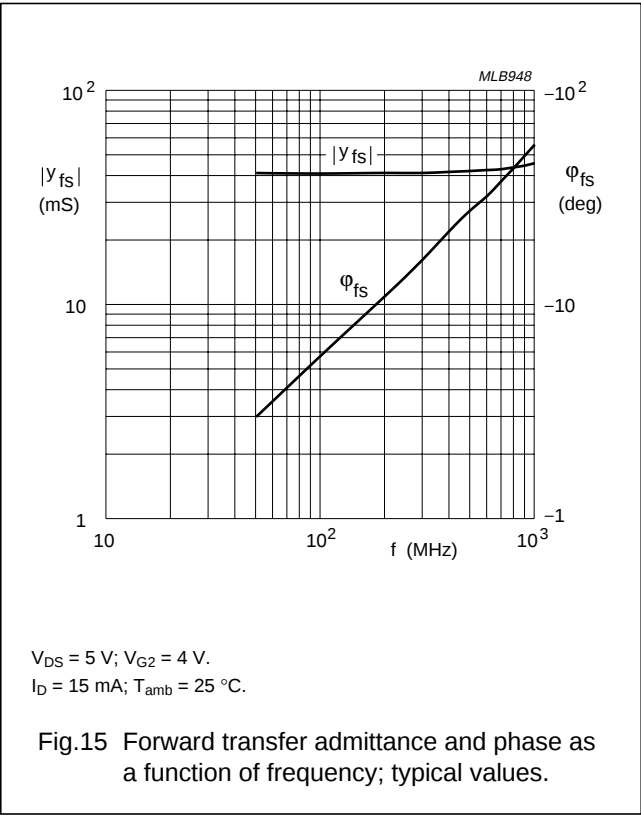


$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.

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Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	−6.4	4.064	172.3	0.001	86.9	0.985	−3.2
100	0.978	−12.6	3.997	164.9	0.002	82.7	0.982	−6.4
200	0.957	−25.0	3.886	150.8	0.005	74.3	0.973	−12.6
300	0.931	−36.5	3.682	137.3	0.006	68.9	0.960	−18.6
400	0.899	−47.6	3.484	123.8	0.007	59.6	0.947	−24.2
500	0.868	−57.4	3.260	111.7	0.007	57.9	0.936	−29.6
600	0.848	−66.6	3.053	101.0	0.006	58.5	0.927	−34.8
700	0.816	−74.6	2.829	90.3	0.005	65.5	0.919	−39.8
800	0.792	−82.2	2.652	79.9	0.005	83.3	0.913	−44.6
900	0.772	−89.3	2.470	69.5	0.005	114.9	0.910	−49.5
1000	0.754	−95.6	2.328	59.5	0.006	138.7	0.909	−54.6

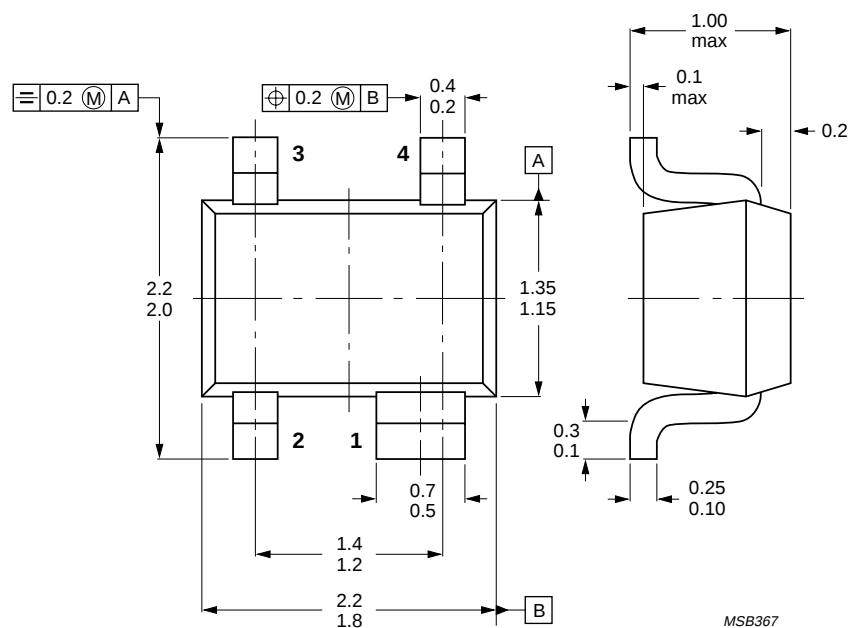
Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

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PACKAGE OUTLINE



Dimensions in mm.

Fig.18 SOT343R.

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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