SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

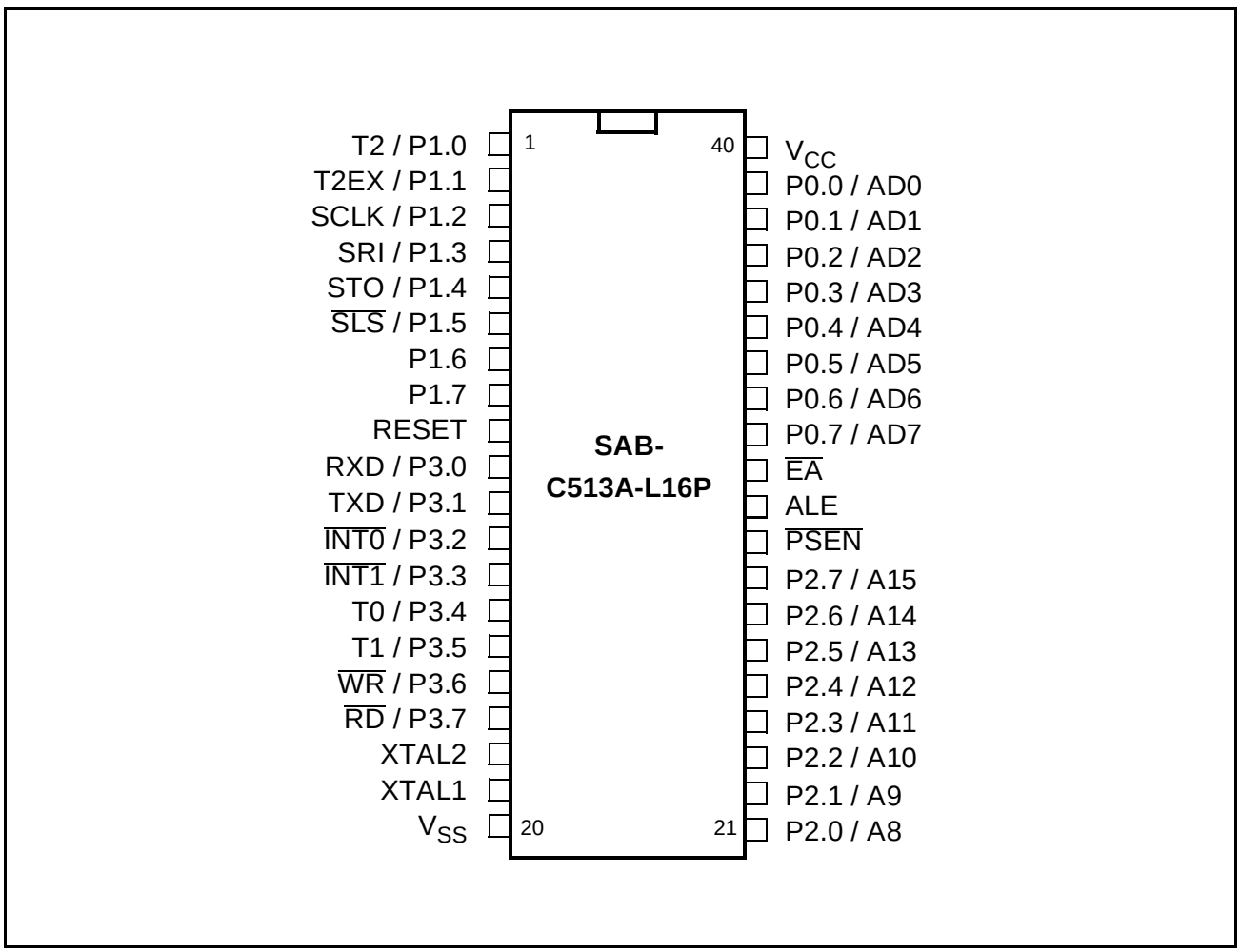
SAB-C513A-L16P

16 MHz Specification

Data Sheet Addendum 03.97

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS Microcontroller)
SAB-C513A-L16P	Q67120-C1039	P-DIP-40	for external memory, 16 MHz



Pin Configuration (Top view)

DC Characteristics

V_{CC} = 4.0 - 5.5V; V_{SS} = 0 V; T_A = 0 to + 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [8]	max.		
Power supply current:					
Active mode, 16 MHz [6]	I_{CC}	11	14.3	mA	V_{CC} = 5 V,[4]
Idle mode, 16 MHz [6]	I_{CC}	4.3	5.6	mA	V_{CC} = 5 V,[5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 … 5.5 V [3]

Notes:

[3] I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{CC}; all other pins are disconnected.

[4] I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

[5] I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

[6] $I_{CC\ Max}$ at other frequencies is given by:
Active mode : I_{CC} = 0.85 x f_{OSC} + 0.72
Idle mode : I_{CC} = 0.34 x f_{OSC} + 0.15
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

[8] The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

AC Characteristics

V_{CC} = 4.0 - 5.5V; V_{SS} = 0 V; T_A = 0 to + 70 °C

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	85	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	33	–	$t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX}	28	–	$t_{CLCL} - 35$	–	ns
ALE low to valid instr in	t_{LLIV}	–	150	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	38	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	153	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	88	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ}*)	–	43	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV}*)	55	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	198	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C513 microcontroller to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	275	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	275	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	90	–	$2t_{CLCL} - 35$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	148	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	55	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	350	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	398	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	138	238	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	120	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	23	103	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	13	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	288	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

SSC Interface Characteristics

Parameter	Symbol	Limit Values				Unit
		13.5 MHz Clock		16 MHz Clock		
		min.	max.	min.		
Clock Cycle Time : Master Mode Slave Mode	t_{SCLK} t_{SCLK}	592 530	– –	500 450	– –	ns ns
Clock high time	t_{SCH}	230	–	200	–	ns
Clock low time	t_{SCL}	230	–	200	–	ns
Data output delay	t_{D}	–	100	–	100	ns
Data output hold	t_{HO}	0	–	0	–	ns
Data input setup	t_{S}	100	–	80	–	ns
Data input hold	t_{HI}	100	–	80	–	ns
TC bit set delay	t_{DTC}	–	16 t_{CLCL}	–	16 t_{CLCL}	ns

External Clock Characteristics

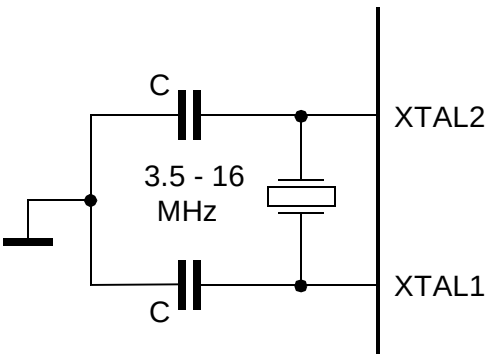
Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 16 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	62.5	285	ns
High time	t_{CHCX}	15	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	15	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	15	ns
Fall time	t_{CHCL}	–	15	ns

Reset Characteristics

Parameter	Symbol	Limit Values				Unit
		16 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 16 MHz		
		min.	max.	min.	max.	
RESET high pulse width (when CPU is running)	t_{RES}	1.5	–	24 t_{CLCL}	–	µs

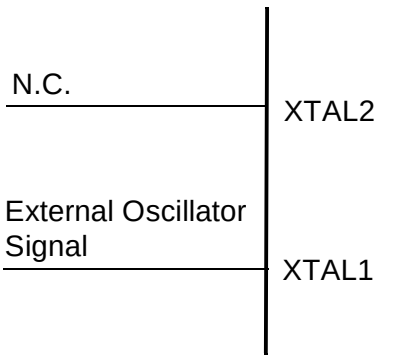
Recommended Oscillator Circuits

Crystal Oscillator Mode



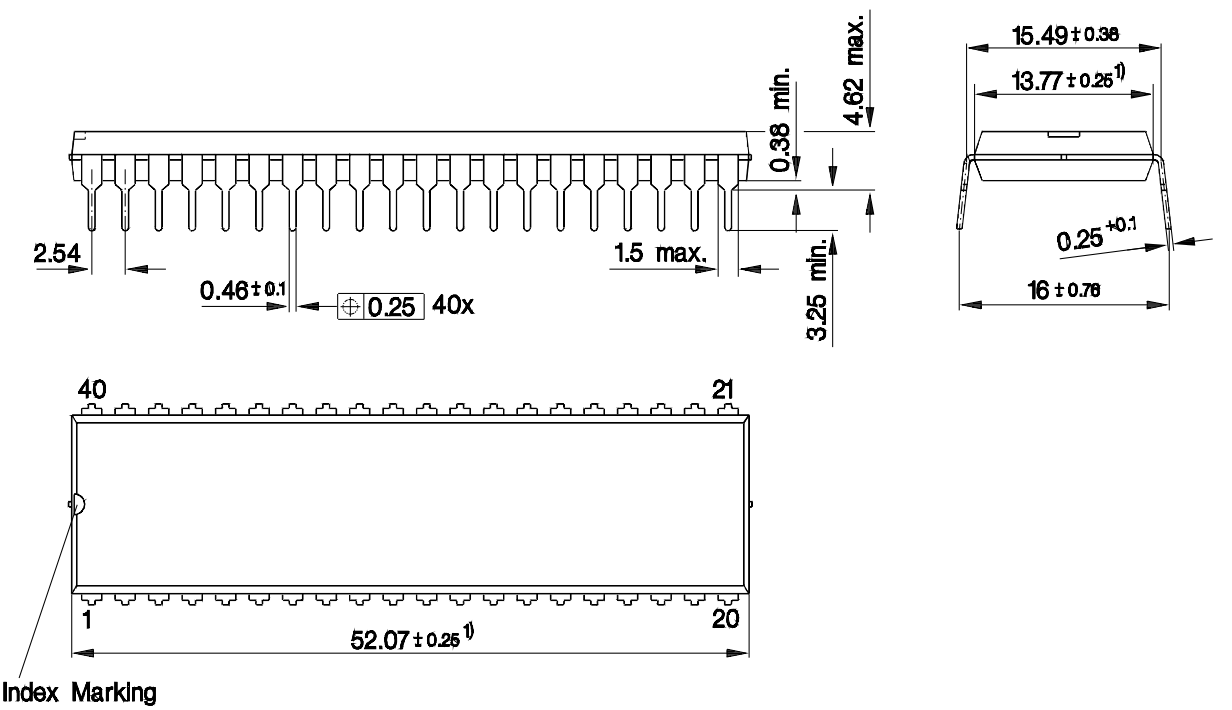
C = 20 pF ± 10 pF
(incl. stray capacitance)

Driving from External Source



Package Outline

Plastic Package, P-DIP-40-2
(Plastic Dual in-Line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side