BURR - BROWN®

DAC1220

20-Bit Low Power DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 20-BIT MONOTONICITY GUARANTEED OVER –40°C to +85°C
- LOW POWER: 2.5mW
- VOLTAGE OUTPUT
- SETTLING TIME: 2ms to 0.012%
- MAX LINEARITY ERROR: ±0.0015%
- ON-CHIP CALIBRATION

APPLICATIONS

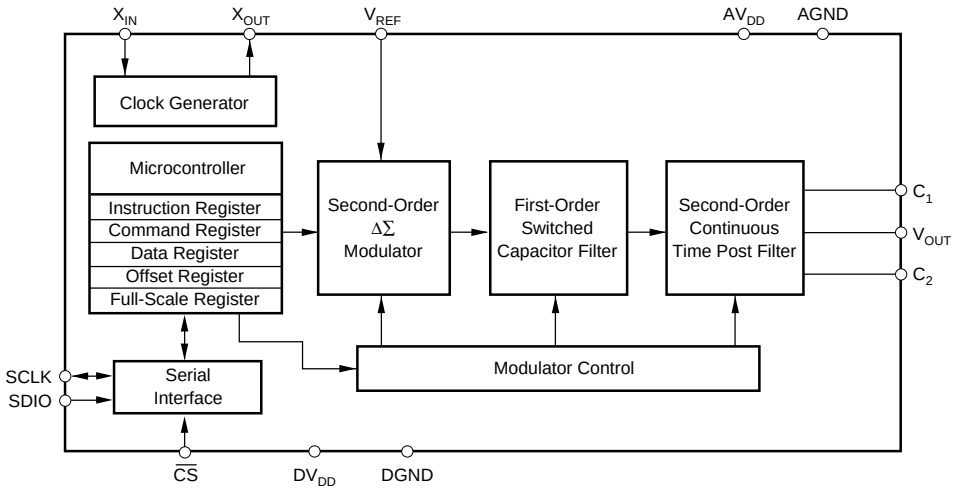
- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS

DESCRIPTION

The DAC1220 is a 20-bit digital-to-analog (D/A) converter offering 20-bit monotonic performance over the specified temperature range. It utilizes delta-sigma technology to achieve inherently linear 20-bit performance in a small package at very low power. The resolution of the device can be programmed to 20 bits for full-scale settling to 0.003% within 15ms typical or 16 bits for full-scale settling to 0.012% within 2ms max. The output range is 0V to two times the external reference voltage and on-chip calibration circuitry provides extremely low offset and gain error.

The DAC1220 features a synchronous serial interface that is SPI and Microwire compatible. In single converter applications, the serial interface can be accomplished with just two wires, allowing low cost isolation. For multiple converters, a third $\overline{CS}$ signal allows for selection of the appropriate D/A converter.

The DAC1220 has been designed for closed-loop control applications in the industrial process control market and high resolution applications in the test and measurement market. It is also ideal for remote applications, battery powered instruments and isolated systems. The DAC1220 is available in a 16-lead SSOP package.



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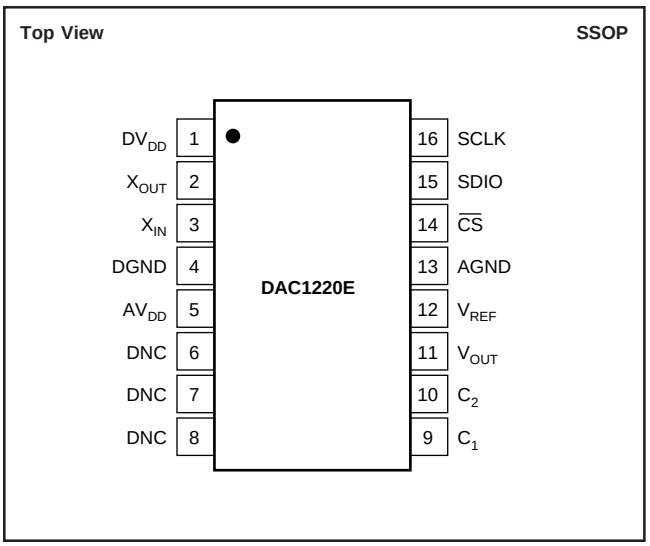
SPECIFICATIONS

All specifications T_{MIN} to T_{MAX}, AV_{DD} = DV_{DD} = +5V, f_{XIN} = 2.5MHz, V_{REF} = +2.5V, and 16-bit mode, unless otherwise noted.

PARAMETER	CONDITIONS	DAC1220E MIN	DAC1220E TYP	DAC1220E MAX	UNITS
ACCURACY					
Monotonicity		16			Bits
Monotonicity	20-Bit Mode	20			Bits
Linearity Error				±1(1)	LSB
Unipolar Offset Error(2)				±4	LSB
Unipolar Offset Error Drift(3)			1		ppm/°C
Bipolar Zero Offset Error(2)			±1		LSB
Bipolar Zero Offset Drift(3)			1		ppm/°C
Gain Error(2)				±10	LSB
Gain Error Drift(3)			2		ppm/°C
Power Supply Rejection Ratio			60		dB
ANALOG OUTPUT					
Output Voltage(4)		0		$2 \cdot V_{REF}$	V
Output Current				0.5	mA
Capacitive Load			500		pF
Short-Circuit Current			±20		mA
Short-Circuit Duration	GND or V_{DD}		Indefinite		
DYNAMIC PERFORMANCE					
Settling Time(5)	To ±0.012%		1.8	2	ms
	20-Bit Mode, to ±0.003%		15		ms
Output Noise Voltage	0.1Hz to 10Hz		1		µVrms
REFERENCE INPUT					
Input Voltage		2.25	2.5	2.75	V
Input Impedance			100		kΩ
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible CMOS		
Logic Levels (all except X_{IN})					
V_{IH}	I_{IH} = ±10µA	2.0		DV_{DD} +0.3	V
V_{IL}	I_{IL} = ±10µA	–0.3		0.8	V
V_{OH}	I_{OH} = –0.8mA	3.6			V
V_{OL}	I_{OL} = 1.6mA			0.4	V
X_{IN} Frequency Range (f_{XIN})		0.5		2.5	MHz
Data Format	User Programmable		Binary Two's Complement or Offset Binary		
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage		4.75		5.25	V
Supply Current					
Analog Current			360		µA
Digital Current			140		µA
Analog Current	20-Bit Mode		460		µA
Digital Current	20-Bit Mode		140		µA
Power Dissipation			2.5	3.5	mW
	20-Bit		3.0		mW
	Sleep Mode		0.45		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTES: (1) Valid from AGND + 20mV to AV_{DD} – 20mV, in the 16-bit mode. (2) Applies after calibration, in 16-bit mode. (3) Re-calibration can remove these errors. (4) Ideal output voltage, does not take into account gain and offset error. (5) Valid from AGND +20mV to AV_{DD} –20mV. Outside of this range, settling time may be twice the value indicated. For 16-bit mode, C_1 = 2.2nF, C_2 = 0.22nF; for 20-bit mode, C_1 = 10nF, C_2 = 3.3nF.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	DV_{DD}	Digital Supply, +5V nominal
2	X_{OUT}	System Clock Output (for Crystal)
3	X_{IN}	System Clock Input
4	DGND	Digital Ground
5	AV_{DD}	Analog Supply, +5V nominal
6	DNC	Do Not Connect
7	DNC	Do Not Connect
8	DNC	Do Not Connect
9	C_1	Filter Capacitor, see text.
10	C_2	Filter Capacitor, see text.
11	V_{OUT}	Analog Output Voltage
12	V_{REF}	Reference Input
13	AGND	Analog Ground
14	$\overline{CS}$	Chip Select Input
15	SDIO	Serial Data Input/Output
16	SCLK	Clock Input for Serial Data Transfer

ABSOLUTE MAXIMUM RATINGS[1]

AV_{DD} to DV_{DD} ..... ±0.3V
AV_{DD} to AGND ..... –0.3V to 6V
DV_{DD} to DGND ..... –0.3V to 6V
AGND to DGND ..... ±0.3V
V_{REF} Voltage to AGND ..... 2.0V to 3.0V
Digital Input Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
Digital Output Voltage to DGND ..... –0.3V to DV_{DD} + 0.3V
Package Power Dissipation ..... $(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_{JMAX}) ..... +150°C
Thermal Resistance, θ_{JA}
16-Lead SSOP ..... 200°C/W
Lead Temperature (soldering, 10s) ..... +300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

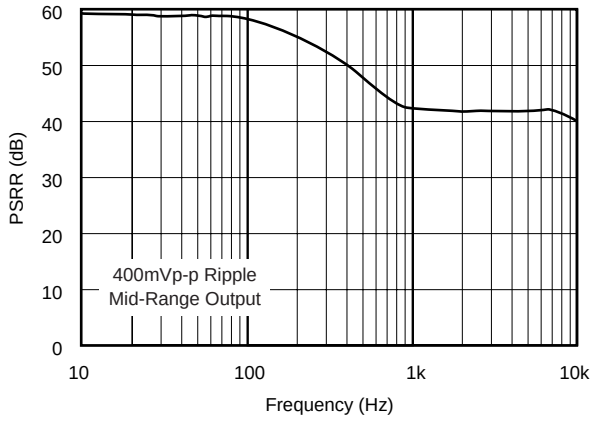
PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[2]	TRANSPORT MEDIA
DAC1220E	±1	16-Lead SSOP	322	–40°C to +85°C	DAC1220E/250	Tape and Reel
"	"	"	"	"	DAC1220E/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC1220E/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

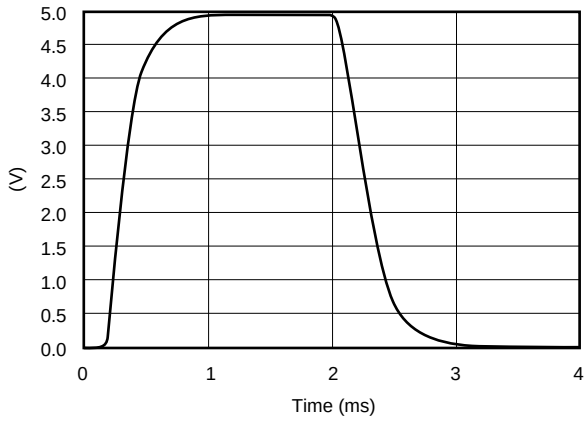
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, AV_{DD} = DV_{DD} = +5.0V, f_{XIN} = 2.5MHz, V_{REF} = 2.5V, C_1 = 2.2nF and C_2 = 0.22nF, calibrated mode, unless otherwise specified.

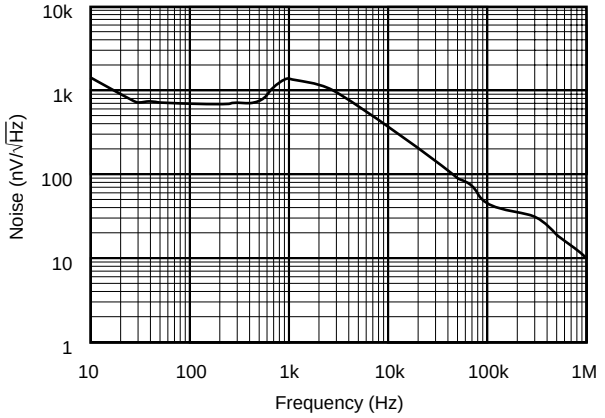
POWER SUPPLY REJECTION RATIO vs FREQUENCY



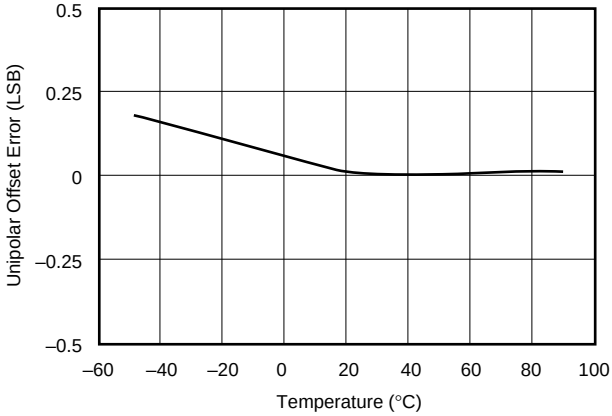
LARGE-SIGNAL SETTLING TIME



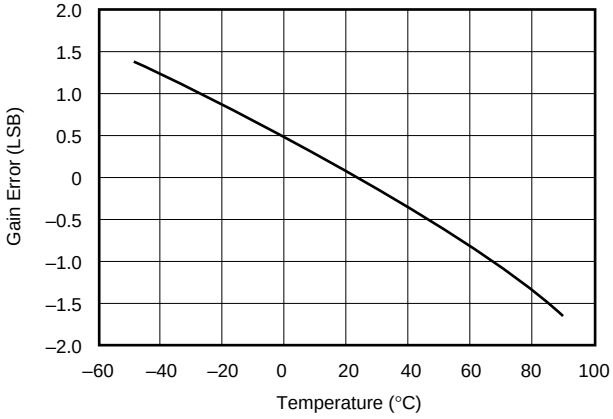
OUTPUT NOISE VOLTAGE vs FREQUENCY



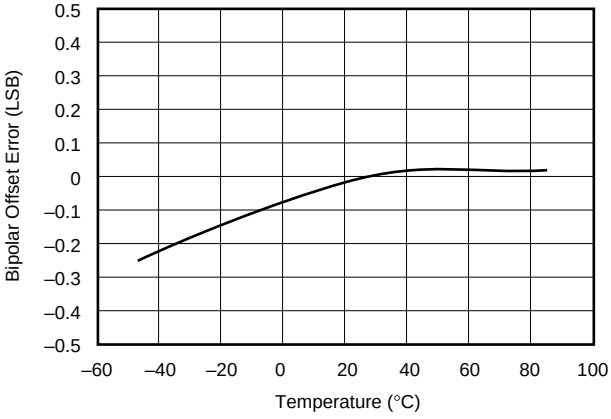
UNIPOLAR OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



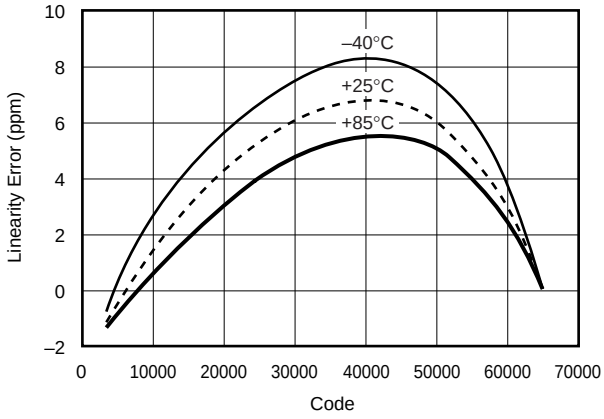
BIPOLAR OFFSET ERROR vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, AV_{DD} = DV_{DD} = +5.0V, f_{XIN} = 2.5MHz, V_{REF} = 2.5V, C_1 = 2.2nF and C_2 = 0.22nF, calibrated mode, unless otherwise specified.

LINEARITY ERROR vs CODE



THEORY OF OPERATION

The DAC1220 is precision, high dynamic range, self-calibrating, 20-bit, delta-sigma D/A converter. It contains a second-order delta-sigma modulator, a first-order switched capacitor filter, a second-order continuous time post filter, a microcontroller including the Instruction, Command and Calibration registers, a serial interface, and a clock generator circuit.

The design topology provides low system noise and good power supply rejection. The modulator frequency of the delta-sigma D/A converter is controlled by the system clock. With a 2.5MHz system clock, the delta-sigma D/A converter operates at 312.5kHz.

The DAC1220 also includes complete onboard calibration that can correct for internal offset and gain errors. The calibration registers are fully readable and writable. This feature allows for system calibration. The various settings, modes, and registers of the DAC1220 are read or written via a synchronous serial interface. This interface operates as an externally clocked interface.

The high resolution and flexibility of the DAC1220 allows this converter to fill a wide variety of D/A conversion tasks. In order to ensure that a particular configuration will meet the design goals, there are several important items which must be considered. These include (but are certainly not limited to) the needed resolution, required linearity, desired settling time, and power consumption goal. The remainder of this data sheet discusses the operation of the DAC1220 in detail.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Differential Nonlinearity Error—The differential nonlinearity error is the difference between an actual step width and the ideal value of 1LSB. If the step width is exactly 1LSB, then the differential nonlinearity error is zero. A differential nonlinearity specification of 1LSB guarantees monotonicity.

Drift—The drift is the change in a parameter over temperature.

Full-Scale Range (FSR)—The full-scale range of the DAC1220 is defined as the digital code which produces the positive full-scale analog output. For example, when the converter is configured with a 2.5V reference and a gain setting of 2, the full-scale range is [2.5V (positive full scale) • 2] = 5V.

Gain Error—The gain error is the difference between gain points on the transfer function after the offset error has been corrected to zero. This error represents a difference in the slope of the actual and ideal transfer functions and as such, corresponds to the same percentage error in each step. Gain error may be adjusted to zero externally.

Integral Nonlinearity—The integral nonlinearity error is the deviation of the values on the actual transfer function calculated from data end points. The name “integral nonlinearity” derives from the fact that the summation of the differential nonlinearities, from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

Least Significant Bit (LSB) Weight—This is the theoretical amount of voltage that the voltage at the analog output would change with a change in the digital input code of 1LSB.

Main Controller—A generic term for the external microcontroller, microprocessor, or digital signal processor which is controlling the operation of the DAC1220 and writing input data.

Monotonicity—Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes.

Offset Error—The offset error is the difference between the expected and actual offset points when the digital input is zero.

Settling Time—The settling time is the time is takes the output to settle to its new value after the digital code has been changed. It is specified for a worst-case change of all digital zeros to all digital ones and vice versa and is measured from AGND + 20mV to AV_{DD} – 20mV.

Voltage Span—This is the magnitude of the typical analog output voltage range. For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 2, the output voltage span is 5.0V.

f_{XIN}—The frequency of the crystal oscillator or CMOS-compatible input signal at the X_{IN} input of the DAC1220.

ANALOG OPERATION

The system clock is divided down to provide the sample clock for the modulator. The sample clock is used by the modulator to convert the multi-bit digital input into a one-bit digital output stream. The use of a 1-bit DAC provides inherent linearity. The digital output stream is then converted into an analog signal via the 1-bit DAC and then filtered by the 1st-order switched capacitor filter.

The output of the switched-capacitor filter feeds into the continuous time filter. The continuous time filter uses external capacitors connected between the C_1, C_2, V_{REF}, and V_{OUT} pins to adjust the settling time. The connections for the capacitors are shown in Figure 1 (C_1 connects between the V_{REF} and C_1 pins, and C_2 connects between the V_{OUT} and C_2 pins).

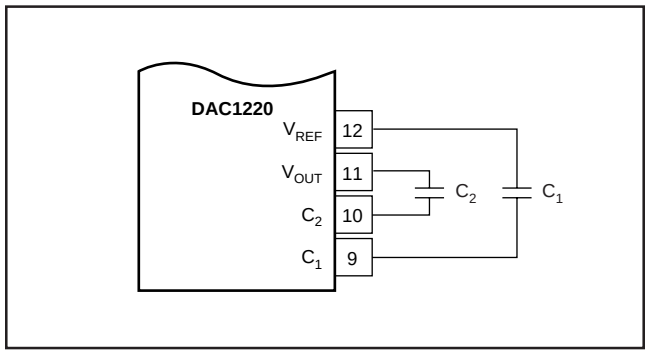


FIGURE 1. Capacitor Connections for Settling Time.

CAPACITOR	16-BIT MODE	20-BIT MODE
C_1	2.2nF	10nF
C_2	0.22nF	3.3nF

TABLE I. Capacitor Values.

CALIBRATION

The DAC1220 offers a self-calibration mode which automatically calibrates the output offset and gain. The calibration is performed once and then normal operation is resumed. In general, calibration is recommended immediately after power-on and whenever there is a "significant" change in the operating environment. The amount of change which should cause a re-calibration is dependent on the application. Where high accuracy is important, re-calibration should be done on changes in temperature and power supply.

After a calibration has been accomplished, the Offset Calibration Register (OCR) and the Full-Scale Calibration Register (FCR) contain the results of the calibration. The data in these registers are accurate to the effective resolution of the DAC1220's mode of operation during the calibration.

The calibration registers can also be used to provide system offset and gain corrections separate from those computed by the DAC1220. For example, these might be burned into E^2PROM during final product testing. On power on, the main controller would load these values into the calibration registers. A further possibility is a look-up table based on the current temperature.

Note that the values in the calibration registers will vary from configuration-to-configuration and from part-to-part. There is no method of reliably computing what a particular calibration register should be to correct for a given amount of system error.

Self-Calibration

A self-calibration is performed after the bits "01" have been written to the Command Register Operation Mode bits (MD1 through MD0) and a "1" has been written to the Command Register sample-and-hold bit (SH). This initiates a self-calibration on the next clock cycle. The self-calibration starts with the OCR being cleared. The offset correction code is determined by a repeated sequence of auto-zeroing the calibration comparator to the offset reference and then comparing the DAC output to the offset reference value. The end result is then averaged, Binary Two's Complement adjusted, and placed in the OCR. The gain correction is done in a similar fashion except the correction is done against V_{REF} to eliminate common-mode errors. The FCR result represents the gain code and is not Binary Two's Complement adjusted.

The calibration function takes between 300ms and 500ms to complete. Once calibration is initiated, further writing of register bits is disabled until calibration completes. The status of calibration can be verified by reading the status of the Command Register Operation Mode bits (MD1 through MD0). These bits will return to normal mode "00" when calibration is complete.

Self-calibration can be done with the output isolated or connected. This is done by setting (output connected) or clearing (output isolated) the CALPIN bit in the CMR register. The load at the output affects the calibration accuracy. If the load sinks excessive current, the calibration will be out-of-specification.

Output Mode

The DAC1220 can operate in either 16-bit mode or 20-bit mode. The mode is determined by setting (20-bit) or clearing (16-bit) the RES bit in the CMR register.

The output of the DAC1220 can be synchronously reset. By setting the CLR bit in the CMR, the data input register is cleared to zero. This will result in an output of 0V in unipolar mode or V_{REF} in bipolar mode.

The settling time is determined by the DISF, RES, and ADPT bits of the CMR register. By clearing the DISF bit, the enhanced settling filter is disabled. The ADPT bit of the CMR determines whether the data step controls activation of fast settling. By clearing this bit, the adaptive filter is disabled which enables fast settling.

The SH bit of the CMR register determines if C_2 is internally connected to V_{REF}. By clearing the SH bit, C_2 is disconnected from V_{REF}.

The CRST bit of the CMR register can be used to reset the offset and calibration registers. By setting the CRST bit, the contents of the calibration register are reset to 0.

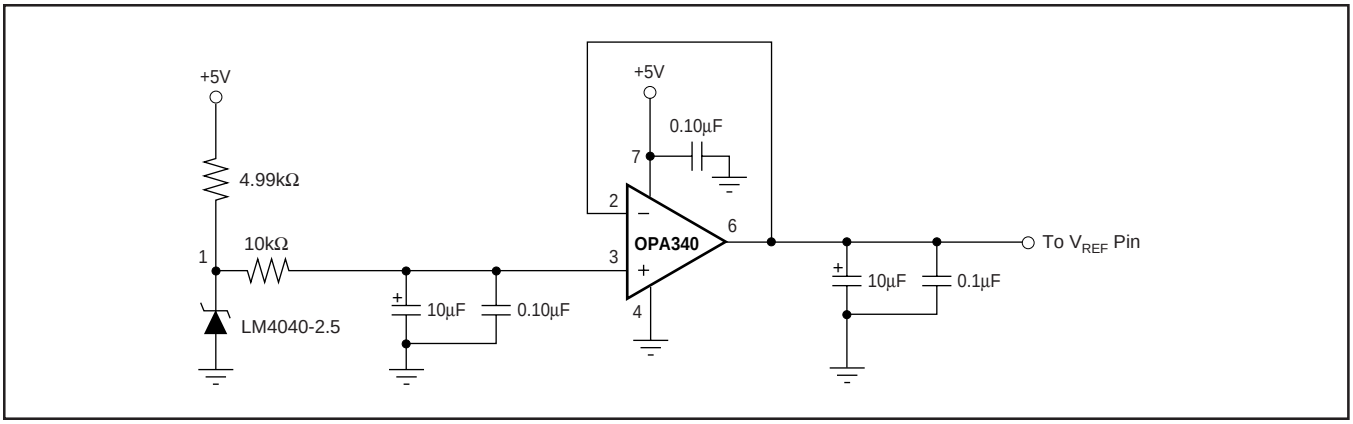


FIGURE 2. Recommended External Voltage Reference Circuit for Best Low Noise Operation with the DAC1220.

REFERENCE INPUT

The reference input voltage of 2.5V can be directly connected to V_{REF}. Higher reference voltages will cause the full-scale range to increase up to the supply voltage while the internal circuit noise of the converter remains approximately the same.

The recommended reference circuit for the DAC1220 is shown in Figure 2.

DIGITAL OPERATION

SYSTEM CONFIGURATION

The DAC1220 supports Serial Peripheral Interface (SPI) and Synchronous Serial Interface (SSI) interfaces. Via the serial interface, the DAC1220 is controlled by 8-bit instruction codes and 16-bit command codes. Two kinds of protocol are available for the serial interface: SPI and SSI. SPI is a byte-based, 2-wire serial interface. SSI is a popular 3-wire interface. The serial input is externally clocked in both protocols.

The Microcontroller (MC) consists of an ALU and a register bank. The MC has three states: power-on reset, calibration, and normal operation. In the power-on reset state, the MC resets all the registers to their default states. In the calibration state, the MC performs offset and gain self-calibration. In the normal state, the MC performs D/A conversions.

The DAC1220 has five internal registers, as shown in Table II. Two of these, the Instruction Register (INSR) and the Command Register (CMR), control the operation of the converter. The Instruction register utilizes an 8-bit instruction code to control the serial interface to determine whether the next operation is either a read or a write, to control the word length and to select the appropriate register to read/write. Communication with the DAC1220 is controlled via the INSR. Under normal operation, the INSR is written as the first part of each serial communication. The instruction that is sent determines what type of communication will occur next. It is not possible to read the INSR. The Command register has a 16-bit command code to set up the DAC1220 operation mode, resolution mode, settling mode and data format. The Data Input Register (DIR) contains the value for the next conversion. The Offset and Full-Scale Calibration Registers (OCR and FCR) contain data used for correcting the internal conversion value after it is placed into the DIR. The data in these two registers may be the result of a calibration routine, or they may be values which have been written directly via the serial interface.

INSR	Instruction Register	8 Bits
DIR	Data Input Register	24 Bits
CMR	Command Register	16 Bits
OCR	Offset Calibration Register	24 Bits
FCR	Full-Scale Calibration Register	24 Bits

TABLE II. DAC1220 Registers.

Instruction Register (INSR)

Each serial communication starts with the 8 bits of the INSR being sent to the DAC1220. This directs the remainder of the communication cycle, which consists of n bytes being read from or written to the DAC1220. The read/write bit, the number of bytes n, and the starting register address are defined, as shown in Table III. When the n bytes have been transferred, the INSR is complete. A new communication cycle is initiated by sending a new INSR (under restrictions outlined in the Interfacing section).

MSB							LSB
R/$\overline{W}$	MB1	MB0	0	A3	A3	A1	A0

TABLE III. Instruction Register.

NOTE: INSR is a write-only register with the MSB (most significant byte and bit) be written first, independent of the BD bit.

R/$\overline{W}$ (Read/Write) Bit—For a write operation to occur, this bit of the INSR must be 0. For a read, this bit must be 1, as follows:

R/$\overline{W}$	
0	Write
1	Read

MB1, MB0 (Multiple Bytes) Bits—These two bits are used to control the word length (number of bytes) of the read or write operation, as follows:

MB1	MB0	
0	0	1 Byte
0	1	2 Bytes
1	0	3 Bytes
1	1	4 Bytes

A3 - A0 (Address) Bits—These four bits select the beginning register location which will be read from or written to, as shown in Table IV. Each subsequent byte will be read from or written to the next higher location. (If the BD bit in the Command register is set, each subsequent byte will be read from the next lower location. This bit does not affect the write operation.) If the next location is not defined in Table IV, the results are unknown. Reading or writing continues until the number of bytes specified by MB1 and MB0 have been transferred.

A3	A2	A1	A0	
0	0	0	0	Data Input Register Byte 2
0	0	0	1	Data Input Register Byte 1
0	0	1	0	Data Input Register Byte 0
0	0	1	1	Reserved
0	1	0	0	Command Register Byte 1
0	1	0	1	Command Register Byte 0
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Offset Cal Register Byte 2
1	0	0	1	Offset Cal Register Byte 1
1	0	1	0	Offset Cal Register Byte 0
1	0	1	1	Reserved
1	1	0	0	Full-Scale Cal Register Byte 2
1	1	0	1	Full-Scale Cal Reigster Byte 1
1	1	1	0	Full-Scale Cal Register Byte 0
1	1	1	1	Reserved

TABLE IV. A3 - A0 Addressing.

Command Register (CMR)

The CMR controls all of the functionality of the DAC1220. The new configuration takes effect on the negative transition of SCLK for the last bit in each byte of data being written to the Command register. The organization of the CMR is comprised of 16 bits of information in 2 bytes of 8 bits each.

MSB			Byte 1				
ADPT	CALPIN	SH	0	1	0	CRST	X
			Byte 0				**LSB**
RES	CLR	DF	DISF	BD	MSB	MD1	MD0

NOTE: In order to obtain optimal performance, the default bit states for the Command Register should be used (refer to Table VI). The only exception is the SH bit—the default bit state is 0, however, the bit should be set to 1 for optimal performance.

TABLE V. Command Register.

RES (Resolution) Bit—The Resolution bit selects either 16-bit or 20-bit resolution.

RES		
0	16-Bit	Default
1	20-Bit	

CLR (Clear) Bit—The clear bit synchronously resets the data input register to zero. The analog output will be based on the DF bit (1 = unipolar for 0V output, 0 = bipolar for V_{REF} output).

CLR		
0	OFF	Default
1	ON	

DF (Data Format) Bit—The DF bit controls the format of the input data, either Binary Two's Complement (bipolar) or Offset Binary (unipolar), as follows:

DF		
0	Binary Two's Complement (bipolar)	Default
1	Offset Binary (unipolar)	

DISF (Disable Enhanced Settling of Filter) Bit—The disable enhanced settling of filter bit disables the settling filter. The time for settling is dependent upon this bit setting, the RES bit, and the ADPT bit.

DISF		
0	Disabled	Default
1	Enabled	

BD (Byte Order) Bit—The BD bit controls the order in which bytes of data are read, either most significant byte first or least significant byte first, as follows:

BD		
0	Byte Access from MSB Byte to LSB Byte	Default
1	Byte Access From LSB Byte from LSB Byte to MSB Byte	

MSB (Bit Order) Bit—The MSB bit controls the order in which bits within a byte of data are read, either most significant bit first or least significant bit first, as follows:

MSB		
0	MSB-First	Default
1	LSB-First	

MD1 - MD0 (Operating Mode) Bits—The Operating Mode bits control the calibration functions of the DAC1220. In operation, the Normal mode is used to perform conversions. The Self-Calibration mode is a one-step calibration sequence that calibrates both the offset and full scale.

MD1	MD0	
0	0	Normal Mode
0	1	Self-Cal
1	0	Sleep
1	1	X

ADPT (Adaptive Filter) Bit—The Adaptive Filter bit determines if the adaptive filter is enabled or disabled. Disabling this bit will always do fast settling.

ADPT		
0	Enabled	Default
1	Disabled	

CALPIN (Calibration Pin) Bit—The Calibration Pin bit determines if the output is isolated or connected during calibration.

CALPIN		
0	Output Isolated	Default
1	Output Connected	

SH (Sample/Hold) Bit —The Sample-and-Hold bit determines if C_2 is internally connected to V_{REF}. For best performance, it is recommended to set this bit to 1.

SH		
0	Disconnected	Default
1	Connected	Recommended

CRST (Calibration Reset) Bit—The CRST bit resets the offset and full-scale calibration registers.

CRST		
0	OFF	Default
1	Reset	

MSB			Byte 1				
0	0	0	0(1)	1(1)	0(1)	0	0(1)
			Byte 0				LSB
0	0	0	0	0	0	0	0

NOTE: (1) These bit locations are readable and writable. Modifying these bit values will reduce the performance of the device.

TABLE VI. Command Register Default Condition.

Offset Calibration Register (OCR)

The OCR is a 24-bit register which contains the offset correction factor that is applied to the digital input before it is transferred to the modulator. The contents of this register will be the result of the self-calibration. The calibration is very precise.

The OCR is both readable and writeable via the serial interface. For applications requiring an accurate system calibration, a system calibration can be performed, the results averaged, and a more precise system offset calibration value written back to the OCR.

The actual OCR value will change from part to part and with configuration, temperature, and power supply. Thus, the actual OCR value for any arbitrary situation cannot be accurately predicted. That is, a given system offset could not be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the OCR.

In addition, be aware that the contents of the OCR are not used to directly correct the digital input. Rather, the correction is a function of the OCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the OCR. Consult the Calibration section for more details.

MSB			Byte 2				
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
			Byte 1				
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR9	OCR8
			Byte 0				LSB
OCR7	OCR6	OCR5	OCR4	OCR3	OCR2	OCR1	OCR0

TABLE VII. Offset Calibration Register.

Full-Scale Calibration Register (FCR)

The FCR is a 24-bit register which contains the full-scale correction factor that is applied to the digital input before it is transferred to the modulator. The contents of this register will be the result of a self-calibration.

The FCR is both readable and writable via the serial interface. For applications requiring an accurate system calibration, a system calibration can be performed, the results averaged, and a more precise system offset calibration value written back to the FCR.

The actual FCR value will change from part to part and with configuration, temperature, and power supply. Thus, the actual FCR value for any arbitrary situation cannot be accurately predicted. That is, a given system full-scale error cannot be corrected simply by measuring the error externally, computing a correction factor, and writing that value to the FCR.

In addition, be aware that the contents of the FCR are not used to directly correct the digital input. Rather, the correction is a function of the FCR value. This function is linear and two known points can be used as a basis for interpolating intermediate values for the FCR. Consult the Calibration

section for more details. The contents of the FCR are in unsigned binary format. This is not affected by the DF bit in the Command register.

MSB			Byte 2				
FCR23	FCR22	FCR21	FCR20	FCR19	FCR18	FCR17	FCR16
			Byte 1				
FCR15	FCR14	FCR13	FCR12	FCR11	FCR10	FCR9	FCR8
			Byte 0				LSB
FCR7	FCR6	FCR5	FCR4	FCR3	FCR2	FCR1	FCR0

TABLE VIII. Full-Scale Calibration Register.

Data Input Register (DIR)

The DIR is a 24-bit register which contains the digital input value (see Table IX). The register is latched on the falling edge of the LSB. The contents of the DIR are then loaded into the modulator. In the 16-bit mode, DIR23 through DIR8 are used to represent the 16-bit value. Therefore, the register data is latched on the falling edge of DIR8. In 20-bit mode, DIR23 through DIR4 are used to represent the 20-bit value. Therefore, the register data is latched on the falling edge of DIR4. The contents of the DIR Register can be Binary Two's Complement (bipolar mode) or Offset Binary (unipolar mode).

MSB			Byte 2				
DIR23	DIR22	DIR21	DIR20	DIR19	DIR18	DIR17	DIR16
			Byte 1				
DIR15	DIR14	DIR13	DIR12	DIR11	DIR10	DIR9	DIR8
			Byte 0				LSB
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

TABLE IX. Data Input Register.

SLEEP MODE

The Sleep mode is entered after the bits 10 have been written to the Command Register Operation Mode bits (MD1 through MD0). This mode is exited by entering a new mode into the MD1 - MD0 bits.

To establish serial communication with the converter while it is in Sleep mode, one of the following procedures must be used: if $\overline{CS}$ is being used, simply taking $\overline{CS}$ LOW will enable serial communication to proceed normally. Additionally, if $\overline{CS}$ is not being used (tied LOW), simply sending a normal Instruction Register command will re-establish communication.

Once serial communication is resumed, the Sleep mode is exited by changing the MD1 - MD0 bits to any other mode. When a new mode (other than Sleep) has been entered, the DAC1220 will execute a very brief internal power-up sequence of the analog and digital circuitry. In addition, the settling of the external V_{REF} and other circuitry must be taken into account to determine the amount of time required to resume normal operation.

SERIAL INTERFACE

The DAC1220 includes a flexible serial interface which can be connected to microcontrollers and digital signal processors in a variety of ways. Along with this flexibility, there is also a good deal of complexity. This section describes the trade-offs between the different types of interfacing methods in a top-down approach—starting with the overall flow and control of serial data, moving to specific interface examples, and then providing information on various issues related to the serial interface.

The serial interface has two basic protocols which are SPI (Serial Peripheral Interface) and SSI (Synchronous Serial Interface).

Reset, Power-On Reset and Brown-Out

The DAC1220 contains an internal power-on reset circuit. If the power supply ramp rate is greater than 50mV/ms, this circuit will be adequate to ensure the device powers up correctly. (Due to oscillator settling considerations, communication to and from the DAC1220 should not occur for at least 25ms after power is stable.)

If this requirement cannot be met or if the circuit has brown-out considerations, the timing diagram of Figure 3 can be used to reset the DAC1220. This accomplishes the reset by controlling the duty cycle of the SCLK input. In general, reset is required after power-up, after a brown-out has been detected, or when a watchdog timer event has occurred.

I/O Recovery

If serial communication stops during an instruction or data transfer for longer than 4 t_{DATA}, the DAC1220 will reset its serial interface. This will not affect the internal registers. The main controller must not continue the transfer after this event but, must restart the transfer from the beginning. This feature is very useful if the main controller can be reset at any point. After reset, simply wait 8 t_{DATA} before starting serial communication.

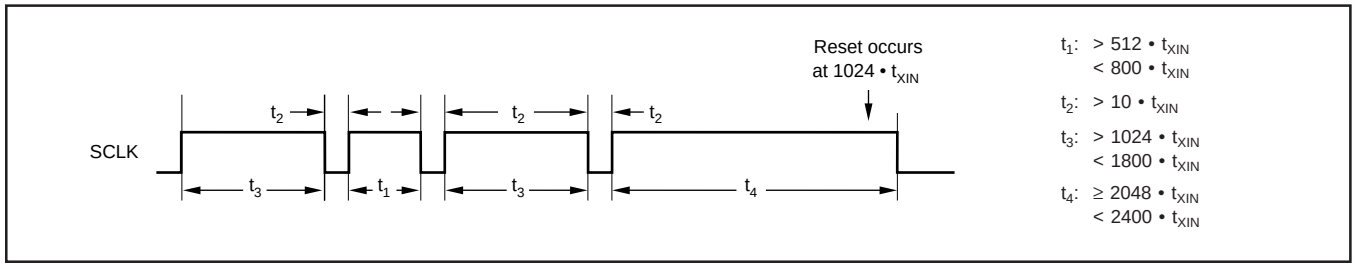


FIGURE 3. Resetting the DAC1220.

Isolation

The serial interface of the DAC1220 provides for simple isolation methods. An example of an isolated two-wire interface is shown in Figure 4.

Using $\overline{CS}$

The serial interface may make use of the $\overline{CS}$ signal, or this input may simply be tied LOW. There are several issues associated with choosing to do one or the other. The $\overline{CS}$ signal does not directly control the tri-state condition of the SDIO output. These signals are normally in the tri-state condition. They only become active when serial data is being transmitted from the DAC1220. If the DAC1220 is in the middle of a serial transfer and the SDIO is an output, taking $\overline{CS}$ HIGH will not tri-state the output signal.

If there are multiple serial peripherals utilizing the same serial I/O lines and communication may occur with any peripheral at any time, the $\overline{CS}$ signal must be used. The $\overline{CS}$ signal is then used to enable communication with the DAC1220.

Serial Clock

The DAC1220 allows multiple instructions to be issued per settling period as well as allowing the main controller to set the serial clock frequency and pace the serial data transfer. There are several important items regarding the serial clock for this mode of operation. The maximum serial clock frequency cannot exceed the DAC1220 X_{IN} frequency divided by 10.

TIMING

Table X and Figures 5 through 9 define the basic digital timing characteristics of the DAC1220. Figure 5 and the associated timing symbols apply to the X_{IN} input signal. Figures 6 through 9 and associated timing symbols apply to the serial interface signals (SCLK, SDIO, and $\overline{CS}$). The serial interface is discussed in detail in the Serial Interface section.

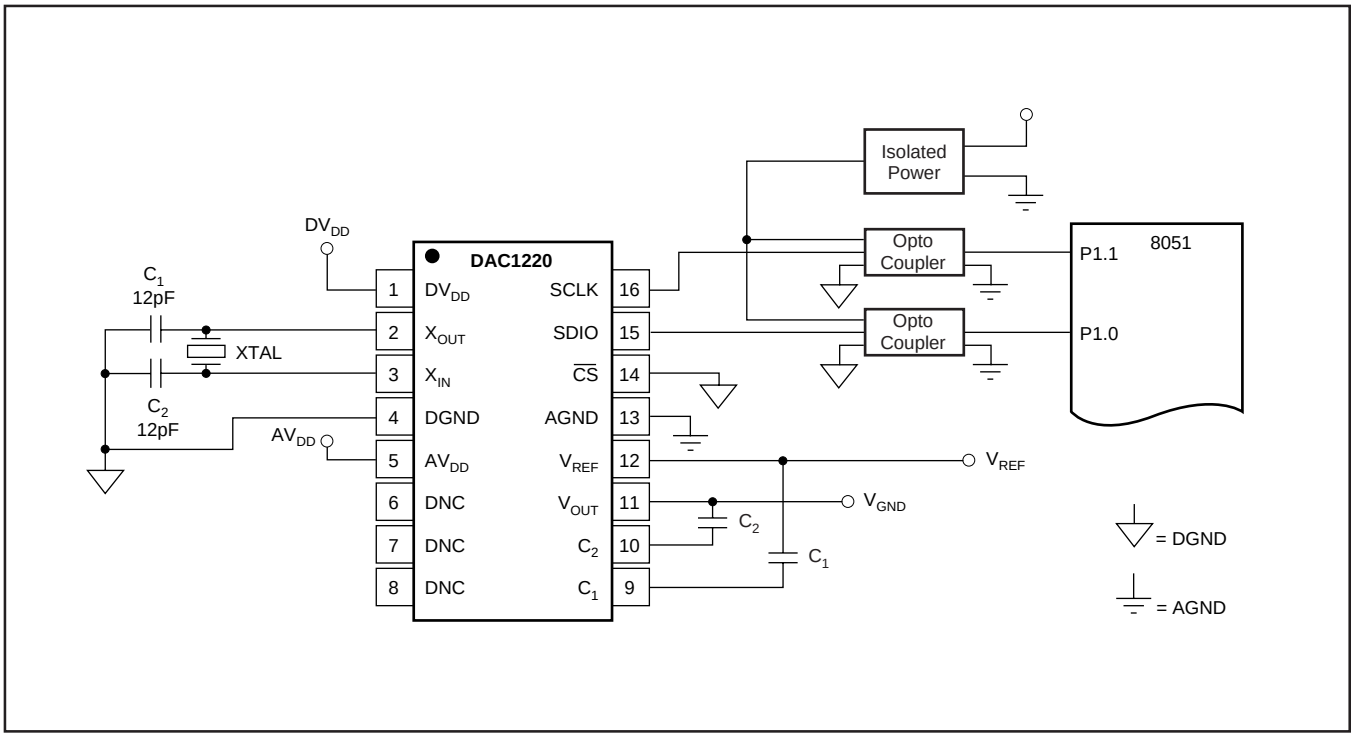


FIGURE 4. Isolation for Two-Wire Interface

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS
f_{XIN}	X_{IN} Clock Frequency	0.5	1	2.5	MHz
t_{XIN}	X_{IN} Clock Period	400		2000	ns
t_2	X_{IN} Clock High	0.4 • t_{XIN}			ns
t_3	X_{IN} Clock LOW	0.4 • t_{XIN}			ns
t_{10}	External Serial Clock HIGH	5 • t_{XIN}			ns
t_{11}	External Serial Clock LOW	5 • t_{XIN}			ns
t_{12}	Data In Valid to External SCLK Falling Edge (Setup)	40			ns
t_{13}	External SCLK Falling Edge to Data In Not Valid (Hold)	20			ns
t_{14}	Data Out Valid to External SCLK Falling Edge (Setup)	t_{XIN} –40			ns
t_{15}	External SCLK Falling Edge to Data Out Not Valid (Hold)	4 • t_{XIN}			ns
t_{19}	Falling Edge of Last SCLK for INSR to Rising Edge of First SCLK for Register Data	13 • t_{XIN}			ns ns
t_{24}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	11 • t_{XIN}			ns
t_{26}	SDIO as Output to Rising Edge of First SCLK for Register Data		4 • t_{XIN}		ns
t_{27}	Falling Edge of Last SCLK for INSR to SDIO Tri-state	6 • t_{XIN}		8 • t_{XIN}	ns
t_{28}	SDIO Tri-state Time		2 • t_{XIN}		ns
t_{30}	Falling Edge of Last SCLK for Register Data to SDIO Tri-State	4 • t_{XIN}		6 • t_{XIN}	ns
t_{36}	Falling Edge of Last SCLK for Register Data to Rising Edge of First SCLK of next INSR ($\overline{CS}$ Tied LOW)	41 • t_{XIN}			ns
t_{37}	Rising Edge of $\overline{CS}$ to Falling Edge of $\overline{CS}$ (Using $\overline{CS}$)	22 • t_{XIN}			ns

TABLE X. Digital Timing Characteristics.

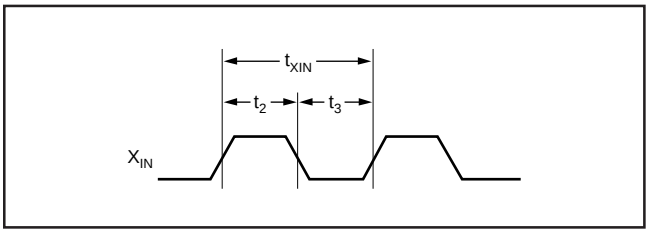


FIGURE 5. X_{IN} Clock Timing.

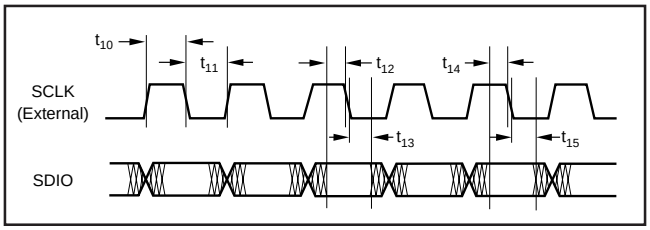


FIGURE 6. Serial Input/Output Timing.

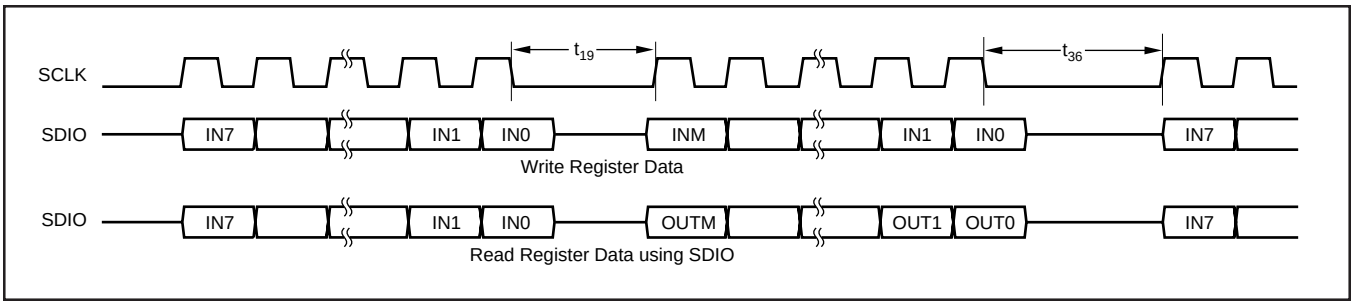


FIGURE 7. Serial Interface Timing ($\overline{CS}$ LOW).

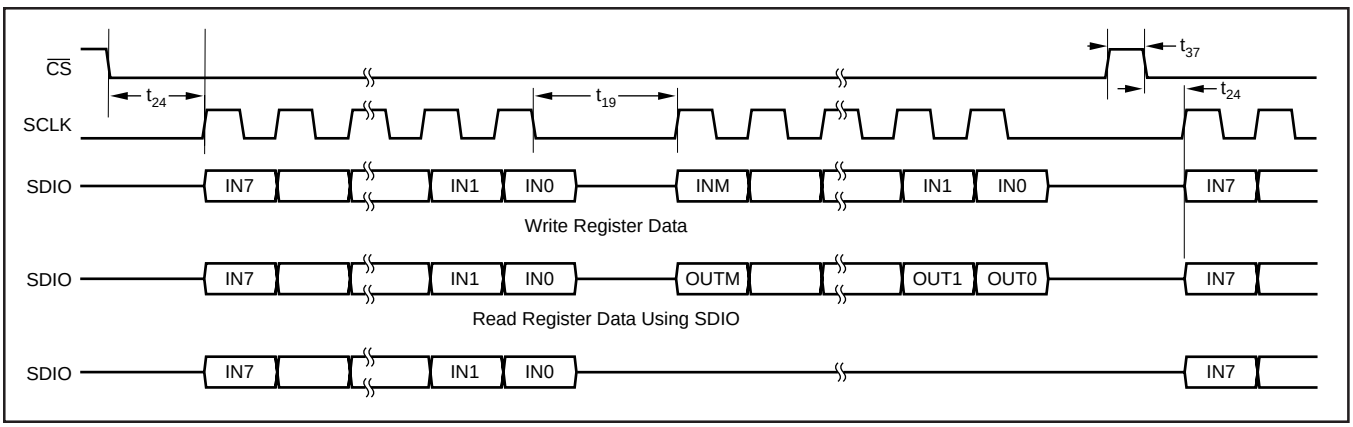


FIGURE 8. Serial Interface Timing (using $\overline{CS}$).

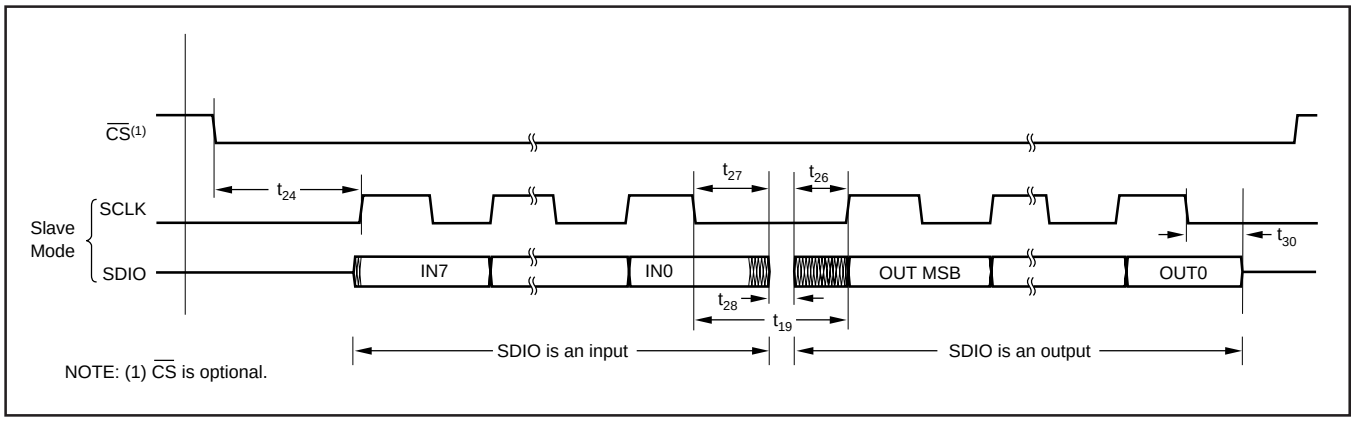


FIGURE 9. SDIO Input to Output Transition Timing.

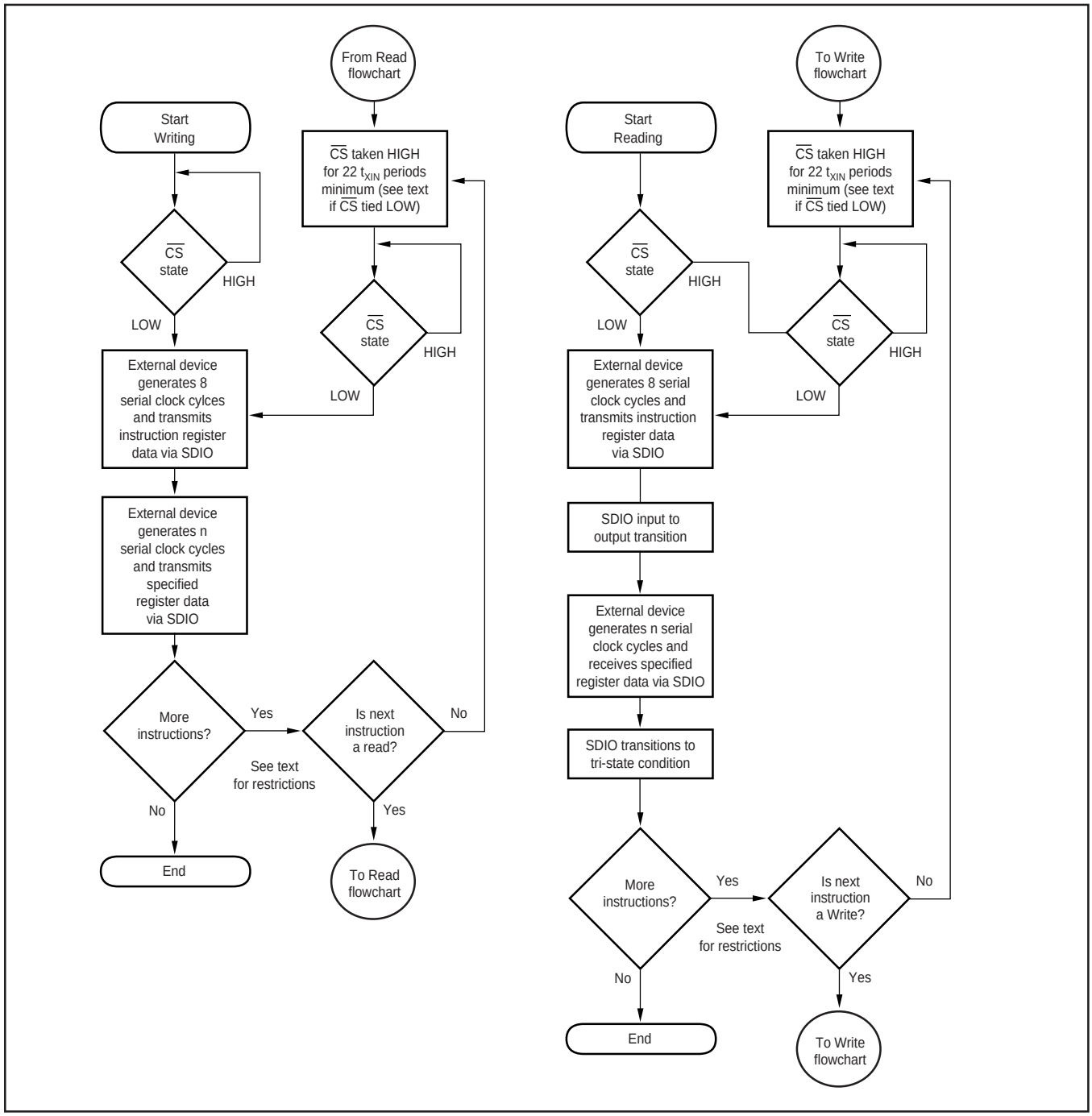


FIGURE 10. Flowchart for Writing and Reading Register Data.

LAYOUT

POWER SUPPLIES

The DAC1220 requires the digital supply (DV_{DD}) to be no greater than the analog supply (AV_{DD}) +0.3V. In the majority of systems, this means that the analog supply must come up first, followed by the digital supply and V_{REF}. Failure to observe this condition could cause permanent damage to the DAC1220.

Inputs to the DAC1220, such as SDIO or V_{REF} should not be present before the analog and digital supplies are on. Violating this condition could cause latch-up. If these signals are present before the supplies are on, series resistors should be used to limit the input current.

The best scheme is to power the analog section of the design and AV_{DD} of the DAC1220 from one +5V supply and the digital section (and DV_{DD}) from a separate +5V supply. The analog supply should come up first. This will ensure that SCLK, SDIO, $\overline{CS}$ and V_{REF} do not exceed AV_{DD} and that the digital inputs are present only after AV_{DD} has been established, and that they do not exceed DV_{DD}.

The analog supply should be well regulated and low noise. For designs requiring very high resolution from the DAC1220, power supply rejection will be a concern. See the "PSRR vs Frequency" curve in the Typical Performance Curves section of this data sheet for more information.

The requirements for the digital supply are not as strict. However, high frequency noise on DV_{DD} can capacitively couple into the analog portion of the DAC1220. This noise can originate from switching power supplies, very fast microprocessors or digital signal processors.

If one supply must be used to power the DAC1220, the AV_{DD} supply should be used to power DV_{DD}. This connection can be made via a 10Ω resistor which, along with the decoupling capacitors, will provide some filtering between DV_{DD} and AV_{DD}. In some systems, a direct connection can be made. Experimentation may be the best way to determine the appropriate connection between AV_{DD} and DV_{DD}.

GROUNDING

The analog and digital sections of the design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. AGND should be connected to the analog ground plane as well as all other analog grounds. DGND should be connected to the digital ground plane and all digital signals referenced to this plane.

The DAC1220 pinout is such that the converter is cleanly separated into an analog and digital portion. This should allow simple layout of the analog and digital sections of the design.

For a single converter system, AGND and DGND of the DAC1220 should be connected together, underneath the converter. Do not join the ground planes, but connect the two with a moderate signal trace. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. The printed circuit board can be designed to provide different analog/digital ground connections via short jumpers. The initial prototype can be used to establish which connection works best.

DECOUPLING

Good decoupling practices should be used for the DAC1220 and for all components in the design. All decoupling capacitors, but specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF to 10µF capacitor, in parallel with a 0.1µF ceramic capacitor, should be used to decouple AV_{DD} to AGND. At a minimum, a 0.1µF ceramic capacitor should be used to decouple DV_{DD} to DGND, as well as for the digital supply on each digital component.

SYSTEM CONSIDERATIONS

The recommendations for power supplies and grounding will change depending on the requirements and specific design of the overall system. In general, a system can be broken up into four different stages:

Digital Processing

Digital Portion of the DAC1220

Analog Portion of the DAC1220

Analog Processing

For the simplest system consisting of a self-contained microcontroller, one clock source, and minimal analog signal conditioning (basic filtering and gain), high performance could be achieved by powering all components by a common power supply. In addition, all components could share a common ground plane. Thus, there would be no distinctions between "analog" and "digital" power and ground. The layout should still include a power plane, a ground plane, and careful decoupling.

In a more extreme case, the design could include: multiple DAC1220s; one or more microcontrollers, digital signal processors, or microprocessors; many different clock sources; or extensive analog signal conditioning and interconnections to various other systems. High performance will be very difficult to achieve for this design. The approach would be to break the system into as many different parts as possible.

For example, each DAC1220 may have its own analog power and ground (possibly shared with the analog back end), and its own "digital" power and ground. The converter's "digital" power and ground would be separate from the power and ground for the system's processors, RAM, ROM, and "glue" logic.