

# T 6 B 5 0

## SOURCE DRIVER FOR TFT LCD PANELS

The T6B50 is a 120-channel-output source driver for TFT LCD panels. Its sampling select pin allows switching the of VIDEO input signals (R, G, B) to the desired output pins. Furthermore, since two or more of these devices can be used in combination, enabling designers to keep pace with increasing LCD panel sizes.

The T6B50 offers both low power consumption and high integration circuit due to the use of CMOS technology.

Unit: mm

| T6B50 | USER AREA PITCH |      |
|-------|-----------------|------|
|       | IN              | OUT  |
| (UCM) | 1.0             | 0.20 |

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

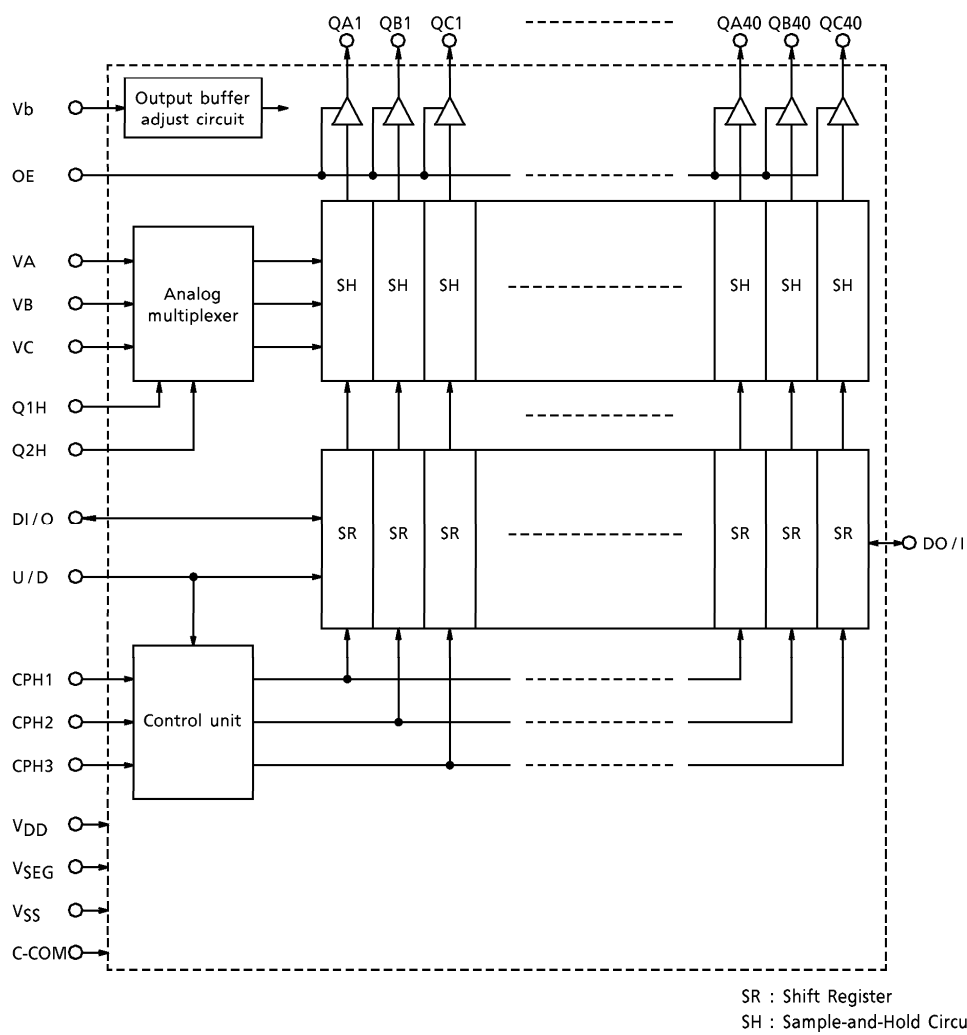
### FEATURES

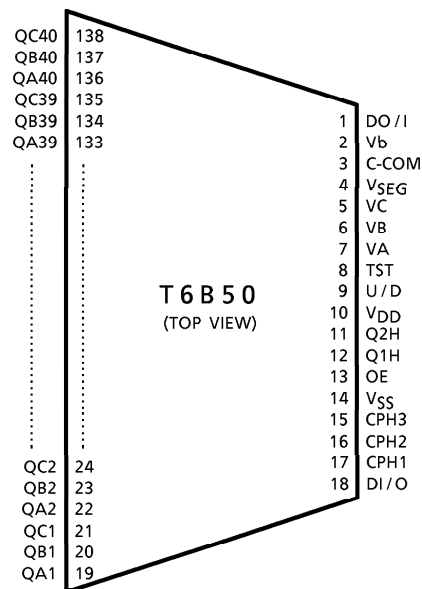
- LCD drive output pins : 120 pins (40 pins each for R, G and B)
- LCD drive voltage : Max 15 V
- Data transfer method : Bidirectional shift register
- Operating temperature : -20°C to 75°C
- Package : Tape carrier package (TCP)
- Low-offset drive output
- Auto standby function for reduced power consumption
- TFT LCD gate drivers : T6L08

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## BLOCK DIAGRAM



**PIN ASSIGNMENT**

The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

## PIN FUNCTION

| PIN NAME     | I/O    | FUNCTION  |     |      |      |   |       |        |   |        |       |
|--------------|--------|---|-----|------|------|---|-------|--------|---|--------|-------|
| DI/O<br>DO/I | I/O    | <p>Vertical shift data I/O pins</p> <p>These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.</p> <table border="1"> <tr> <td>U/D</td><td>DI/O</td><td>DO/I</td></tr> <tr> <td>H</td><td>Input</td><td>Output</td></tr> <tr> <td>L</td><td>Output</td><td>Input</td></tr> </table> <p>When set for input<br/>This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPH1.</p> <p>When set for output<br/>When two or more T6B50s are cascaded, this pin outputs the data to be fed into the next stage.</p> | U/D | DI/O | DO/I | H | Input | Output | L | Output | Input |
| U/D          | DI/O   | DO/I  |     |      |      |   |       |        |   |        |       |
| H            | Input  | Output  |     |      |      |   |       |        |   |        |       |
| L            | Output | Input   |     |      |      |   |       |        |   |        |       |
| U/D          | Input  | <p>Transfer direction select pin</p> <p>This pin specifies the direction of sampling performed by the sample-and-hold circuits before data is output to QA1 through QC40 as shown below.</p> <p>When U/D is high, data is sampled in the sequence<br/>QA1 → QB1 → QC1 → QA2 → QB2 → QC2 → ... → QC40</p> <p>When U/D is low, the sequence is reversed to give<br/>QC40 → QB40 → QA40 → QC39 → ... → QA1</p> <p>The voltage applied to this pin must be a DC-level voltage that is either high (<math>V_{DD}</math>) or low (<math>V_{SS}</math>).</p>   |     |      |      |   |       |        |   |        |       |
| CPH1 to 3    | Input  | <p>Shift clock input</p> <p>These clocks sequentially shift the signal necessary to sample the data that are output to the LCD drive output pins (QA1 to QC40).</p>   |     |      |      |   |       |        |   |        |       |
| OE           | Input  | <p>Output enable input</p> <p>This signal enables the LCD drive output.</p> <p>The LCD drive output is enabled when this signal is high; it is placed in the Hi-Z state when this signal is low.</p>  |     |      |      |   |       |        |   |        |       |
| Q1H/Q2H      | Input  | <p>Analog signal select input</p> <p>These signals switch the input data VA, VB and VC to the corresponding output pins: QA, QB and QC.</p>   |     |      |      |   |       |        |   |        |       |

| PIN NAME                            | I/O    | FUNCTION  |
|-------------------------------------|--------|---|
| Vb                                  | Input  | Output buffer adjustment input<br>This signal allows the capacity of the LCD drive output buffer to be varied depending on the voltage applied to it. The higher the applied voltage, the greater the drive capacity.<br>* Toshiba recommends using Vb = approximately 2.0 V. |
| VA<br>VB<br>VC                      | Input  | Analog signal input<br>These pins accept as their input the analog signals that are output to the LCD drive output pins.  |
| C-COM                               | Input  | Sample and hold reference voltage input<br>This is the reference voltage for the sample-and-hold circuit. For this input, Toshiba recommends using the middle one of the these analog input voltage levels (VA, VB and VC).   |
| QA1 to 40<br>QB1 to 40<br>QC1 to 40 | Output | LCD drive output<br>These pins output one of the analog signal inputs (VA, VB and VC) after it has been sampled and held by the sample-and-hold circuit.  |
| VSEG                                | —      | Power supply for the device's high-voltage block  |
| VDD                                 | —      | Power supply for the device's logic block   |
| VSS                                 | —      | Common GND for the device   |

## DEVICE OPERATION

### (1) Analog signal sampling

Data transfer begins with the assertion of DI/O (U/D = high) or DO/I (U/D = low).

The table below shows the relation between the shift clocks and the analog signals (see Fig. 1).

| U/D | CPH1      | CPH2      | CPH3      |
|-----|-----------|-----------|-----------|
| H   | QA1 to 40 | QB1 to 40 | QC1 to 40 |
| L   | QC40 to 1 | QB40 to 1 | QA40 to 1 |

#### <When U/D = high>

- A high on DI/O is latched into the internal logic synchronously with the rising edge of CPH1, and the analog signal to be output to QA1 is sampled at the next rising edge of CPH1. In this way, all analog signals are sampled sequentially at each rising edge of CPH2, CPH3, CPH1, CPH2, CPH3 and so on, and the analog signals are output to QB1, QC1, QA2, QB2, QC2 and so on.
- After the device finishes sampling the data for QC40, it automatically enters standby state. Unless DI/O is asserted again, no data is sampled, irrespective of whether CPH1 to CPH3 are input to the device.

#### <When U/D = low>

- A high on DO/I is latched into the internal logic synchronously with the rising edge of CPH1, and the analog signal to be output to QC40 is sampled at the next rising edge of CPH1. In this way, all analog signals are sampled sequentially at each rising edge of CPH2, CPH3, CPH1, CPH2, CPH3 and so on, and the analog signals are output to QB40, QA40, QC39, QB39, QA39 and so on.
- After the device finishes sampling the data for QA1, it automatically enters standby state. Unless DO/I is asserted again, no data is sampled, irrespective of whether CPH1 to CPH3 are input to the device.

Analog signal inputs VA, VB and VC are fed into the sample-and-hold circuits before they are forwarded to the LCD drive outputs: QA1 to 40, QB1 to 40 and QC1 to 40. Which analog input is sampled and held by which LCD drive output is determined by the Q1H/Q2H select signals as shown below.

| ANALOG SIGNAL INPUT SELECT PIN |     | ANALOG SIGNAL INPUT | LCD DRIVE OUTPUT |
|--------------------------------|-----|---------------------|------------------|
| Q1H                            | Q2H |                     |                  |
| 0                              | 0   | VA                  | QC1 to 40        |
|                                |     | VB                  | QB1 to 40        |
|                                |     | VC                  | QA1 to 40        |
| 0                              | 1   | VA                  | QA1 to 40        |
|                                |     | VB                  | QC1 to 40        |
|                                |     | VC                  | QB1 to 40        |
| 1                              | 0/1 | VA                  | QB1 to 40        |
|                                |     | VB                  | QA1 to 40        |
|                                |     | VC                  | QC1 to 40        |

## (2) LCD drive output

When OE is driven high, the sampled-and-held data is fed to the LCD drive output pins (QA1 through QC40).

The LCD drive output is enabled when OE is high; it is put in the Hi-Z state when OE is low.

OE must be kept low while the device is sampling data and driven high when the device has finished sampling.

The drive capabilities of the LCD drive output pins are controlled by the output buffer adjustment input (Vb). The drive capability is at a minimum when  $V_b = V_{SS}$  and increases as the Vb voltage is raised, hence the drive capability can be set to the desired level (typ.:  $V_b = V_{SS} + 1\text{ V}$  to  $V_{SS} + 3\text{ V}$ ).

## (3) Vertical shift data output

The output DO/I (U/D = high) or DI/O (U/D = low) is driven high for one clock period synchronously with the falling edge of CPH3, one-and-a-half clock period before the data (which is to be output to QC40 or QA1) is latched into the shift register (see timing diagram).

## (4) Expanding LCD drive output

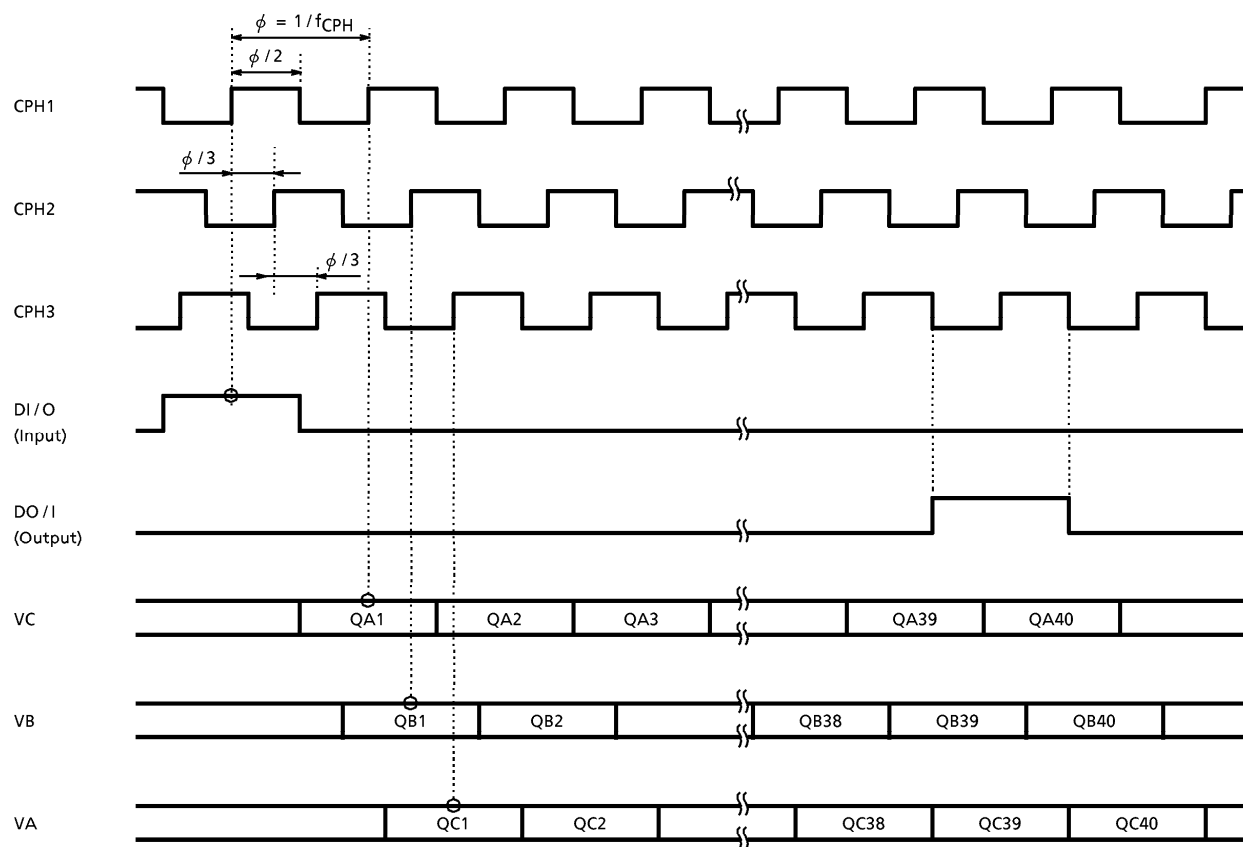
When using two or more of these devices to drive a large screen, connect the vertical shift data output from the first stage of the LCD driver directly to the vertical shift data input at the next stage. In this way, the device's LCD drive output pin can easily be expanded as necessary.

## (5) Sample-and-hold reference voltage (C-COM)

The device's sample-and-hold circuits are configured using the internal capacitors. The C-COM pin is used to supply the reference voltage for these circuits. For this input, Toshiba recommends using the middle one of the three analog input voltage levels signals input to the device. The voltage applied here must be a DC-level voltage.

## TIMING DIAGRAM

- UP mode (U/D = high)



Conditions Q1H = Low  
Q2H = Low



• Down mode (U/D = low)

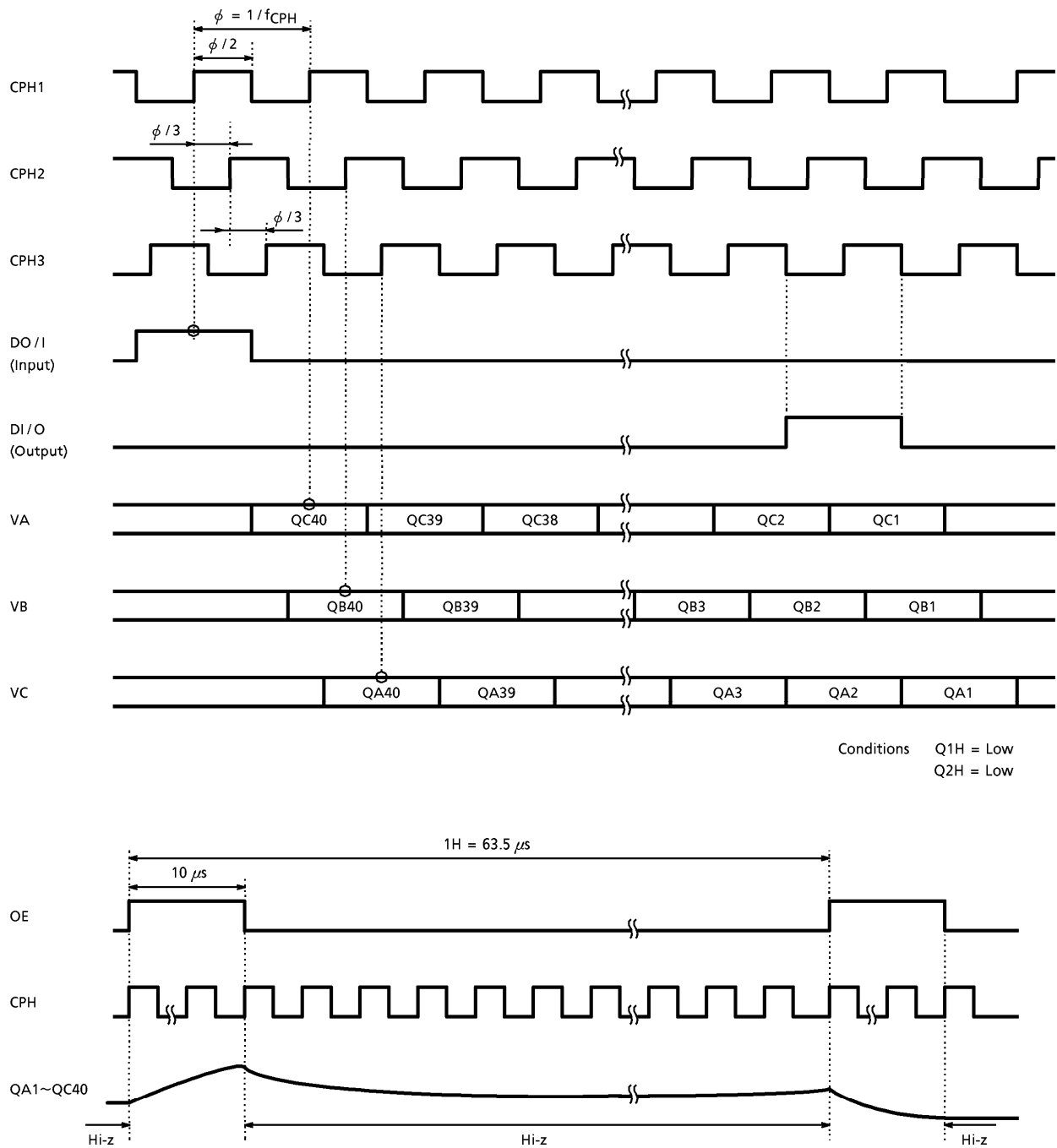


Fig.1

**ABSOLUTE MAXIMUM RATINGS** ( $V_{SS} = 0\text{ V}$ )

| PARAMETER            | SYMBOL      | RATING                  | UNIT | RELEVANT PIN |
|----------------------|-------------|-------------------------|------|--------------|
| Supply Voltage (1)   | $V_{DD}$    | -0.3 to 7.0             | V    | —            |
| Supply Voltage (2)   | $V_{SEG}$   | -0.3 to 18              | V    | —            |
| Input Voltage        | $V_{IN}$    | -0.3 to $V_{DD} + 0.3$  | V    | (Note 1)     |
| Storage Temperature  | $T_{STG}$   | -55 to 125              | °C   | —            |
| Analog Input Voltage | $V_{VIDEO}$ | -0.3 to $V_{SEG} + 0.3$ | V    | (Note 2)     |

**RECOMMENDED OPERATING CONDITIONS** ( $V_{SS} = 0\text{ V}$ )

| PARAMETER               | SYMBOL      | RATING                 | UNIT | RELEVANT PIN |
|-------------------------|-------------|------------------------|------|--------------|
| Supply Voltage (1)      | $V_{DD}$    | 4.5 to 5.5             | V    | —            |
| Supply Voltage (2)      | $V_{SEG}$   | $V_{DD}$ to 15         | V    | —            |
| Operating Temperature   | $T_{OP}$    | -20 to 75              | °C   | —            |
| Operating Frequency     | $f_{CPH}$   | 0.5 to 6.0             | MHz  | —            |
| Output Load Capacitance | $C_L$       | 0 to 100               | pF   | —            |
| Analog Input Voltage    | $V_{VIDEO}$ | 1.0 to $V_{SEG} - 2.0$ | V    | (Note 2)     |

(Note 1) : All input pins except the analog signal input pins ( $V_A$ ,  $V_B$ ,  $V_C$ ,  $V_b$  and C-COM)

(Note 2) : Analog signal input pins ( $V_A$ ,  $V_B$ ,  $V_C$ ,  $V_b$  and C-COM)

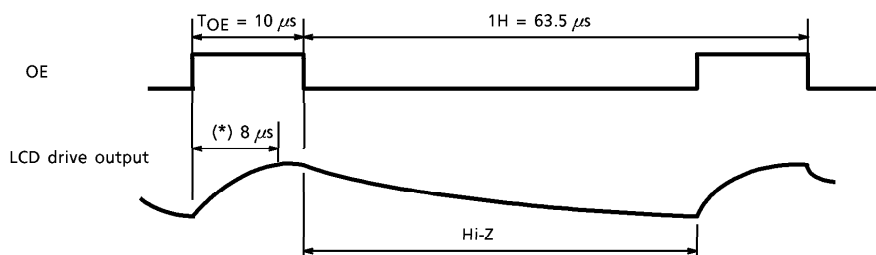
## ELECTRICAL CHARACTERISTICS

DC CHARACTERISTIC (Referenced to  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SEG} = 13$  V,  $V_{SS} = 0$  V at  $T_a = -20$  to  $75^\circ\text{C}$  unless otherwise noted)

| PARAMETER               |            | SYMBOL      | TEST CIRCUIT | TEST CONDITIONS            | MIN                 | TYP. | MAX                 | UNIT          | RELEVANT PIN |
|-------------------------|------------|-------------|--------------|----------------------------|---------------------|------|---------------------|---------------|--------------|
| Input Voltage           | Low Level  | $V_{IL}$    | —            | —                          | 0                   | —    | $0.2 \times V_{DD}$ | V             | Logic input  |
|                         | High Level | $V_{IH}$    |              | —                          | $0.8 \times V_{DD}$ | —    | $V_{DD}$            |               |              |
| Output Voltage          | Low Level  | $V_{OL}$    | —            | $I_{OL} = 40 \mu\text{A}$  | $V_{SS}$            | —    | $V_{SS} + 0.3$      | V             | DI/O, DO/I   |
|                         | High Level | $V_{OH}$    |              | $I_{OH} = -40 \mu\text{A}$ | $V_{DD} - 0.3$      | —    | $V_{DD}$            |               |              |
| Output Offset Voltage   |            | $V_{OFF}$   | —            | —                          | -50.0               | —    | 50.0                | mV            | QA1 to QC40  |
| Output Current          |            | $I_{OL}$    | —            | (Note 3)                   | —                   | 0.2  | —                   | mA            | QA1 to QC40  |
| Output Leakage Current  |            | $I_{DLEAK}$ | —            | OE = L                     | -1.0                | —    | 1.0                 | $\mu\text{A}$ | QA1 to QC40  |
| Input Current           |            | $I_{IN}$    | —            | —                          | -1.0                | —    | 1.0                 | $\mu\text{A}$ | Logic input  |
| Current Consumption (1) |            | $I_{DD}$    | —            | (Note 4)                   | —                   | —    | 3.0                 | mA            | —            |
| Current Consumption (2) |            | $I_{SEG}$   | —            | (Note 4)                   | —                   | —    | 6.5                 | mA            | —            |

(Note 3) :  $V_b = 2$  V,  $V_{LOAD} = Q_{OUT} \pm 0.5$

(Note 4) :  $f_{CPH} = 3$  MHz,  $1H = 63.5 \mu\text{s}$ ,  $T_{OE} = 10 \mu\text{s}$ ,  $V_{VIDEO} =$  amplitude of 1 to 11 V, load capacitance = 100 pF (all output pins)



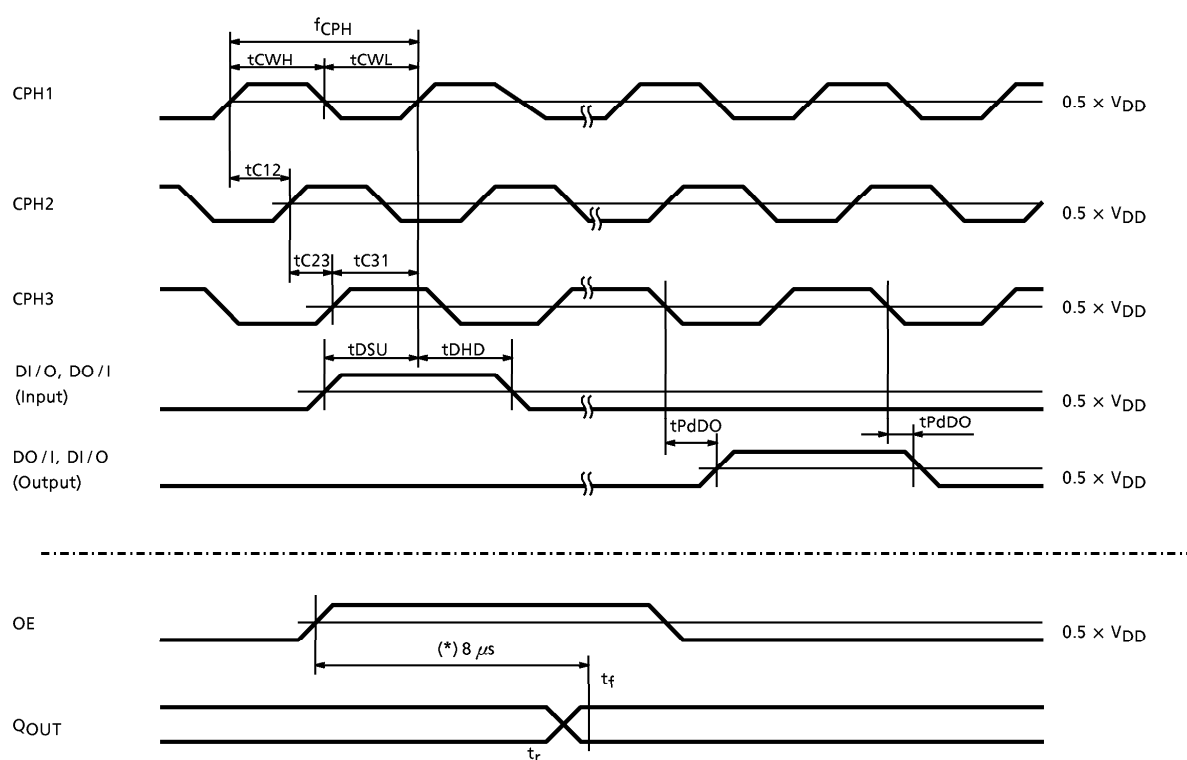
(\*) : This interval can be varied by adjusting  $V_b$ .

Fig. 2

AC CHARACTERISTICS (Referenced to  $V_{DD} = 4.5$  to  $5.5$  V,  $V_{SEG} = 13$  V,  $V_{SS} = 0$  V at  $T_a = -20$  to  $75^\circ\text{C}$  unless otherwise noted)

| PARAMETER                 | SYMBOL                            | TEST CONDITIONS | MIN | TYP. | MAX         | UNIT |
|---------------------------|-----------------------------------|-----------------|-----|------|-------------|------|
| Operating Frequency       | $f_{CPH}$ ( $1/t_{CPH}$ )         | —               | 0.5 | —    | 6           | MHz  |
| Clock to Clock Delay Time | $t_{C12}$ , $t_{C23}$ , $t_{C31}$ | —               | 40  | —    | $t_{CPH}/2$ | ns   |
| CPH Pulse Width (H)       | $t_{CWH}$                         | —               | 80  | —    | —           | ns   |
| CPH Pulse Width (L)       | $t_{CWL}$                         | —               | 80  | —    | —           | ns   |
| Data Set-up Time          | $t_{DSU}$                         | —               | 20  | —    | —           | ns   |
| Data Hold Time            | $t_{DHD}$                         | —               | 60  | —    | —           | ns   |
| Output Delay Time         | $t_{pDO}$                         | $C_L = 30$ pF   | 50  | —    | —           | ns   |

(Note) : The  $Q_{OUT}$  rise and fall times ( $t_r$ ,  $t_f$ ) can be varied by changing  $V_b$ .



(Duration of Logic Input Signal  $t_r$ ,  $t_f = 6$  ns)

(\*) : Use OE with a period at  $63.5 \mu s$  intervals.