TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6L09

SOURCE DRIVER FOR TFT LCD PANELS

The T6L09 is a 240-channel-output source driver for TFT LCD panels. Its sampling select pin allows switching of the VIDEO input signals (R, G, B) to the desired output pins. Furthermore, two or more of these devices can be used in combination enabling designers to keep pace with increasing LCD panel sizes.
The T6L09 offers both low power consumption and high integration circuit due to CMOS technology.

Unit: mm

T6L09	USER AREA PITCH	
	IN	OUT
(SGN, 7ES)	1.0	0.09

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

FEATURES

- LCD drive output pins : 240 pins (80 pins each for R, G and B)
- LCD drive voltage : Max 15 V
- Data transfer method : Bidirectional shift register
- Operating temperature : −20 to 75°C
- Package : Tape carrier package (TCP)
- TFT LCD gate driver : T6L08

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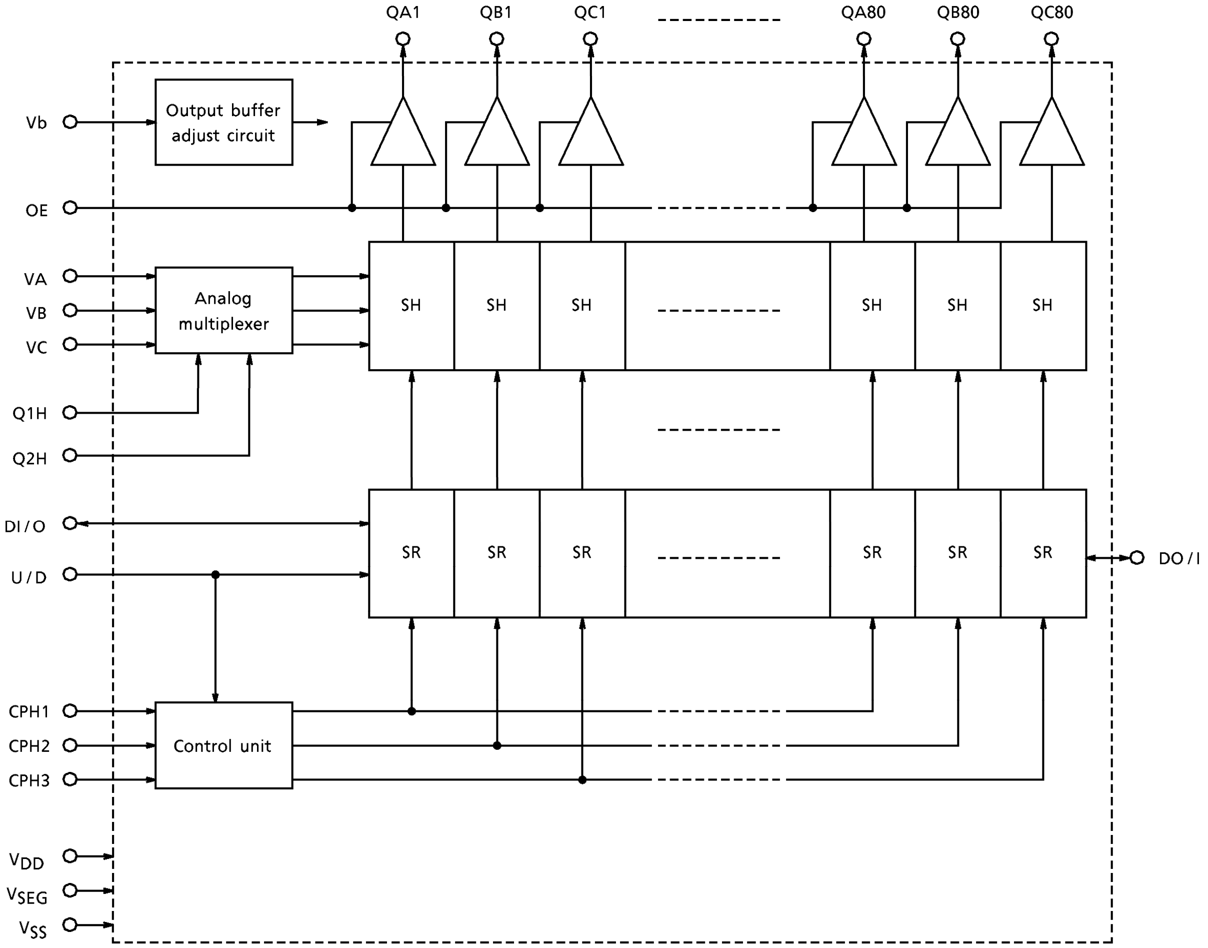
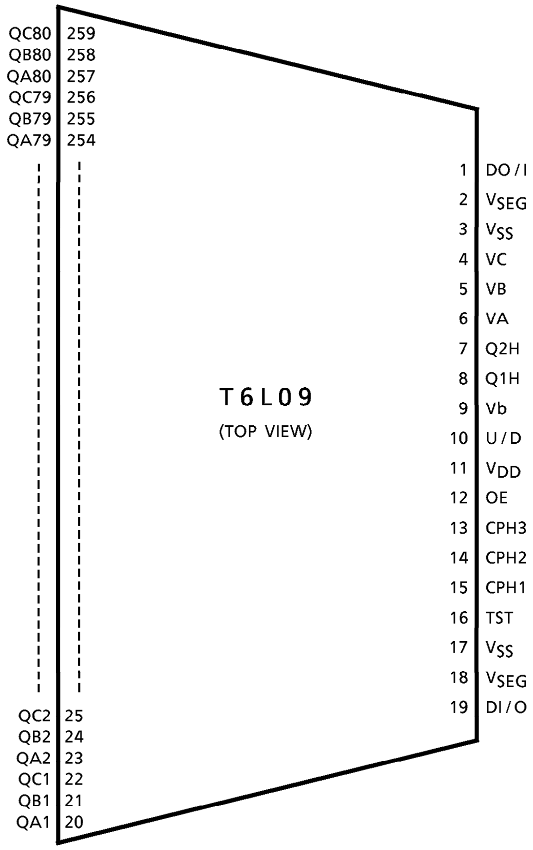
BLOCK DIAGRAM



SR : Shift Register
SH : Sample-and-Hold Circuit

PIN ASSIGNMENT



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

PIN FUNCTION

<table>
<tr><th>PIN NAME</th><th>I / O</th><th>FUNCTION</th></tr>
<tr><td>DI / O
DO / I</td><td>I / O</td><td>Vertical shift data I / O pins
These pins are used to input and output shift data. These pins are switched for input or output by setting the U / D pin as shown below.
<table>
<tr><th>U / D</th><th>DI / O</th><th>DO / I</th></tr>
<tr><td>H</td><td>INPUT</td><td>OUTPUT</td></tr>
<tr><td>L</td><td>OUTPUT</td><td>INPUT</td></tr>
</table>
When set for input
This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPH1.
When set for output
When two or more T6L09s are cascaded, this pin outputs the data to be fed into the next stage.</td></tr>
<tr><td>U / D</td><td>Input</td><td>Transfer direction select pin
This pin specifies the direction of sampling performed by the sample-and-hold circuit.
When U / D is high, data is sampled in the sequence
QA1 → QB1 → QC1 → QA2 → QB2 → ····· → QC80
When U / D is low, the sequence is reversed to give
QC80 → QB80 → QA80 → QC79 → ····· → QA1
The voltage applied to this pin must be a DC-level voltage that is either high (V_{DD}) or low (V_{SS}).</td></tr>
<tr><td>CPH1 to 3</td><td>Input</td><td>Shift clock input
These clocks sequentially shift the signals necessary to sample the data that are output to the LCD drive output pins (QA1 to QC80).</td></tr>
<tr><td>OE</td><td>Input</td><td>Output enable input
This signal enables the LCD drive output.
The LCD drive output is enabled when this signal is high; it is put in the Hi-Z state when this signal is low.</td></tr>
<tr><td>Q1H / Q2H</td><td>Input</td><td>Analog signal select input
These signals switch the input data VA, VB and VC to the corresponding output pins: QA, QB and QC.</td></tr>
<tr><td>Vb</td><td>Input</td><td>Output buffer adjustment input
This signal allows the capacity of the LCD drive output buffer to be varied depending on the voltage applied to it. The lower the applied voltage, the greater the drive capacity.</td></tr>
<tr><td>VA
VB
VC</td><td>Input</td><td>Analog signal input
These pins accept as their input the analog signals that are output to the LCD drive output pins.</td></tr>
</table>

PIN NAME	I / O	FUNCTION
QA1 to 80 QB1 to 80 QC1 to 80	Output	LCD drive output These pins output one of the analog signal inputs (VA, VB or VC) after it has been sampled and held by the sample-and-hold circuit.
V_{SEG}		Power supply for the device's high-voltage block
V_{DD}		Power supply for the device's logic block
V_{SS}		Common GND for the device

DEVICE OPERATION (see timing diagram)

(1) Analog signal sampling

Data transfer begins with the assertion of DI / O (when U / D = high) or DO / I (when U / D = low).

The table below shows the relation between the shift clocks and the analog signals.

U / D	CPH1	CPH2	CPH3
H	QA1 to 80	QB1 to 80	QC1 to 80
L	QC80 to 1	QB80 to 1	QA80 to 1

<When U / D = high>

- A high on DI / O is latched into the internal logic synchronously with the rising edge of CPH1, and the analog signal to be output to QA1 is sampled at the next rising edge of CPH1. In this way, all analog signals are sampled sequentially at each rising edge of CPH2, CPH3, CPH1, CPH2, CPH3 and so on, as the analog signals are output to QB1, QC1, QA2, QB2, QC2 and so on.
- After the device finishes sampling the data for QC80, it automatically enters standby state. Unless DI / O is asserted again, no data is sampled, irrespective of whether CPH1 to CPH3 are input to the device.

<When U / D = low>

- A high on DO / I is latched into the internal logic synchronously with the rising edge of CPH1, and the analog signal to be output to QC80 is sampled at the next rising edge of CPH1. In this way, all analog signals are sampled sequentially at each rising edge of CPH2, CPH3, CPH1, CPH2, CPH3 and so on and the analog signals are output to QB80, QA80, QC79, QB79, QA79 and so on.
- After the device finishes sampling the data for QA1, it automatically enters standby state. Unless DO / I is asserted again, no data is sampled, irrespective of whether CPH1 to CPH3 are input to the device.

Analog signal inputs VA, VB and VC are fed into the sample-and-hold circuits before they are forwarded to the LCD drive outputs: QA1-80, QB1-80 and QC1-80. Which analog input is sampled and held by which LCD drive output is determined by the Q1H / Q2H select signal as shown below.

ANALOG SIGNAL INPUT SELECT PIN		ANALOG SIGNAL INPUT	LCD DRIVE OUTPUT	
Q1H	Q2H		U / D = high	U / D = low
0	0	VA	QC1 to 80	QA1 to 80
		VB	QB1 to 80	QB1 to 80
		VC	QA1 to 80	QC1 to 80
0	1	VA	QA1 to 80	QB1 to 80
		VB	QC1 to 80	QC1 to 80
		VC	QB1 to 80	QA1 to 80
1	0 / 1	VA	QB1 to 80	QC1 to 80
		VB	QA1 to 80	QA1 to 80
		VC	QC1 to 80	QB1 to 80

(2) LCD drive output

When OE is driven high, the sampled-and-held data is fed to the LCD drive output pins (QA1 through QC80).

The LCD drive output is enabled when OE is high; it is put in the Hi-Z state when OE is low.

OE should be kept low while the device is sampling data.
The drive capabilities of the LCD drive output pins are controlled by the output buffer adjustment input (Vb). The drive capability is at a minimum when Vb = V_{SEG} and decrease as the Vb voltage is raised, hence the drive capability can be set to the desired level.

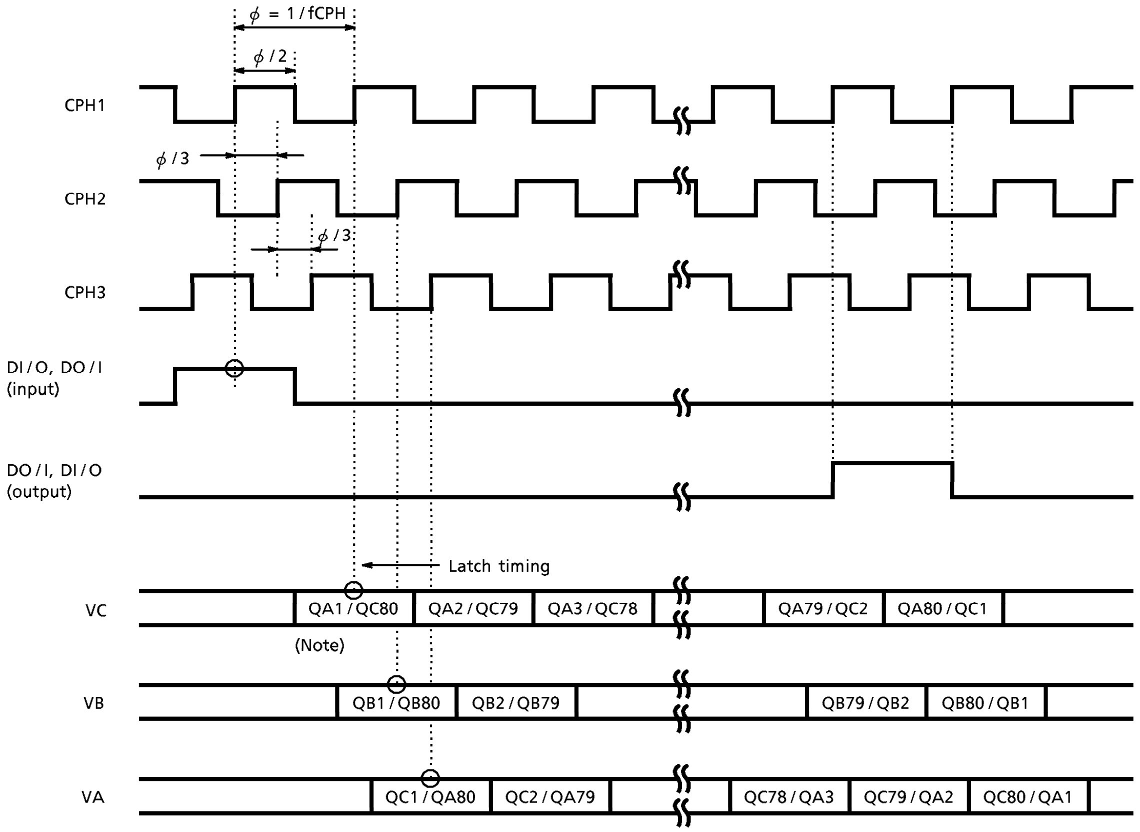
(3) Vertical shift data output

The output DO / I (when U / D = high) or DI / O (when U / D = low) is driven high for one clock period synchronously with the rising edge of CPH1 one clock period before the data to be output to QA80 or QC1 is latched into the shift register (see timing diagram).

(4) Expanding LCD drive output

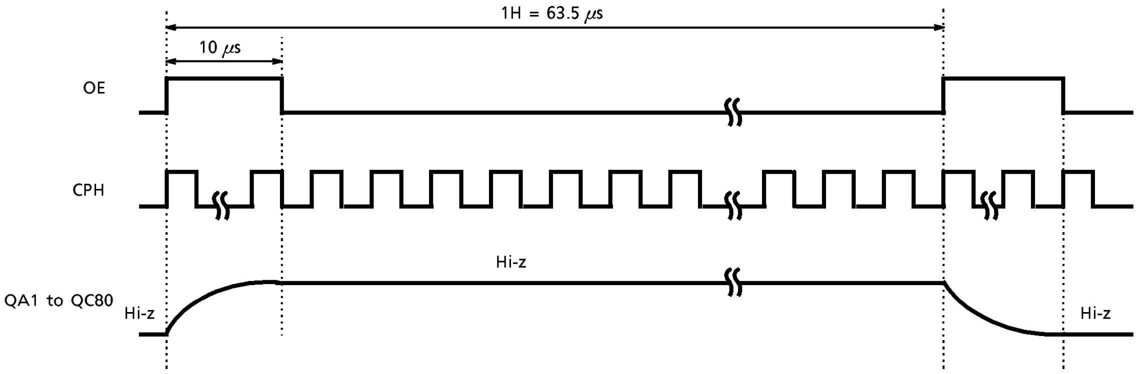
When using two or more of these devices to drive a large screen, connect the vertical shift data output from the first stage of the LCD driver directly to the vertical shift data input at the next stage. In this way, the device's LCD drive output pin can easily be expanded as necessary.

TIMING DIAGRAM



Conditions Q1H = low, Q2H = low

(Note) : QA1 / QC80 : U / D = high → QA1
U / D = low → QC80



ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING	UNIT	RELEVANT PIN
Supply Voltage (1)	V_{SEG}	−0.3 to 18	V	
Supply Voltage (2)	V_{DD}	−0.3 to 7.0	V	
Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	(Note 1)
Storage Temperature	T_{stg}	−55 to 125	°C	
Analog Input Voltage	V_{VIDEO}	−0.3 to V_{SEG} + 0.3	V	(Note 2)

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING	UNIT	RELEVANT PIN
Supply Voltage (1)	V_{SEG}	V_{DD} to 15	V	
Supply Voltage (2)	V_{DD}	4.5 to 5.5	V	
Operating Temperature	T_{OP}	−20 to 75	°C	
Operating Frequency	f_{CPH}	0.5 to 6.0	MHz	
Output Load Capacitance	C_L	0 to 200	pF	
Analog Input Voltage	V_{VIDEO}	1.0 to V_{SEG} − 2.0	V	(Note 2)

(Note 1) : All input pins except the analog signal input pins (VA, VB, VC and Vb)
(Note 2) : Analog signal input pins (VA, VB, VC and Vb)

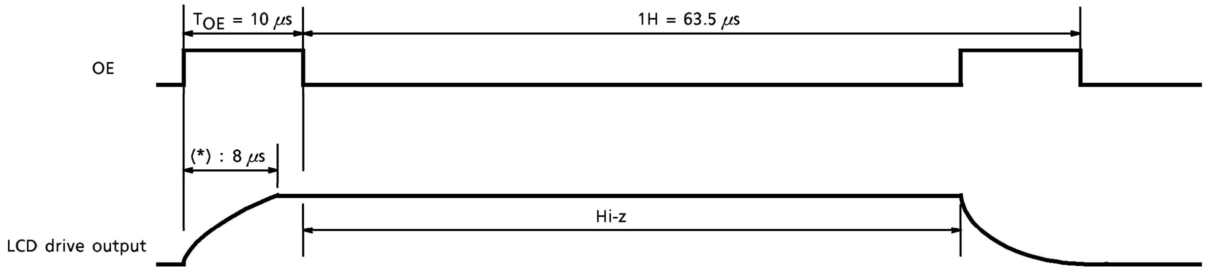
ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Referenced to V_{DD} = 4.5 to 5.5 V, V_{SEG} = 13 V, V_{SS} = 0 V, Ta = −20 to 75°C unless otherwise noted)

PARAMETER		SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	RELEVANT PIN
Input Voltage	Low Level	V_{IL}	—		0		0.2 × V_{DD}	V	Logic input
	High Level	V_{IH}	—		0.8 × V_{DD}		V_{DD}		
Output Voltage	Low Level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}		V_{SS} + 0.3	V	DI / O, DO / I
	High Level	V_{OH}	—	I_{OH} = −40 μA	V_{DD} − 0.3		V_{DD}		
Output Offset Voltage		V_{OFF}	—		−50.0		50.0	mV	QA1 to QC80
Output Current		I_{OL}	—	(Note 3)		0.2		mA	QA1 to QC80
Output Leakage Current		I_{DLEAK}	—	OE = Low	−1.0		1.0	μA	
Input Current		I_{IN}	—		−1.0		1.0	μA	Logic input
Current Consumption (1)		I_{DD}	—	(Note 4)				mA	
Current Consumption (2)		I_{SEG}	—	(Note 4)				mA	

(Note 3) : Vb = 11 V, V_{VIDEO} = 11 V

(Note 4) : f_{CPH} = 3 MHz, 1H = 63.5 μs, TOE = 10 μs, V_{VIDEO} = amplitude of 1 to 11 V, load capacitance = 100 pF (all output pins)

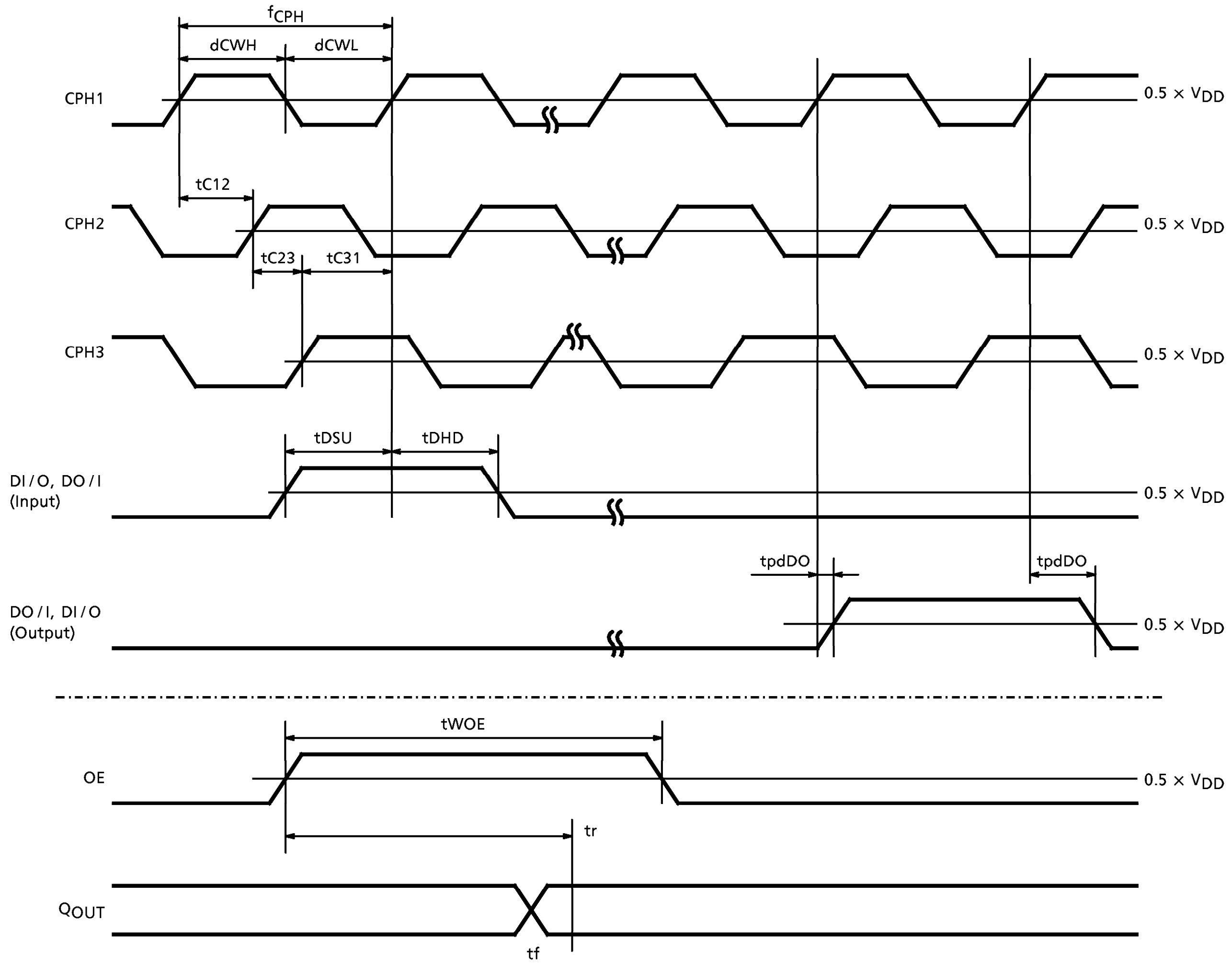


(*) : This interval can be varied by adjusting Vb.

AC CHARACTERISTICS (Referenced to V_{DD} = 4.5 to 5.5 V, V_{SEG} = 13 V, V_{SS} = 0 V, Ta = −20 to 75°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Operating Frequency	f_{CPH} (1 / tCPH)		0.5	6	MHz
Clock to Clock Delay Time	tC12, tC23, tC31		40	tCPH / 2	ns
CPH Pulse Duty Cycle	dCWH / dCWL		40	60	%
Data Set-up Time	tDSU		20		ns
Data Hold Time	tDHD		60		ns
Output Delay Time	tpdDO	CL = 30 pF		60	ns
OE Pulse Width	tWOE		5	20	μs

(Note) : The Qout rise and fall times (tr, tf) can be varied by changing Vb.



(Duration of Logic Input Signals tr, tf = 6 ns)

(*) : Use OE with a period at 63.5 ns intervals.