#### CMOS 8-Bit Microcontroller

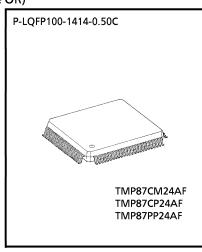
# TMP87CM24AF, TMP87CP24AF

The TMP87CM24A/P24A are the high speed and high performance 8-bit single chip microcomputers. These MCU contain, large ROM, RAM, input/output ports, LCD driver, a 8-bit AD converter, four multi-function timer/counters, two serial interfaces, and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP87CM24A	32 K × 8 bits	2 K 0 hita	D L OFD100 1414 0 F0C	TM/D07DD3//A
TMP87CP24A	48 K × 8 bits	2 K × 8 bits	P-LQFP100-1414-0.50C	TMP87PP24A

#### **Features**

- ◆8-bit single chip microcomputer TLCS-870 Series
- Instruction execution time: 0.5  $\mu$ s (at 8 MHz), 122  $\mu$ s (at 32 kHz)
- 129 types and 412 basic instructions
  - Multiplication and Division (8 bits  $\times$  8 bits , 16 bits  $\div$  8 bits): Execution time 3.5  $\mu$ s (at 8 MHz)
  - Bit manipulations (Set/Clear/Complement/Load/Store/Test/Exclusive OR)
  - 16-bit data operations
  - 1-byte jump/call (Short relative jump/Vector call)
- ◆14 interrupt sources (External: 5, Internal: 9)
   ◆ All sources have independent latches each,
  - and nested interrupt control is available
  - 4 edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆ 10-input/output ports (Max 69 pins)
- Two 16-bit timer/counters
  - Timer, Event counter, External trigger timer, Window, PPG output Pulse width measurement modes
- Two 8-bit timer/counters
  - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, PDO modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16384 kHz)
- ◆Divider output function (frequency: 1 kHz to 8 kHz)
- ► Watchdog Timer
- Two 8-bit Serial Interfaces
  - Each 8 bytes transmit/receive data buffer
  - Internal/external serial clock, and 4-/8-bit mode



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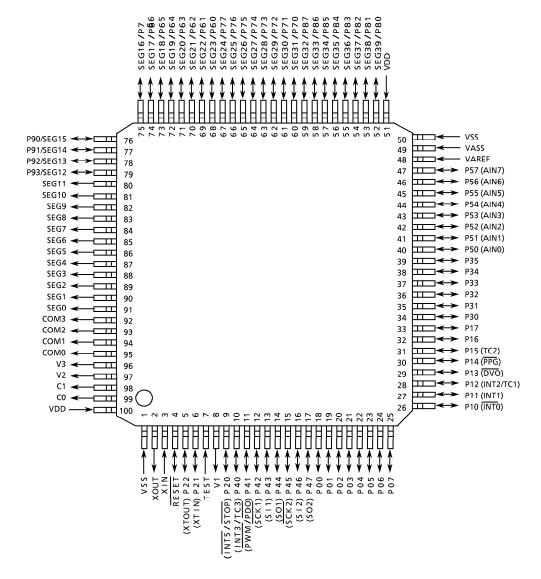
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- ◆LCD driver

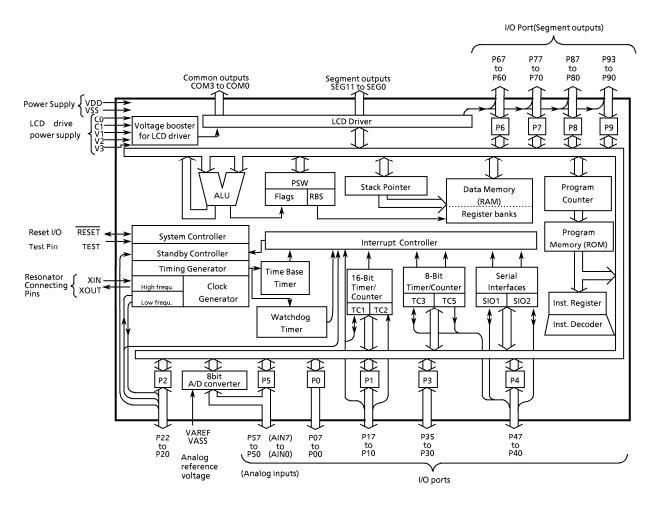
  - Built-in voltage booster for LCD driver
    With display memory (20 bytes)
    LCD direct drive capability (Max 40 seg × 4 com)
    1/4, 1/3, 1/2 duty or static drive are programmably selectable
- ◆8-bit successive approximate type AD converter with sample and hold
  - 8 analog inputs
  - Conversion time: 23  $\mu$ s/92  $\mu$ s (at 8 MHz)
- ◆Dual clock operation (optional)
- ◆ Five Power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - SLOW mode: Low power consumption operation using
    - low-frequency clock (32.768 kHz).
  - IDLE1 mode: CPU stops, and Peripherals operate using
    - high-frequency clock.
    - Release by interrupts.
  - IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock.
    - Release by interrupts.
  - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock.
    - Release by interrupts.
  - ◆Operating Voltage: 2.2 to 5.5 V at 4.2 MHz/32.768 kHz, 4.5 to 5.5 V at 8 MHz/32.768 kHz
  - ◆Emulation Pod: BM87CP24F0A

#### Pin Assignments (Top View)

P-LQFP100-1414-0.50C



## **Block Diagram**



# **Pin Functions**

Pin Name	Input/Output	Func	tion
P07 to P00 P17, P16	I/O	8-bit programmable input/output ports (tri-state).	
P15 (TC2)	I/O (Input)	Each bit of these ports can be individually	Timer/Counter 2 input
P14 (PPG)		configured as an input or an output under software control.	Programmable pulse generator output
P13 (DVO)	I/O (Output)	When used as an input port, timer/counter input or external interrupt input, the	Divider output
P12 (INT2/TC1)		POCR/P1CR must be set to "0". When used	External interrupt 2 input or Timer/Counter 1 input
P11 (INT1)	I/O (Input)	as timer/counter output or divider output, the POCR/P1CR must be set to "1" after	External interrupt 1 input
P10 (INTO)		setting output latch to "1".	External interrupt 0 input
	1/O (Output)	3-bit input/output port with latch.	Resonator connecting pins (32.768 kHz).
P22 (XTOUT)	I/O (Output)	When used as an input port, external	For inputting external clock, XTIN is used
P21 (XTIN)  P20 (INT5/STOP)	I/O (Input)	interrupt input or STOP mode release input, the output latch must be set to "1".	and XTOUT is opened.  External interrupt 5 input or STOP mode release signal input
P35 to P30	1/0	6-bit input/output port with latch. When used as input port, the output latch m	
P47 (SO2)	I/O (Output)		SIO2 serial data output
P46 (SI2)	I/O (Input)	8-bit input/output port with latch.	SIO2 serial data input
P45 (SCK2)	I/O (I/O)	When used as serial interface output or timer/counter output, the P4CR1 must be	SIO2 serial clock input/output
P44 (SO1)	I/O (Output)	set to "1" after setting output latch to "1". When used as an input port, serial	SIO1 serial data output
P43 (SI1)	I/O (Input)	interface input or external interrupt input,	SIO1 serial data input
P42 (SCK1)	I/O (I/O)	the P4CR1 must be set to "0".	SIO1 serial clock input/output
l			8-bit PWM output, 8-bit programmable
P41 (PWM/PDO)	I/O (Output)		divider output External interrupt 3 input, Timer/Counter
P40 (INT3/TC3)	I/O (Input)	O hit and an area his in a strong to a strong to a strong to a	3 input
P57 (AIN07) to P50 (AIN00)	I/O (Input)	8-bit programmable input/output port (tristate). Each bit of the port can be individually configured as an input or an output under software control. When used as analog input, the P5CR must be set to "0".	AD converter analog inputs
SEG39 (P80) to SEG32 (P87)	Output (I/O)	8-bit input/output port with latch.	LCD segment outputs. When used as
SEG31 (P70) to SEG24 (P77)	Output (I/O)	When used as an input port, the segment output control register must be set to "0"	segment output, the segment output
SEG23 (P60) to SEG16 (P67)	Output (I/O)	after setting output latch to "1".	control register must be set to "1".
SEG15 (P90) to SEG12 (P93)	Output (I/O)	4-bit input /output port with latch. When used as an input port, the segment output control register must be set to "0" after setting output latch to "1".	
SEG11 to SEG0	Output	LCD segment outputs	
COM3 to COM0	Output	LCD common outputs	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequen used and XOUT is opened.	cy clock. For inputting external clock, XIN is
RESET	I/O	Reset signal input or watchdog timer output	/address-trap-reset output
TEST	Input	Test pin for out-going test. Be fixed to low.	
VDD, VSS	Power Supply	+5V, 0V (GND)	
VAREF, VASS	Power Supply	Analog reference voltage inputs (High, Low)	
C0, C1, V1, V2, V3	LCD voltage booster pin	LCD voltage booster pin. Capacitors are red V1/V2/V3 pin and GND.	quired between C0 and C1 pin and between

### **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

### 1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM24A/P24A. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

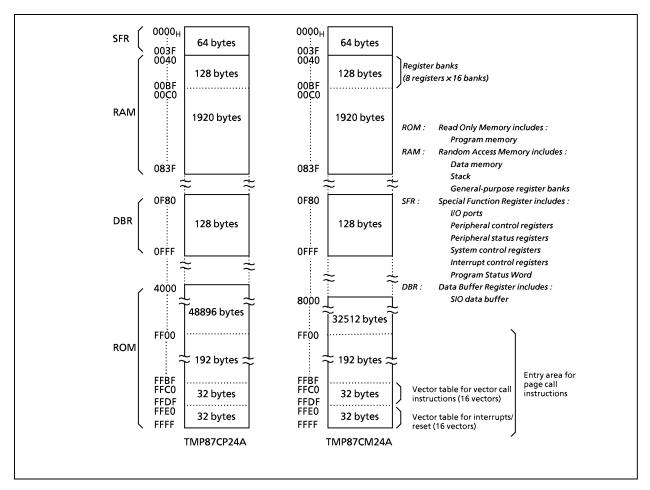


Figure 1-1. Memory Address Maps

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### **Electrical Characteristics**

**Absolute Maximum Ratings**  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	] ,,
Output Valtage	V <sub>OUT1</sub>	Except P20 and P3 ports	- 0.3 to V <sub>DD</sub> + 0.3	1 V
Output Voltage	V <sub>OUT2</sub>	Ports P20, P3	- 0.3 to 5.5	
Output Current (Per 1 pin)	I <sub>OUT1</sub>	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	3.2	
	I <sub>OUT2</sub>	P41	30	] .
Output Current (Total)	Σ l <sub>OUT1</sub>	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	120	mA
	Σ I <sub>OUT2</sub>	P41	30	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 125	ე •c
Operating Temperature	Topr		- 10 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V<sub>SS</sub> = 0 V, Topr = -10 to 70°C)

			ı			ı	
Parameter	Symbol	Pins	Conditions		Min	Max	Unit
			fo ONALL-	NORMAL1, 2 mode	4.5		
			fc = 8 MHz	IDLE1, 2 mode	4.5		
			fc = 4.2 MHz	NORMAL1, 2 mode			
Supply Voltage	$V_{DD}$		1C = 4.2 IVIHZ	IDLE1, 2 mode	2.2	5.5	
			fs =	SLOW mode	2.2		
			32.768 kHz	SLEEP mode			
				STOP mode	2.0		
	V <sub>IH1</sub>	Except hysteresis input	V <sub>DD</sub> ≥ 4.5 V V <sub>DD</sub> < 4.5 V		V <sub>DD</sub> × 0.70		
Input High Voltage	V <sub>IH2</sub>	Hysteresis input			$V_{DD} \times 0.75$	$V_{DD}$	
	V <sub>IH3</sub>				V <sub>DD</sub> × 0.90		
	V <sub>IL1</sub>	Except hysteresis input		/ > A E \/		$V_{DD} \times 0.30$	
Input Low Voltage	$V_{IL2}$	Hysteresis input	]	$V_{DD} \ge 4.5 V$ 0 $V_{DD} \ge 4.5 V$		$V_{DD} \times 0.25$	
	V <sub>IL3</sub>		V	/ <sub>DD</sub> <4.5 V		V <sub>DD</sub> × 0.10	
Clock Frequency	fo	VIN VOLIT	V <sub>DD</sub>	= 4.5 to 5.5 V	0.4	8.0	MHz
	cy fc XIN, XOUT		V <sub>DD</sub> = 2.2 to 5.5 V		0.4	4.2	IVITZ
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

#### **DC Characteristics**

 $(V_{SS} = 0 \text{ V, Topr} = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis inputs		_	0.9	_	٧
	I <sub>IN1</sub>	TEST					
Input Current	I <sub>IN2</sub>	Open-drain ports and tri-state ports	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V/0 V	_	_	± 2	μΑ
	I <sub>IN3</sub>	RESET, STOP					
Input Low Current	I <sub>IL</sub>	Push-pull ports	$V_{DD} = 5.5 \text{ V}, V_{IN} = 0.4 \text{ V}$	_	_	- 2	mΑ
Input Resistance	R <sub>IN2</sub>	RESET		100	220	450	kΩ
Output Leakage	I <sub>LO1</sub>	Open drain ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	-	_	2	
Current	I <sub>LO2</sub>	Tri-state ports	V <sub>OUT</sub> = 5.5 V/0 V	_	_	± 2	$\mu$ A
	V <sub>LCD1</sub>			0.75	1.0	1.33	
Segment/Common Output Voltage	V <sub>LCD2</sub>	SEG39 to SEG0 and COM3 to COM0		V <sub>LCD1</sub> ×2		2	1
Output Voltage	V <sub>LCD3</sub>	COIVIS to COIVIO		$V_{LCD1} \times 3$			
	V <sub>OH1</sub>	Push-pull ports (P4 port)	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -200 μA	2.4	_	_	v
Output High Voltage	V <sub>OH2</sub>	Tri- state ports (P0, P1, P5 ports)	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -0.7 mA	4.1	_	_	
Output Low Voltage	V <sub>OL</sub>	Except XOUT and P41	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	_	_	0.4	
Output Low Current	I <sub>OL3</sub>	P41	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	_	
Supply Current in NORMAL 1, 2 mode			V <sub>DD</sub> = 5.5 V fc = 8 MHz	_	10	16	mA
Supply Current in IDLE 1, 2 mode		fs = 32.768 kHz V <sub>IN</sub> = 5.3 V/0.2 V	10 0=11 00 1111	_	6	10	
Supply Current in SLOW mode	I <sub>DD</sub>		V <sub>DD</sub> = 3.0 V fs = 32.768 kHz	_	30	70	μΑ
Supply Current in SLEEP mode			V <sub>IN</sub> = 2.8 V/0.2 V Voltage boost frequency = 1 kHz	_	15	40	
Supply Current in STOP mode			V <sub>DD</sub> = 5.5 V V <sub>IN</sub> = 5.3 V/0.2 V	_	0.5	10	

Note 1: Typical values show those at  $Topr = 25^{\circ}C$ ,  $V_{DD} = 5 V$ .

Note 2: Input Current; The current through pull-up or pull-down resistor is not included.

Note 3:  $I_{DD}$ ; Except for  $I_{REF}$ 

Note 4: V<sub>LCD2</sub> indicates an output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.

Note 5:  $V_{LCD1}$  indicates an output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.

Note6: SEG/COM output voltage indicates an output voltage at no local.

Topr [°C]		$V_{LCD1}$		Unit
Topr [ C]	Min	typ.	Max	Unit
- 10	1.03	-	1.33	
25	0.85	1.0	1.15	V
70	0.75	-	1.00	

AD Conversion Characteristics (  ${\bf I}$  )

 $(Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit	
	V <sub>AREF</sub>		2.7	-	V <sub>DD</sub>		
Analog Reference Voltage	V <sub>ASS</sub>	$V_{AREF} - V_{ASS} \ge 2.5 V$	V <sub>SS</sub>	_	1.5	.,	
Analog Input Voltage	$\triangle$ V <sub>AREF</sub>		2.5	_	_	V	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_	V <sub>AREF</sub>		
Analog Supply Current	I <sub>REF</sub>	V <sub>AREF</sub> = 5.5 V, V <sub>ASS</sub> = 0.0 V	_	0.5	1.0	mA	
Nonlinearity Error			_	_	± 1		
Zero Point Error		$V_{DD} = 2.7 \text{ V to } 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1		
Full Scale Error		V <sub>AREF</sub> = 5.000 V, 2.700 V V <sub>ASS</sub> = 0.000 V	_	_	± 1	LSB	
Total Error			_	-	± 2		

Note: Quantizing error is not contained in those errors.

AD Conversion Characteristics (II)

 $(Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
	V <sub>AREF</sub>		2.2	-	V <sub>DD</sub>	
Analog Reference Voltage	V <sub>ASS</sub>		V <sub>SS</sub>			.,
Analog Input Voltage	$\triangle V_{AREF}$		2.2	_	_	V
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_	V <sub>AREF</sub>	
Analog Supply Current	I <sub>REF</sub>	V <sub>AREF</sub> = 5.5 V, V <sub>ASS</sub> = 0.0 V	_	0.5	1.0	mA
Nonlinearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = 2.2 \text{ V}, V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 2.200 \text{ V}$	_	_	± 2	
Full Scale Error		$V_{ASS} = 0.000 V$	_	_	± 2	LSB
Total Error			_	_	± 4	

Note: Quantizing error is not contained in those errors.

## AC Characteristics (I)

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit	
		In NORMAL1, 2 modes	٥٦		10		
Marshina Guela Tina		In IDLE 1, 2 modes	0.5	_	10		
Machine Cycle Time	t <sub>cy</sub>	In SLOW mode	447.6		422.2	$\mu$ S	
		In SLEEP mode	117.6	_	133.3		
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	F0				
Low Level Clock Pulse Width	t <sub>WCL</sub>	(XIN input), fc = 8 MHz	50	_	_	ns	
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation	14.7				
Low Level Clock Pulse Width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	14.7	ı	_	μS	

## AC Characteristics (II)

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.2 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		In NORMAL1, 2 modes	0.05		10	
Machine Curle Time	١.	In IDLE 1, 2 modes	0.95	_	10	
Machine Cycle Time	t <sub>cy</sub>	In SLOW mode	117.6		422.2	$\mu$ \$
		In SLEEP mode	117.6	_	133.3	
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	110			
Low Level Clock Pulse Width	t <sub>WCL</sub>	(XIN input), fc = 4.2 MHz	110	_	_	ns
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation	14.7			
Low Level Clock Pulse Width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	14.7	_	_	μ\$

## Recomended Oscillating Condition ( ${ m I}$ )

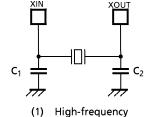
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

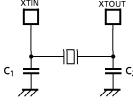
Parameter	Osillator	Frequency	Recommender	Recomr Cond	nended lition
			Oscillator	C <sub>1</sub>	C <sub>2</sub>
			KYOCERA KBR8.0M	30 pF	30 pF
			Standard/Lead Type CSA8.00MTZ	built-in	built-in
			(MURATA) CST8.00MTW	30 pF	30 pF
	Ceramic Resonator	8 MHz	Standard/SMP Type CSACS8.00MT (MURATA)	30 pF	30 pF
111			Standard/Small ChipType CSTCS8.00MT	built-in	built-in
High-			(MURATA)	30 pF	30 pF
frequency		4 MHz	KYOCERA KBR4.0MS	30 pF	30 pF
		8 MHz	TOYOCOM 210B 8.0000		
Crystal Oscillator		4 MHz	TOYOCOM 204B 4.0000	20 pF	20 pF
Low-frequency	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF

## Recomended OScillating Condition (II)

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.2 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$$

Parameter	Osillator	Frequency	Recommender Oscillator		Recomn Cond	
			Oscillato	or	C <sub>1</sub>	C <sub>2</sub>
			Standard/Lead Type	CSA4.00MG	30 pF	30pF
			(MURATA)	CST4.00MGW	built-in 30 pF	built-in 30 pF
High-	Ceramic Resonator	4 MHz	Standard/SMD Type (MURATA)	CSA4.00MGC CSAC4.00MGCM	30 pF	30 pF
frequency				CSTC4.00MG	built-in	built-in
					30 pF	30 pF
			Standard/Small Chin Type	CSTCS 4 DONAC	built-in	built-in
			Standard/Small Chip Type	C31C34.00IVIG	10 pF	10 pF





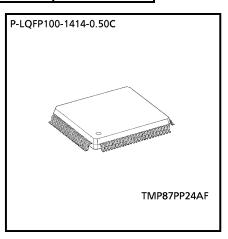
- (2) Low-frequency
- Note1: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.
- Note2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html

CMOS 8-Bit Microcontroller

### TMP87PP24AF

The TMP87PP24A is a One-Time PROM microcontroller with low-power 384 Kbits electrically programmable read only memory for the TMP87CM24A/CP24A system evaluation. The TMP87PP24A is pin compatible with the TMP87CM24A/CP24A. The operations possible with the TMP87CM24A/CP24A can be performed by writing programs to PROM. The TMP87PP24A can write and verify in the same way as the TMM571000D using an adaptor socket BM11127 and an EPROM programmer.

Pro	oduct No.	OTP	RAM	Package	OTP Adapter
TMF	87PP24AF	48 K × 8 bits	2 K × 8 bits	P-LQFP100-1414-0.50C	BM11127



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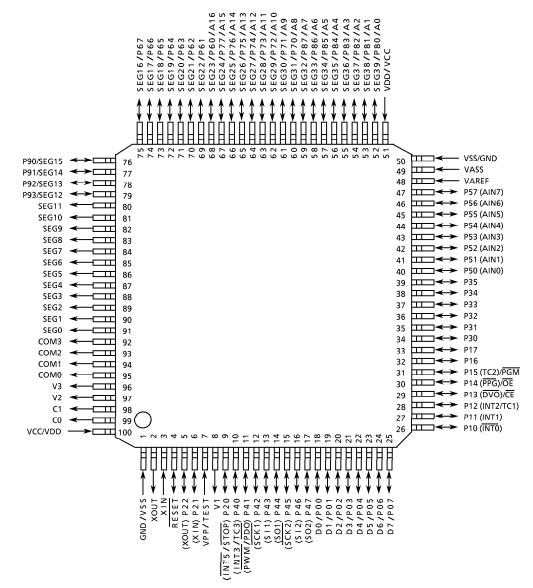
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### Pin Assignments (Top View)

P-LQFP100-1414-0.50C



## **Pin Function**

The TMP87PP24A has two modes: MCU and PROM.

(1) MCU mode
In this mode, the TMP87PP24A is pin compatible with the TMP87CM24A/CP24A (fix the TEST pin at low level.)

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Function	Pin Name (MCU mode)			
A16			P60			
A15 to A8	Input	PROM address inputs	P77 to P70			
A7 to A0			P87 to P80			
D7 to D0	I/O	PROM data input/outputs	P07 to P00			
CE		Chip enable signal input (active low)	P13			
ŌĒ	Input	Output enable signal input (active low)	P14			
PGM			P15			
VPP		+ 12.75 V/5 V (Program supply voltage)	TEST			
vcc	Power supply	+ 6.25 V/5 V	VDD			
GND		0 V	VSS			
P35 to P30						
P47 to P40						
P57 to P50		Pull-up with resistance for input processing.				
P67 to P62						
P93 to P90						
P11	I/O					
P21						
P31		PROM mode setting pin. Be fixed at high level.				
P61						
P17, P16, P12, P10 P22, P20						
RESET		PROM mode setting pin. Be fixed at low level.				
XIN	Input					
хоит	Output	Connect an 8 MHz oscillator to stabilize the inter	nal state.			
VAREF		21/(21/2)				
VASS	Power supply	0 V (GND)				
COM3 to COM0	Outro					
SEG11 to SEG0	Output	Open				
C0, C1, V1, V2, V3	Power supply					

#### **Operational Description**

The following explains the TMP87PP24A hardware configuration and operation. The configuration and functions of the TMP87PP24A are the same as those of the TMP87CM24A/CP24A, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PP24A is placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

## 1. Operating Mode

The TMP87PP24A has two modes: MCU and PROM.

#### 1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

In the MCU mode, operation is the same as with the TMP87CM24A/CP24A (the TEST/VPP pin cannot be used open because it has no built-in pull-down resistance).

#### 1.1.1 Program Memory

The TMP87PP24A has a  $48K \times 8$ -bit (addresses  $4000_H$  to FFFF<sub>H</sub> in the MCU mode, addresses  $14000_H$  to 1FFFF<sub>H</sub> in the PROM mode) of program memory (OTP).

When the TMP87PP24A is used as a system evaluation of the TMP87CM24A/CP24A, the data is written to the program storage area show in Figure 1-1.

Note: Either write the data  $FF_H$  to the unused area or set the PROM programmer to access only the program storage area.

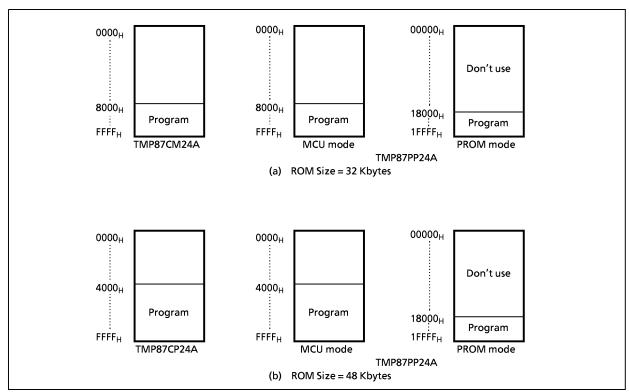


Figure 1-1. Program Memory Area

## 1.1.2 Data Memory

The TMP87PP24A has an on-chip 2K × 8-bit data memory (static RAM).

# 1.1.3 Input/Output Circuitry

## (1) Control pins

The control pins of the TMP87PP24A are the same as those of the TMP87CM24A/CP24A except that the TEST pin has no built-in pull-down resistance.

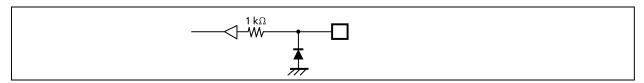


Figure 1-2. TEST Pin

## (2) I/O ports

The I/O circuits of TMP87PP24A I/O ports the are the same as the those of TMP87CM24A/CP24A.

#### 1.2 PROM Mode

The PROM mode is activated by setting the TEST, RESET pin and the ports P17 to P10, P22 to P20 and P61 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

Note: The high-speed programming mode can be used for program operation.

The TMP87PP24A is not supported an electric signature mode, so the ROM type must be set to TC571000D.

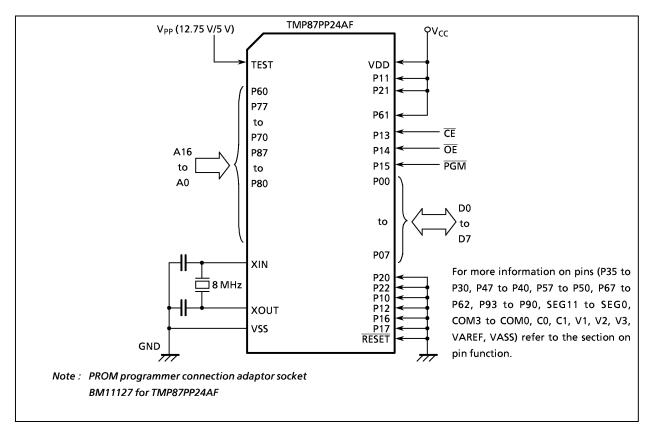


Figure 1-3. Setting for PROM Mode

## 1.2.1 Programming Flowchart (High-speed Programming Mode)

The high-speed programming mode is achieved by applying the program voltage ( $\pm$  12.75 V) to the VPP pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1 ms program pulse to the  $\overline{PGM}$  input. The programmed data is verified. If incorrect, another 0.1 ms program pulse is applied. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

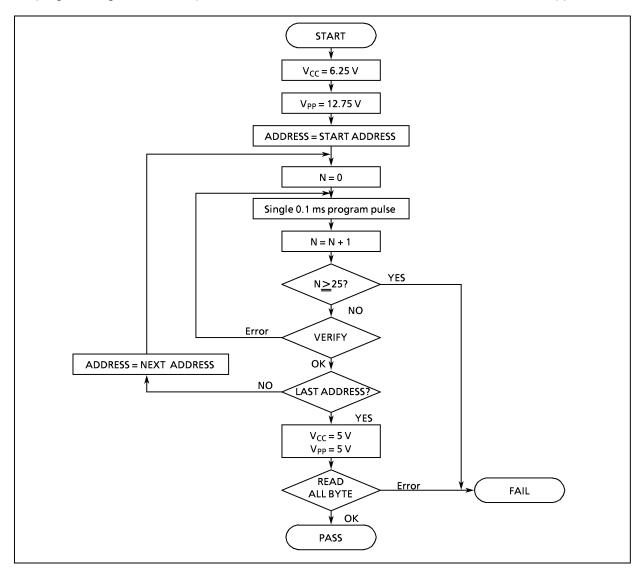


Figure 1-4. Flow Chart of High-speed Programming

### 1.2.2 Writing Method for General-purpose PROM Program

(1) Adapters

BM11127: TMP87PP24AF

(2) Adapter setting Switch (SW1) is set to side N.

(3) PROM programmer specifying

i) PROM type is specified to TC571000D.

Writing voltage: 12.75 V (high-speed program mode)

ii) Data transfer (copy) (note 1)

In the TMP87PP24A, EPROM is within the addresses 14000<sub>H</sub> to 1FFFF<sub>H</sub>. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.

ROM capacity of 48KB: transferred addresses 04000<sub>H</sub> to 0FFFF<sub>H</sub> to addresses 14000 to 1FFFF<sub>H</sub>

iii) Writing address is specified. (Note 1)

Start address: 14000<sub>H</sub> End address: 1FFFF<sub>H</sub>

(4) Writing

Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

- Note 1: The specifying method is referred to the PROM programmer description. Either write the data  $FF_H$  to the unused area or set the PROM programmer to access only the program storage area.
- Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.
- Note 3: The TMP87PP24A does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying  $12V \pm 0.5V$  to the address pin 9 (A9). The signature must not be used.

### **Electrical Characteristics**

**Absolute Maximum Ratings** 

 $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Ratings	Unit	
Supply Voltage	$V_{DD}$		- 0.3 to 6.5		
Program Voltage	V <sub>PP</sub>	TEST/V <sub>PP</sub>	- 0.3 to 13.0		
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	] v	
Output Voltage	V <sub>OUT1</sub>	Except P20 and P3 ports	- 0.3 to V <sub>DD</sub> + 0.3		
Output Voltage	V <sub>OUT2</sub>	Ports P20, P3	- 0.3 to 5.5		
Output Current (Per 1 pin)	I <sub>OUT1</sub>	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	3.2		
	I <sub>OUT2</sub>	P41	30		
Output Current (Total)	Σ l <sub>OUT1</sub>	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	120	mA	
	Σ I <sub>OUT2</sub>	P41	30		
Power Dissipation [Topr = 70°C]	PD		350	mW	
Soldering Temperature (time)	Tsld		260 (10 s)		
Storage Temperature	Tstg		– 55 to 125	] ℃	
Operating Temperature	Topr		– 10 to 70		

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Operating Conditions** 

 $(V_{SS} = 0V, Topr = -10 to 70^{\circ}C)$ 

Parameter	Symbol	Pins		Conditions	Min	Max	Unit		
			fo ONALL	NORMAL1, 2 mode	4.5				
			fc = 8 MHz	IDLE1, 2 mode	4.5				
			NORMAL1, 2 mode						
Supply Voltage	$V_{DD}$		fc = 4.2 MHz	IDLE1, 2 mode	2.2	5.5			
			fs =	SLOW mode	2.2				
			32.768 kHz	SLEEP mode			V		
				STOP mode	2.0				
	V <sub>IH1</sub>	Except hysteresis input	V <sub>DD</sub> ≧ 4.5 V		$V_{DD} \times 0.70$		٧		
Input High Voltage	V <sub>IH2</sub>	Hysteresis input			$V_{DD} \times 0.75$	V <sub>DD</sub>			
	V <sub>IH3</sub>		V	<sub>DD</sub> <4.5 V	$V_{DD} \times 0.90$				
	$V_{IL1}$	Except hysteresis input		′ <sub>DD</sub> ≧4.5 V		$V_{DD} \times 0.30$			
Input Low Voltage	$V_{IL2}$	Hysteresis input	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	DD = 4.5 V	0	$V_{DD} \times 0.25$			
	$V_{IL3}$		V	<sub>DD</sub> <4.5 V		$V_{DD} \times 0.10$			
	fc	XIN, XOUT	V <sub>DD</sub> = 4.5 to 5.5 V		V <sub>DD</sub> = 4.5 to 5.5 V		0.4	8.0	MHz
Clock Frequency	١,	AIN, AUUT	V <sub>DD</sub>	V <sub>DD</sub> = 2.2 to 5.5 V		4.2	IVITZ		
	fs	XTIN, XTOUT			30.0	34.0	kHz		

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

#### **DC Characteristics**

 $(V_{SS} = 0 \text{ V, Topr} = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis inputs		-	0.9	_	٧
	I <sub>IN1</sub>	TEST					
Input Current	I <sub>IN2</sub>	Open drain ports and tri-state ports	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V/0 V	_	_	± 2	μΑ
	I <sub>IN3</sub>	RESET, STOP					
Input Resistance	R <sub>IN2</sub>	RESET		100	220	450	kΩ
Output Leakage	I <sub>LO1</sub>	Open drain ports	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	-	_	2	
Current	I <sub>LO2</sub>	Hysteresis inputs  TEST  Open drain ports and tri-state ports  RESET, STOP  RESET  LO1 Open drain ports  LC2 Tri-state ports  LCD2 SEG39 to SEG0 and COM3 to COM0  COM3 to COM0  Tri-state ports  YOH2 Tri-state ports  (P0, P1, P5 ports)  VOL Except XOUT and P41  DATE OF THE NAME of TAX PART OF THE NAME of TAX PART OF T	V <sub>OUT</sub> = 5.5 V/0 V	-	_	± 2	μA
	V <sub>LCD1</sub>			0.75	1.0	1.33	
Segment/Common Output Voltage	V <sub>LCD2</sub>			'	V <sub>LCD1</sub> × 2	2	
output voltage	V <sub>LCD3</sub>			V <sub>LCD1</sub> × 3			
Output High Voltage -	V <sub>OH1</sub>	Push-pull ports (P4 port)	$V_{DD} = 4.5 \text{ V}, I_{OH} = -200 \mu\text{A}$	2.4	_	_	V
	V <sub>OH2</sub>		$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	-	
Output Low Voltage	V <sub>OL</sub>	Except XOUT and P41	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	_	_	0.4	
Output Low Current	I <sub>OL3</sub>	P41	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	_	
Supply Current in NORMAL 1, 2 mode			V <sub>DD</sub> = 5.5 V fc = 8 MHz	_	12	18	mA
Supply Current in IDLE 1, 2 mode			fs = 32.768 kHz V <sub>IN</sub> = 5.3 V/0.2 V	_	6	10	
Supply Current in SLOW mode  Supply Current in SLEEP mode		V <sub>DD</sub> = 3.0 V fs = 32.768 kHz	_	31	70		
			V <sub>IN</sub> = 2.8 V/0.2 V Voltage boost frequency = 1 kHz	_	16	40	μΑ
Supply Current in STOP mode			$V_{DD} = 5.5 V$ $V_{IN} = 5.3 V/0.2 V$	_	0.5	10	

Note 1: Typical values show those at  $Topr = 25^{\circ}C$ ,  $V_{DD} = 5 V$ .

 $Note\ 2:\ Input\ Current\ ;\ The\ current\ through\ pull-up\ or\ pull-down\ resistor\ is\ not\ included.$ 

Note 3:  $I_{DD}$ ; Except for  $I_{REF}$ 

Note 4:  $V_{LCD2}$  indicates an output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.

Note 5:  $V_{LCD1}$  indicates an output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.

AD Conversion Characteristics (I)

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
	V <sub>AREF</sub>		2.7	_	V <sub>DD</sub>	
Analog Reference Voltage	V <sub>ASS</sub>		V <sub>SS</sub>	_	1.5	V
Analog Input Voltage	V <sub>AIN</sub>		V <sub>ASS</sub>	_	V <sub>AREF</sub>	
Analog Supply Current	I <sub>REF</sub>	$V_{AREF} = 5.5 \text{ V}, \ V_{ASS} = 0.0 \text{ V}$	_	0.5	1.0	mA
Nonlinearity Error		$V_{DD} = 5.0 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1	
Zero Point Error		V <sub>AREF</sub> = 5.000 V V <sub>ASS</sub> = 0.000 V	_	_	± 1	
Full Scale Error		or $V_{DD} = 2.7 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 1	LSB
Total Error		V <sub>AREF</sub> = 2.700 V V <sub>ASS</sub> = 0.000 V	_	_	± 2	

Note: Quantizing error is not contained in those errors.

AD Conversion Characteristics (II)

 $(V_{SS} = 0V, V_{DD} = 2.2 \text{ to } 2.7V, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
	V <sub>AREF</sub>		2.2	_	V <sub>DD</sub>	
Analog Reference Voltage	V <sub>ASS</sub>		Vs	ŝ		
Analog Reference Voltage Range	$\triangle V_{AREF}$		2.2	_	_	V
Analog Input Voltage	$V_{AIN}$		V <sub>ASS</sub>	_	V <sub>AREF</sub>	
Analog Supply Current	I <sub>REF</sub>	$V_{AREF} = 5.5 \text{ V}, \ V_{ASS} = 0.0 \text{ V}$	_	0.5	1.0	mA
Nonlinearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = 2.2 \text{ V}, V_{SS} = 0.0 \text{ V}$	_	_	± 2	
Full Scale Error		V <sub>AREF</sub> = 2.200 V	_	_	± 2	LSB
Total Error		V <sub>ASS</sub> = 0.000 V	_	_	± 4	

Note: Quantizing error is not contained in those errors.

## AC Characteristics (I)

 $(V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 5.5V, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	0.05		10	
Machine Cycle Time	t <sub>cy</sub>	In IDLE 1, 2 mode	0.95	_		
		In SLOW mode	447.6		422.2	$\mu$ S
		In SLEEP mode	117.6	_	133.3	
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation				
Low Level Clock Pulse Width	t <sub>WCL</sub>	(XIN input), fc = 8 MHz	50	_	_	ns
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation	14.7			
Low Level Clock Pulse Width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	14.7	_	-	μS

## AC Characteristics (II)

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.2 \text{ to } 5.5 \text{ V}, \text{Topr} = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	0.05		10	
Machine Cycle Time	t <sub>cy</sub>	In IDLE 1, 2 mode	0.95	_		
		In SLOW mode	117.6		133.3	$\mu$ s
		In SLEEP mode	117.6	_		
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation	440			
Low Level Clock Pulse Width	t <sub>WCL</sub>	(XIN input), fc = 4.2 MHz	110	_	_	ns
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation	14.7			
Low Level Clock Pulse Width	t <sub>WSL</sub>	(XTIN input), fs = 32.768 kHz	14.7	_	_	μS

Recomended Oscillating Condition (I)

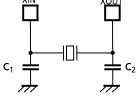
 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$ 

Parameter	Osillator	Frequency	Recomm Oscill		Recomn Cond	
				ator	C <sub>1</sub>	C <sub>2</sub>
			KYOCERA	KBR8.0M	30pF	30pF
			Standard/Lead Type	CSA8.00MTZ	built-in	built-in
			(MURATA)	CST8.00MTW	30pF	30pF
	Ceramic Resonator	8 MHz	Standard/SMP Type (MURATA)	CSAC8.00MT	30pF	30pF
			Standard/Small ChipTyp	e CSTC8.00MT	built-in	built-in
High-			(MURATA)		30pF	30pF
frequency		4 MHz	KYOCERA	KBR4.0MS	30pF	30pF
		8 MHz	тоуосом	210B 8.0000		
	Crystal Oscillator	4 MHz	TOYOCOM 204B 4.0000		20pF	20pF
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15pF	15pF

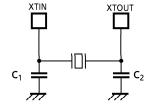
Recomended Oscillating Condition (II)

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.2 \text{ to } 5.5 \text{ V}, Topr = -10 \text{ to } 70^{\circ}\text{C})$$

Parameter	Osillator	Frequency	Recommender Oscillator		Recomn Cond	ition
					C <sub>1</sub>	C <sub>2</sub>
			Standard/Lead Type	CSA4.00MG	30pF	30pF
			(MURATA)	CST4.00MGW	built-in 30pF	built-in 30pF
High-	Ceramic Resonator	4 MHz	Standard/SMD Type (MURATA)	CSA4.00MGC CSAC4.00MGCM	30pF	30pF
frequency				CSTC4.00MG	built-in	built-in
					30pF	30pF
			Standard/Small Chin Tuna	CCTCC4 OONAC	built-in	built-in
			Standard/Small Chip Type	C31C34.00IVIG	10pF	10pF



(1) High-frequency



(2) Low-frequency

Note1: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Note2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html

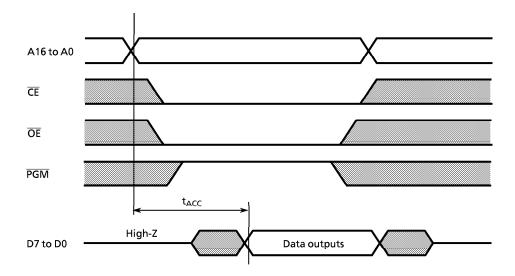
DC/AC Characteristics (PROM mode)

 $(V_{SS} = 0 V)$ 

# (1) Read Operation

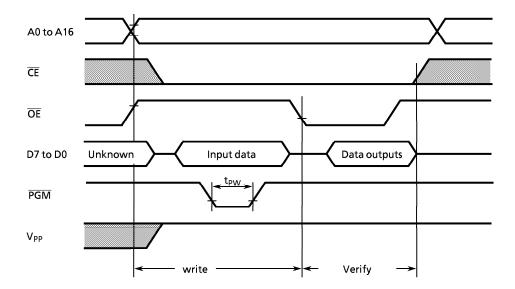
Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	_	V <sub>CC</sub>	
Input Low Voltage	V <sub>IL4</sub>		0	_	V <sub>CC</sub> × 0.12	V
Power Supply Voltage	V <sub>CC</sub>		4.75	5.0	5.25	
Program Power Supply Voltage	$V_{PP}$		4.75	5.0	5.25	
Address Access Time	t <sub>ACC</sub>	V <sub>CC</sub> = 5.0 ± 0.25V	_	1.5tcyc + 300	_	ns

Note: tcyc = 500 ns at 8 MHz



## (2) High-Speed Programming Operation (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input High Voltage	V <sub>IH4</sub>		V <sub>CC</sub> × 0.7	1	V <sub>CC</sub>	
Input Low Voltage	V <sub>IL4</sub>		0	ı	V <sub>CC</sub> × 0.12	v
Power Supply Voltage	V <sub>CC</sub>		6.0	6.25	6.5	
Program Power Supply Voltage	V <sub>PP</sub>		12.5	12.75	13.0	
Initial Program Pulse Width	t <sub>PW</sub>	V <sub>CC</sub> = 6.0 V	0.095	0.1	0.105	ms



- Note 1: When  $V_{cc}$  power supply is turned on or after,  $V_{pp}$  must be increased. When  $V_{cc}$  power supply is turned off or before,  $V_{pp}$  must be increased.
- Note 2: The device must not be set to the EPROM programmer or picked op from it under applying the program voltage (12.5 V  $\pm$  0.5 V = V) to the  $V_{pp}$  pin as the device is damaged.
- Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.