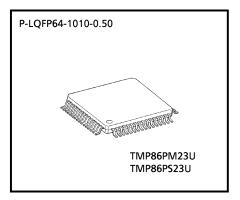
CMOS 8-Bit Microcontroller

# **TMP86PM23U, TMP86PS23U**

The TMP86PM23 is a OTP type MCU which includes 32-Kbyte one-time PROM; the TMP86PS23 is a OTP type MCU which includes 60-Kbyte one-time PROM. These are a pin compatible with a mask ROM product of the TMP86CM23/CP23. Writing the program to built-in PROM, the TMP86PM23/PS23 operates as the same way as the TMP86CM23/CP23. Using the Adapter socket, you can write and verify the data for the TMP86PM23 with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	ОТР	RAM	Package	Adapter Socket
TMP86PM23U	32 K × 8 bits	1.5 K × 8 bits	P-LOFP64-1010-0.50	*BM11198
*TMP86PS23U	60 K × 8 bits	2.0 K × 8 bits		*DIVIT 1 790

\* Under Development



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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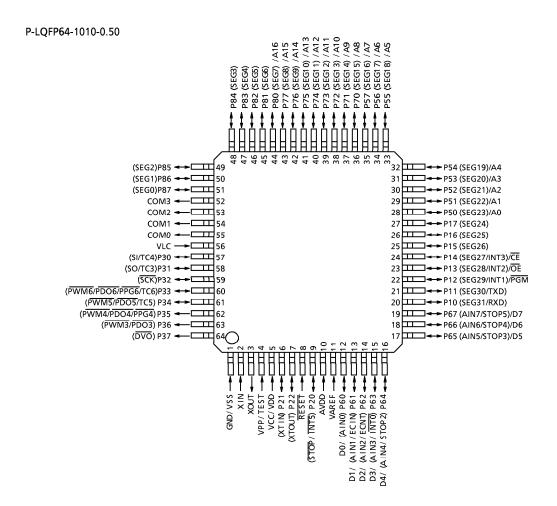
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## Pin Assignments (Top View)



## **Pin Functions**

The TMP86PM23/PS23 have MCU mode and PROM mode.

# (1) MCU mode

In the MCU mode, the TMP86PM23/PS23 are a pin compatible with the TMP86CM23/CP23 (Make sure to fix the TEST pin to low level).

# (2) PROM mode

Pin Name	Input/Output	Function	Pin Name (MCU mode)			
A16			P80			
A15 to A8	Input	Input of Memory address for program	P77 to P70			
A7 to A0			P57 to P50			
D7 to D0	1/0	Input/Output of Memory data for program	P67 to P60			
CE		Chip enable	P14			
ŌĒ	Input	Output enable	P13			
PGM		Program mode control	P12			
VPP		+ 12.75 V/5 V (Power supply of program)	TEST			
vcc		+ 6.25 V/5 V	VDD			
GND		0 V	VSS			
AVDD	··· Power supply	Be pull-up to High level.	AVDD			
VAREF		Be pull-down to Low level.	VAREF			
VLC		Open or release.	VLC			
P11, P21		PROM mode setting pin. Be pull-up to High level.	•			
P15, P20, P22 RESET	Input	PROM mode setting pin. Be fixed at Low level.				
P10	Input	Be fixed at Low level.				
P16, P17	Output	Output pin for PROM operation test. Open or release				
P87 to P81	1/0					
P37 to P30	1/0	Open or release.				
COM3 to COM0	Output					
XIN	Input	Self oscillation with resonator (16 MHz).				
XOUT	Output	Seri oscillation with resonator (10 Will2).				

## Operation

This section describes the functions and basic operational blocks of TMP86PM23.

The TMP86PM23/PS23 have PROM in place of the mask ROM which is included in the TMP86CM23/CP23. The configuration and function are the same as the mask ROM products.

In addition, TMP86PM23/PS23 operate as the single clock mode when releasing reset.

When using the dual clock mode, oscillate a low-frequency clock by SET. XTEN command at the beginning of program.

#### 1. Operating Mode

The TMP86PM23/PS23 have MCU mode and PROM mode.

#### 1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resister) and the TMP86PS23 has a 60Kbyte built-in one time PROM (addresses 1000 to FFFF<sub>H</sub> in MCU mode, addresses 0000 to EFFF<sub>H</sub> in the PROM mode).

#### 1.1.1 Program memory

The TMP86PM23 has a 32 Kbyte built-in one time PROM (addresses 8000 to FFFF $_{\rm H}$  in the MCU mode, addresses 0000 to 7FFF $_{\rm H}$  in the PROM mode) and the TMP86PS23 has a 60-Kbyte built-in one time PROM (addressed 1000 to FFFF $_{\rm H}$  in MCU mode, addresses 0000 to EFFF $_{\rm H}$  in the PROM mode).

When using TMP86PM23/PS23 for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

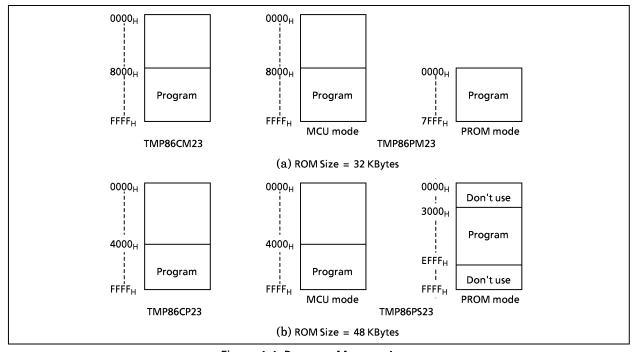


Figure 1-1. Program Memory Area

Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

#### 1.1.2 Data Memory

TMP86PM23 has a built-in 1.5 Kbyte Data memory and TMP86PS23 has a built-in 2-Kbyte data memory (static RAM).

#### **Electrical Characteristics**

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	
Program Voltage	V <sub>PP</sub>	TEST/V <sub>PP</sub>	- 0.3 to 13.0	] ,
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	]
Output Voltage	V <sub>OUT1</sub>		- 0.3 to V <sub>DD</sub> + 0.3	
	I <sub>OUT1</sub>	P1, P30 to P34, P5, P6, P7, P8 Port	- 1.8	
Output Current (Per 1 pin)	I <sub>OUT2</sub>	P1, P2, P30 to P32, P5, P6, P7, P8 Port	3.2	
	I <sub>OUT3</sub>	P33 to P37 Port	30	mA
	Σl <sub>OUT1</sub>	P1, P30 to P34, P5, P6, P7, P8 Port	- 30	] '''′
Output Current (Total)	ΣI <sub>OUT2</sub>	P33 to P37 Port	80	
	ΣI <sub>OUT3</sub>	P1, P2, P30 to P32, P5, P6, P7, P8 Port	60	]
Power Dissipation [T <sub>opr</sub> = 85°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 μ)	
Storage Temperature	Tstg		– 55 to 125	°c
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant.

Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

**Recommended Operating Condition** 

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	С	ondition	Min	Max	Unit		
				NORMAL1, 2 mode	2.5				
			fc = 16 MHz	IDLE0, 1, 2 mode	3.5				
			6 0 0 0 0 1	NORMAL1, 2 mode	2.7				
			fc = 8 MHz	IDLE0, 1, 2 mode	2.7				
Supply Voltage	v V <sub>DD</sub>			NORMAL1, 2 mode		5.5			
			fc = 4.2 MHz	IDLE0, 1, 2 mode					
			fs =	SLOW1, 2 mode	1.8				
			32.768 kHz	SLEEP0, 1, 2 mode					
				STOP mode			V		
	V <sub>IH1</sub>	Except Hysteresis input		> 4 5 1/	$V_{DD} \times 0.70$				
Input high Level	V <sub>IH2</sub>	Hysteresis input	$V_{DD} \ge 4.5 V$		V <sub>DD</sub> = 4.3 V		$V_{DD} \times 0.75$	$V_{DD}$	
	V <sub>IH3</sub>		V <sub>D</sub>	<sub>DD</sub> < 4.5 V	$V_{DD} \times 0.90$				
	V <sub>IL1</sub>	Except Hysteresis input		<sub>DD</sub> ≧ 4.5 V		$V_{DD} \times 0.30$			
Input low Level	$V_{IL2}$	Hysteresis input	V D	0D ≡ 4.3 V	0	$V_{DD} \times 0.25$			
	V <sub>IL3</sub>		V <sub>D</sub>	<sub>DD</sub> < 4.5 V		$V_{DD} \times 0.10$			
			V <sub>DD</sub> =	= 1.8 to 5.5 V		4.2			
Clock Frequency	fc	XIN, XOUT	V <sub>DD</sub> = 2.7 to 5.5 V		1.0	8.0	MHz		
Clock Frequency			V <sub>DD</sub> = 3.5 to 5.5 V			16.0			
	fs	XTIN, XTOUT			30.0	34.0	kHz		

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

**DC Characteristics** 

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Condit	ion	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input			_	0.9	_	V
	I <sub>IN1</sub>	TEST						
Input Current	I <sub>IN2</sub>	Sink open drain, Tri-state $V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$		-	-	± 2	μA	
	I <sub>IN3</sub>	RESET, STOP						
Input Resistance	R <sub>IN2</sub>	RESET pull-Up			100	220	450	kΩ
Output Leakage Current	I <sub>LO</sub>	Sink open drain, Tri-state	$V_{DD} = 5.5  V,  V_{OUT}$		ı	-	± 2	μΑ
Output High Voltage	V <sub>OH2</sub>	C-MOS, Tri-st Port	$V_{DD} = 4.5 \text{ V, } I_{OH} =$		4.1	_	-	<sub>V</sub>
Output Low Voltage	V <sub>OL</sub>	Except XOUT and P3 Port	$V_{DD} = 4.5 \text{ V, } I_{OL} =$	1.6mA	_	-	0.4	v
Output Low Current	I <sub>OL</sub>	High Current Port (P33 to P37 Port)	$V_{DD} = 4.5  V,  V_{OL} = 4.5  V_{DD} = 4.5  V$	= 1.0 V	ı	20	_	
Supply Current in NORMAL 1, 2 mode			$V_{DD} = 5.5 V$ $V_{IN} = 5.3/0.2 V$		-	11.5	16.5	mA
Supply Current in IDLE 0, 1, 2 mode			fc = 16 MHz fs = 32.768 kHz	s = 32.768 kHz V <sub>DD</sub> = 3.0 V V <sub>IN</sub> = 2.8 V/0.2 V s = 32.768 kHz CD driver is	-	7.0	11.0	
Supply Current in SLOW 1 mode	V <sub>DD</sub>		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$		ı	19	33	μΑ
Supply Current in SLEEP 1 mode			fs = 32.768 kHz LCD driver is not enable.		ı	13	26	
Supply Current in SLEEP 0 mode			not enable.		-	5	14	
Supply Current in NORMAL 1, 2 mode			$V_{DD} = 5.5 V$ $V_{IN} = 5.3/0.2 V$		ı	T.B.D	T.B.D	mA
Supply Current in IDLE 0, 1, 2 mode			fc = 16 MHz fs = 32.768 kHz	TMP86PS23	ı	T.B.D	T.B.D	
Supply Current in SLOW 1 mode	V <sub>DD</sub>		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$		-	T.B.D	T.B.D	PΑ
Supply Current in SLEEP 1 mode			fs = 32.768 kHz LCD driver is not enable.		-	T.B.D	T.B.D	
Supply Current in SLEEP 0 mode			not enable.		ı	T.B.D	T.B.D	
Supply Current in STOP mode			$V_{DD} = 5.5 V$ $V_{IN} = 5.3 V/0.2 V$		1	0.5	10	
Segment Output Low Resistance	R <sub>OS1</sub>	SEG Pin			-	20	_	
Common Output Low Resistance	R <sub>OC1</sub>	COM Pin			ı	20	-	 
Segment Output High Resistance	R <sub>OS2</sub>	SEG Pin			ı	200	_	kΩ
Common Output High Resistance	R <sub>OC2</sub>	COM Pin			-	200	-	
C	V <sub>O2/3</sub>		V - F 0 V		3.8		4.2	
Segment/Common Output Voltage	V <sub>O1/2</sub>	SEG/COM Pin	V <sub>DD</sub> = 5.0 V VLC = 2.0 V	$V_{DD} = 5.0 \text{ V}$		_	3.7	] v
1	V <sub>O1/3</sub>		VLC = 2.0 V		2.8		3.2	

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 \text{ V}$ 

Note 2: Input current (I<sub>IN1</sub>, I<sub>IN2</sub>); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

Note 5: Output resistors ROs and ROC indicate "ON" when switching levels.

Note 6: VO2/3 indicates the output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.

Note 7:  $V_{O1/2}$  indicates the output voltage at the 1/2 level when operating in the 1/2 duty or static mode.

Note 8:  $V_{O1/3}$  indicates the output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.

Note 9: When using LCD, it is necessary to consider values of Ros 1/2 and Roc 1/2.

# **AD Conversion Characteristics**

## $(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V} \le V_{DD} \le 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	$V_{AREF}$		A <sub>VDD</sub> - 1.0	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit (Note 6)	A <sub>VDD</sub>			V <sub>DD</sub>		v
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$		3.5	-	_	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.6	1.0	mA
Non linearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V},$	_	_	± 2	1
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 5.0 \text{ V}$	_	_	± 2	LSB
Total Error		TAINEI THE	-	-	± 2	

# $(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} < 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		A <sub>VDD</sub> - 1.0	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit (Note 6)	A <sub>VDD</sub>			V <sub>DD</sub>		v
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$		2.5	-	_	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	-	0.5	0.8	mA
Non linearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 2.7 \text{ V},$	-	-	± 2	LCD
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 2.7 \text{ V}$	-	-	± 2	LSB
Total Error		AMEI	-	-	± 2	

# (V<sub>SS</sub> = 0.0 V, 2.0 V $\leqq$ V<sub>DD</sub> <2.7 V, Topr = -40 to 85°C) Note 5 (V<sub>SS</sub> = 0.0 V, 1.8 V $\leqq$ V<sub>DD</sub> <2.0 V, Topr = -10 to 85°C) Note 5

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>		A <sub>VDD</sub> - 0.9	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit (Note 6)	A <sub>VDD</sub>			$V_{DD}$		.,
Analog Reference Voltage Range (Note 4)	Λv	$1.8 \text{ V} \le \text{V}_{DD} < 2.0 \text{ V}$	1.8	-	_	V
Analog Reference Voltage Range (Note 4)	$\triangle v_{AREF}$ -	$2.0 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	2.0	-	-	
Analog Input Voltage	V <sub>AIN</sub>		V <sub>SS</sub>	-	V <sub>AREF</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	_	0.3	0.5	mA
Non linearity Error			_	-	± 4	
Zero Point Error		$V_{DD} = A_{VDD} = 1.8 \text{ V},$	_	-	± 4	LCD
Full Scale Error		$V_{SS} = 0.0 \text{ V}$ $V_{AREF} = 1.8 \text{ V}$	_	-	± 4	LSB
Total Error		AILI	_	-	± 4	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Conversion time is different in recommended value by power supply voltage.

About conversion time, please refer to "2.10.2 Register Framing".

Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub> - V<sub>SS</sub>.

When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel

conversion value.

- Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = V_{AREF} V_{SS}$ Note 5: When AD is used with  $V_{DD} < 2.7 V$ , the guaranteed temperature range varies with the operating voltage. Note 6: The AVDD pin should be fixed on the VDD level even though AD converter is not used.

**AC Characteristics** 

 $(V_{SS} = 0 \text{ V}, V_{DD} = 3.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
	tcy	NORMAL 1, 2 mode				
Machine Cycle Time		IDLE 1, 2 mode	0.25	-	4	_
		SLOW 1, 2 mode	447.6	-	133.3	μS
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 16 MHz	_	31.25	-	113
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	_	15.26	-	
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz				μS

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
	tcy	NORMAL 1, 2 mode			4	
Machine Cycle Time		IDLE 1, 2 mode	0.5	- 1		
Machine Cycle Time		SLOW 1, 2 mode	447.6	-	133.3	μS
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)		62.5	_	ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	_			113
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)		15.26	-	
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz	1			μS

 $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

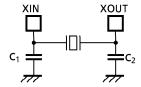
Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL 1, 2 mode				
Machina Cuala Tima	tcy	DLE 1, 2 mode 0.95		_	4	
Machine Cycle Time		SLOW 1, 2 mode	447.6	_	133.3	μS
		SLEEP 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 4.2 MHz	_	119.05	_	115
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input)	-	15.26	-	
Low Level Clock Pulse Width	twcL	fc = 32.768 kHz				μ\$

Timer Counter 1 input (ECIN) Characteristics  $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

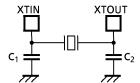
Parameter	Symbol	Condition	Min	Тур.	Max	Unit	
		Frequency measurement mode V <sub>DD</sub> = 3.5 to 5.5 V	Single edge count	-	-	- 16	
			Both edge count	ı	-		
TC1 input (ECIN input)		Frequency measurement mode V <sub>DD</sub> = 2.7 to 5.5 V	Single edge count	ı	-	- 8	MHz
Termput (Lenvinput)	t <sub>TC1</sub>		Both edge count	-	-		IVIIIZ
		Frequency measurement mode V <sub>DD</sub> = 1.8 to 5.5 V	Single edge count	ı	ı	4.2	
			Both edge count	-	-		

Recommended Oscillating Conditions - 1

 $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

  For up-to-date information, please refer to the following URL:

  http://www.murata.co.jp/search/index.html

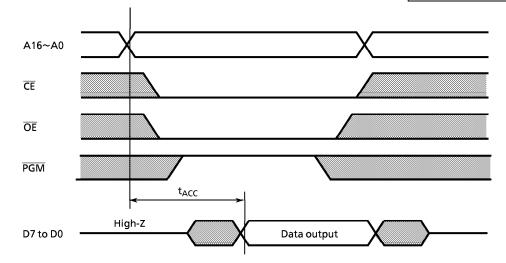
DC Characteristics, AC Characteristics (PROM Mode)

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

# (1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage (TTL)	V <sub>IH4</sub>		2.2	-	V <sub>CC</sub>	
Low leve input voltage (TTL)	V <sub>IL4</sub>		0	-	0.8	v
Power supply	V <sub>CC</sub>		4.75	5.0	5.25	
Power supply of program	$V_{PP}$					
Address access time	t <sub>ACC</sub>	V <sub>CC</sub> = 5.0 ± 0.25 V	-	1.5tcyc + 300	-	ns

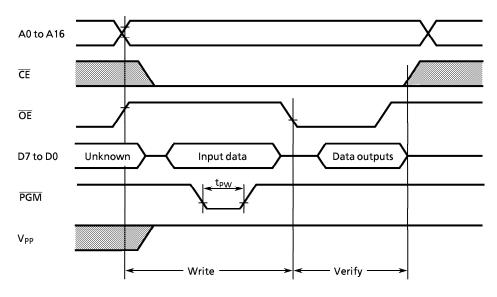
Note: tcyc = 500 ns at 8 MHz



# (2) Program operation (High-speed) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage (TTL)	V <sub>IH4</sub>		2.2	_	V <sub>CC</sub>	
Low leve input voltage (TTL)	V <sub>IL4</sub>		0	_	0.8	v
Power supply	V <sub>CC</sub>		6.0	6.25	6.5	
Power supply of program	V <sub>PP</sub>		12.5	12.75	13.0	
Pulse width of initializing program	t <sub>PW</sub>	V <sub>CC</sub> = 6.0 V	0.095	0.1	0.105	ms

## High-speed program writing



- Note 1: The power supply of  $V_{PP}$  (12.75 V) must be set power-on at the same time or the later time for a power supply of  $V_{CC}$  and must be clear power-on at the same time or early time for a power supply of  $V_{CC}$ .
- Note2: The pulling up/down device on the condition of  $V_{PP} = 12.75 \text{ V } \pm 0.25 \text{ V}$  causes a damage for the device. Do not pull up/down at programming.
- Note3: Use the recommended adapter and mode (See 1.2.2 (1) and 1.2.2 (3) i).

  Using other than the above condition may cause the trouble of the writting.