SIEMENS

V23809-E1-E30

1300 nm ESCON® Parallel Transceiver

FEATURES

- **Complies with ESCON and SBCON standards**
- **Fully compatible with Siemens former parallel transceiver V23806-A6-X1**
- **Includes clock recovery module, parallel-serial/ serial-parallel and ESCON/SBCON receptacle**
- **SMT component for easy mounting on surface mount PC boards**
- **Mates keyed ESCON/SBCON connector**
- **Data rates for ESCON/SBCON applications**
- **Data rates for individual applications from 100 to 300 MBaud**
- **Transmission distance of 3 km and more**
- **All inputs and outputs TTL compatible**
- **System optimized for 62.5 and 50 µm graded index fiber**
- **0.7" spacing between optical interface of transmitter and receiver**
- **Low profile for high slot density**

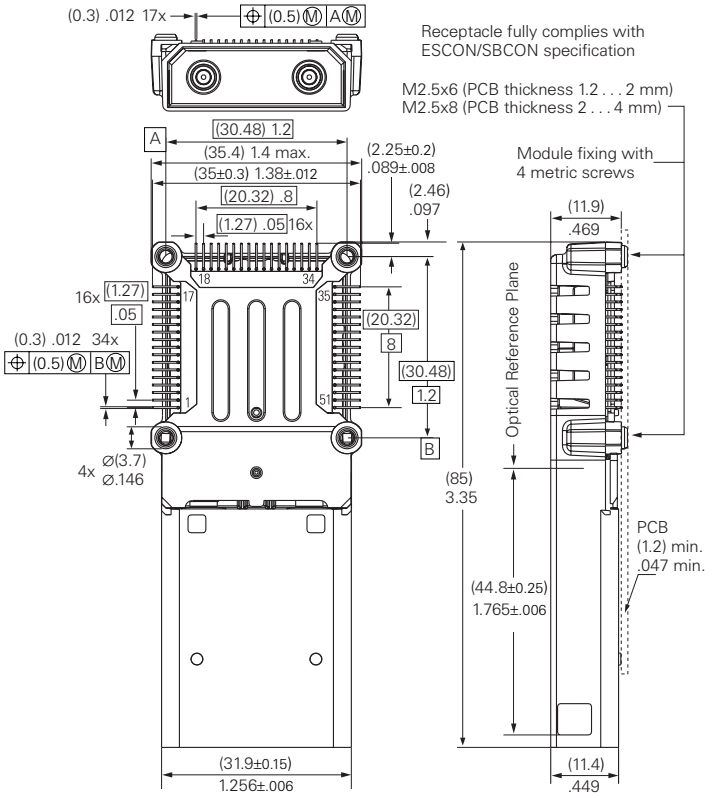
APPLICATIONS

- **ESCON architecture**
- **High speed computer links**
- **Local area networks**
- **High definition/digital television**
- **Switching systems**
- **Control systems**

Regulatory Compliance

Feature	Standard	Comments
Electromagnetic Interference (EMI)	FCC Class B EN 55022 Class B CISPR 22	Noise frequency range: 30 MHz to 1 GHz
Immunity: Electrostatic Discharge	EN 61000-4-2 IEC 1000-4-2	Discharges of ±15 kV with an air discharge probe on the receptacle cause no damage.
Immunity: Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 1000-4-3	With a field strength of 10 V/m rms, noise frequency ranges from 10 MHz to 1 GHz
Eye Safety	IEC 825-1	Class 1

Dimensions in inches (mm)



Absolute Maximum Ratings

Exceeding any one of these values may destroy the device immediately.

Supply Voltage (V_{CC}–V_{EE}) ..... –0.5 V to7 V
Maximum Input Voltage (V_{IN}) ..... V_{EE} to V_{CC}
Operating Ambient Temperature (T_{AMB}) ..... 0°C to 85°C
Humidity/Temperature Test Condition (R_H) ..... 85%/85°C
Life Test Condition (T_{AMB}/LIfe) ..... 115°C/1000h
Soldering Conditions Temp/Time (T_{SOLD}) ..... 260°C/10s
ESD Resistance (all pins to V_{EE}, human body) ..... 1.5 kV
Output Current (I_O) ..... 50 mA

ESCON® is a registered trademark of IBM.

DESCRIPTION

The Siemens ESCON/SBCON optical device, along with the ESCON/SBCON optical duplex connector, is best suited for high speed fiber optic duplex transmission systems operating at a wavelength of 1300 nm. The system is fully compatible with the IBM ESCON standard and the ANSI SBCON standard.

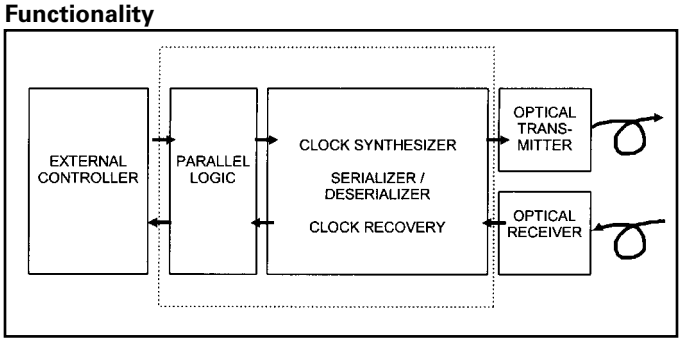
The ESCON parallel transceiver includes a transmitter, a receiver, a clock recovery function and serial/parallel interfaces. It is designed for data rates of up to 300 MBaud. A non-dissipative plastic receptacle matches the ESCON duplex connector.

The inputs/outputs are TTL compatible and the unit operates from a single power supply of 4.5 V to 5.5 V.

The optical interfaces of the transmitter and receiver have standard 0.7" spacing. Receptacle and connector have been keyed to prevent reverse insertion of the connector into the receptacle. After proper insertion, the connector is securely held by a snap-in lock mechanism.

The transmitter converts parallel electrical TTL input signals into an optical serial signal at data rates of between 100 and 300 MBaud. The receiver performs clock recovery on the incoming data stream and converts data into parallel output.

Functionality



TECHNICAL DATA

The electro-optical characteristics described in the following tables are valid only for use under the recommended operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Temperature	T_{AMB}	0	70	°C
Power Supply Voltage	V_{CC}–V_{EE}	4.75	5.25	V
Supply Current	I_{CC}		400	mA
Data Input High Voltage	V_{IH}	2	V_{CC}	V
Data Input Low Voltage	V_{IL}	V_{EE}	0.8	
Input Data Rise/Fall, 10%–90%	t_R, t_F	0.4	1.3	ns
Output Current High	I_O		–0.4	mA
Output Current Low	I_{CC2}		4	

Transmitter Electro-Optical Characteristics

Transmitter	Symbol	Min.	Typ.	Max.	Units
Data Rate	DR	100		300	MBaud
Supply Current[1]	I_{CC}			300	mA
Launched Power (Ave.) BOL into 62.5 µm Fiber[2, 3, 4]	P_O	–20	–16.5	–14	dBm
Launched Power (Ave.) EOL into 62.5 µm Fiber[2, 3. 4, 5]		–21.5			
Center Wavelength[6]	λ_C	1280		1355	nm
Spectral Width (FWHM)[7]	$\Delta\lambda$			175	
Temperature Coefficient, Optical Output Power	TCp			0.03	dB/°C
Output Rise/Fall Time, 20%–80%[6]	t_R, t_F		1	1.65	ns
Deterministic Jitter[8]	J_D		0.6	0.8	
Random Jitter[9]	J_R			0.06	
Extinction Ratio (Dynamic)[10]	ER		–16	–13	dB

Notes

1. Transmitter operating at 200 MBaud and 50% duty cycle.
2. Measured at the end of 1 meter fiber. Cladding modes removed at a data rate of between 50 and 200 MBaud, 50% duty cycle.
3. P_O [dBm]=10 log (P_O/1 mW).
4. P_O (BOL) >–20dBm and P_O (EOL) >–21.5 dBm at T_{CASE}=60°C.
5. Over 10^5 hours lifetime at T_{AMB}=35°C.
6. Measured at T_{CASE}=60°C.
7. Full width, half magnitude of peak wavelength. Special relationship between λc, Δλ, t_R/t_F according to FC-PH Rev 4.3 Paragraph 6.3.2. and Fig.26. Spectral width must be considered.
8. Measured at 200 MBaud with Jitter Test Pattern (see page 4). In the Test Pattern are five positive and five negative transitions. Measure the time of the 50% crossing of all 10 transitions. The time of each crossing is then compared to the mean expected time of the crossing. Deterministic jitter is the range of the timing variations.
9. RMS value measured with 1010 pattern. Peak-to-peak value is determined as RMS multiplied by 14 for BER 1E-12.
10. Extinction ratio is the logarithmic measure of the optical power in the OFF state (P_{OFF}) to twice the average power (P_O).
    ER=10 log [(2xP_O)/P_{OFF}] (optical power measured in mW), or
    E=|P_O+3 dB| –P_{OFF} (optical power measured in dBm).

Receiver Electro-Optical Characteristics

Receiver	Symbol	Min.	Typ.	Max.	Units
Data Rate	Dr	100		300	MBaud
Supply Current (1)	I_{CC}			100	mA
Sensitivity (Average Power) BOL(2, 3, 4)	P_{IN}	–32.5	–35.5	–14	dBm
Sensitivity (Average Power) EOL(2, 3, 4, 5)		–32	–35	–14	
Saturation (Average Power)	P_{SAT}	–14			
Signal Detect Assert Level(6)	P_{SDA}	–44.5		–36	
Signal Detect Deassert Level(6)	P_{SDD}	–45		–37.5	
Signal Detect Hysteresis	P_{SDA}–P_{SDD}	0.5	1.5	3	dB
Signal Detect Reaction Time	SDreac	3		500	µs
Max. Deterministic Jitter Optical Input(7, 9)	J_D			0.19	% of Unit Intervals
Max. Random Jitter RMS Optical Input(8, 9)	J_R			0.09	

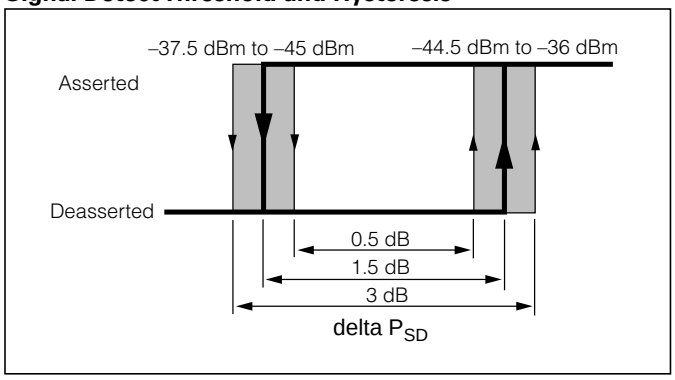
Notes

1. For V_{CC}–V_{EE} (min., max.). 50% duty cycle.
2. Measured at the end of 1 meter fiber and at a duty cycle of 50%. Cladding modes are removed.
3. P_O [dBm]=10 log (P_O/1mW).
4. Measured at BER=1E-12, 200 MBaud transmission rate and 50% duty cycle 2^7-1 PRBS pattern. For 300 MBaud the sensitivity will be decreased by 4 dB. Center wavelength between 1200 nm and 1500 nm. Fiber type 62.5/125 µm/0.29 NA or 50/125 µm/0.2 NA. Input optical rise and fall times 1.2 ns and 1.5 ns (20%–80%) respectively.
5. Over 10^5 hours lifetime at T_{AMB}=35°C.
6. Indicates the presence or absence of optical power at the receiver input. Signal detect at logic High when asserted. All powers are average power levels. Pattern 2^7-1 at 200 MBaud.
7. Measured at 200 MBaud with Jitter Test Pattern (see page 4). In the test pattern are five positive and five negative transitions. Measure the time of the 50% crossing of all 10 transitions. The time of each crossing is then compared to the mean expected time of the crossing. Deterministic jitter is the range of the timing variations.
8. To convert from specified RMS value to peak-to-peak value (at BER 1E-12), multiply value by 14.
9. Jitter at optical input. Jitter magnitudes above specified level may increase the bit error rate.

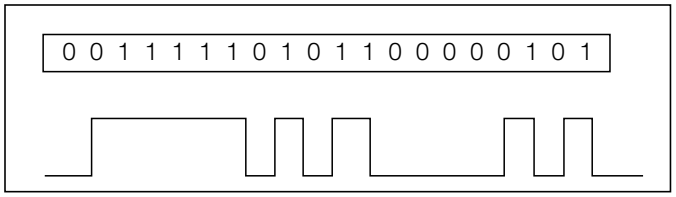
Pin Description 10 Bit Interface

Pin#	Pin Name	Level/Logic	Description
1, 6, 9, 26, 43, 45, 48, 51	V_{EE}	Power Supply	Ground attached to the case
2	V_{CC} PRE		Preamplifier positive power supply
3	SIGDET	TTL out	Signal detected
4	LOCKREF	TTL in	Control input for RX PLL
5	SYNCEN		Control of byte alignment operation
7,8	V_{CC}FAST	Power Supply	Bipolar IC positive power supply
10 to 19	D_{OUT} a to j	TTL out	Data output parallel 10 channels
20	RBCLK	TTL out	Read byte clock
21	PAROUT		Parity bit out
22	BSYNC		Byte synchronization operation
23	PARERR	TTL out	Parity bit error
24, 25	V_{CC}SLOW	Power Supply	Logic positive power supply
27	Loopsel a	TTL in	Test loop select
28	Loopsel b		
29	RESREC		Receiver reset
30	RESFF		Reset all flip-flops
31	TBCLK		Transmit byte clock
32	PARIN		Parity bit in
33 to 42	D_{IN} j to a		Data input parallel 10 channels
44	TESTCLK		Test clock. In test mode this clock is the bit clock
46	TESTMOD		If this signal is low TESTCLK is used
47	TXOFF		Transceiver off when logical high
49, 50	V_{CC} DRI	Power Supply	LED driver positive power supply

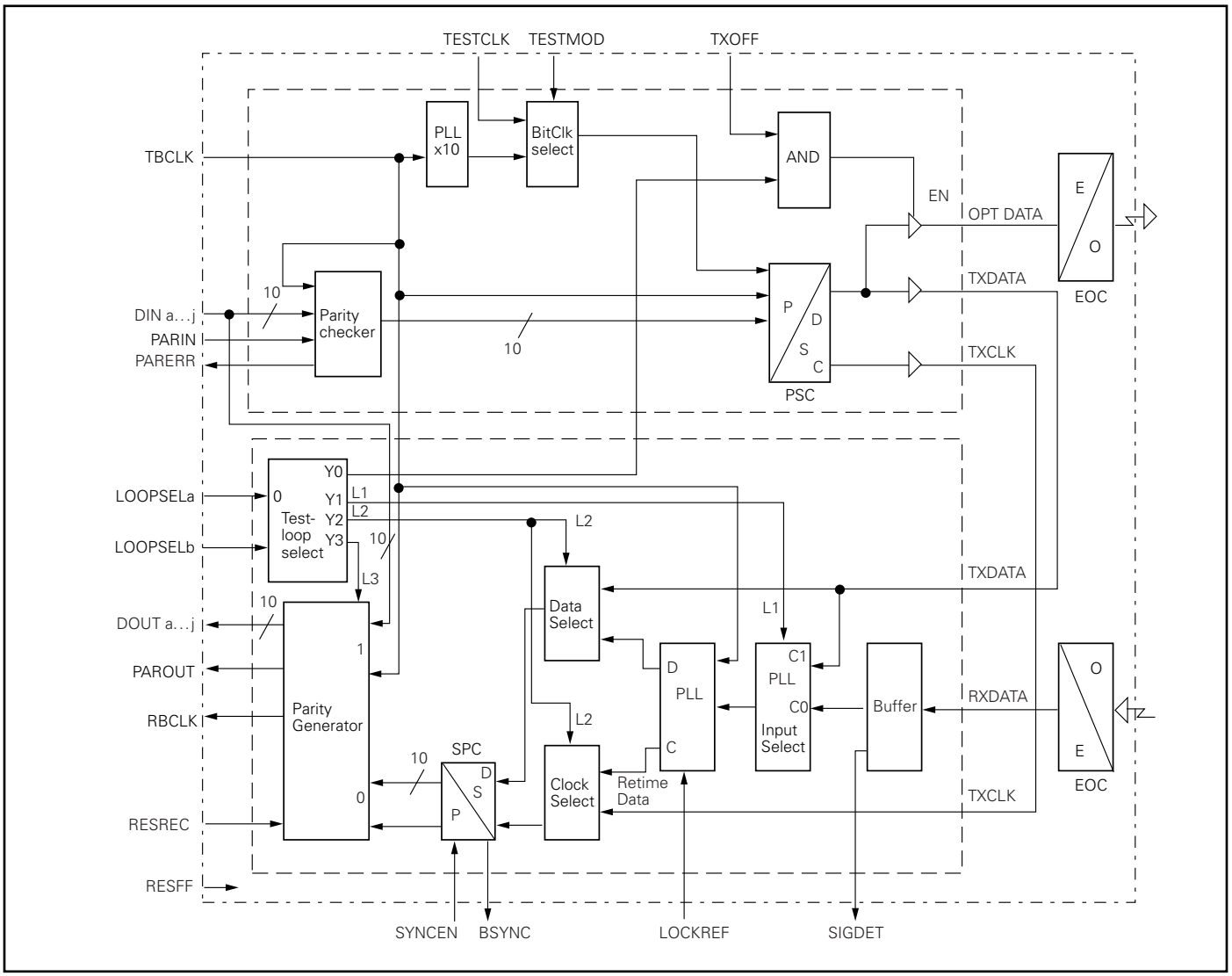
Signal Detect Threshold and Hysteresis



Jitter Test Pattern



Block Diagram of ESCON Parallel Transceiver



APPLICATION NOTE

Power Supply Filtering

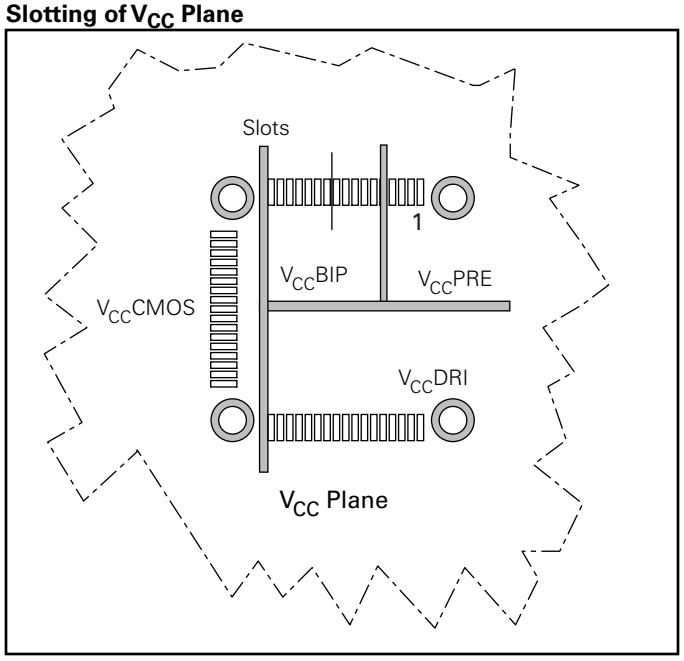
In most applications using the ESCON 200 MBd transceiver additional high speed circuits, such as a switching power supply, clock oscillator, or high speed multiplexer, are present on the application board. These often create power supply noise at a high spectral bandwidth, which is caused by very fast transitions in today's chip technology.

The Siemens ESCON transceiver provides superior EMI performance immunity against conductive noise. Some basic recommendations are given here to ensure proper functionality in the field.

The use of a multilayer board with ground and V_{CC} plane is strongly recommended. The Vcc plane should be slotted to avoid crosstalk between different circuitry inside the module. The metallized package is internally connected to the V_{EE} pins of the module. Nevertheless, the package must be connected externally to ground for best shielding characteristics. Ground contact should be made with the ground rings shown in the diagram below. Because of high switching currents at V_{CC}DRI, the use of an external 6.8 µF to 22 µF capacitor is recommended at V_{CC}DRI.

The observance of normal design rules for high speed digital systems is sufficient to ensure safe operation.

Slotting of V_{CC} Plane

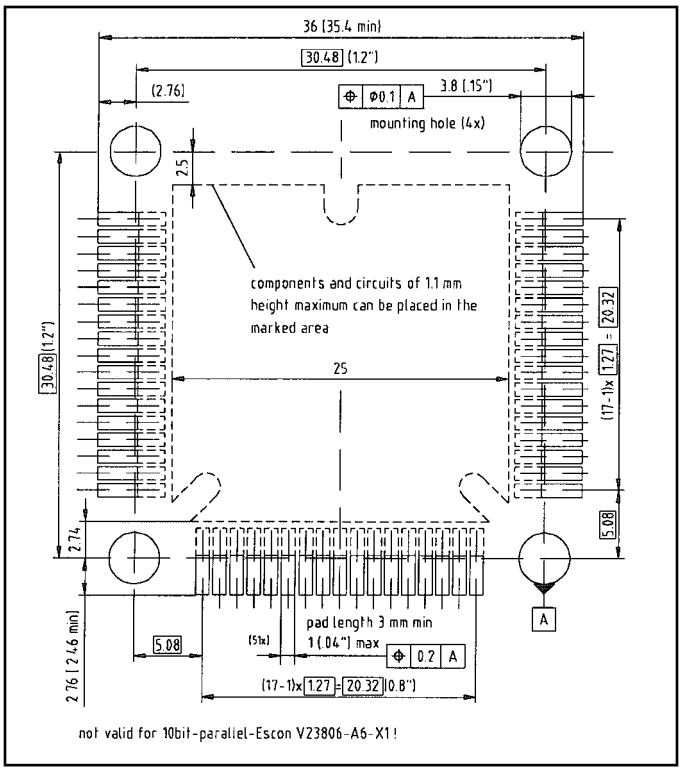


Note

Slots are non-copper areas inside the V_{CC} plane to avoid cross-current flow.

Recommended Footprint

Avoid placing any component or non-isolated structure, like tracks or vias, under the transceiver.



Power On Sequence