

Errata: CS4299 Rev. D

(Reference CS4299 Data Sheet revision DS319PP3 dated FEB '99)

1. The CS4299 requires a minimum SYNC pulse width of 1.13 μ s in the absence of BIT_CLK for a warm reset to occur. AC '97 version 2.1 requires SYNC to be asserted for a minimum of only 1.0 μ s.

Note: This requirement refers to the behavior of SYNC during warm reset only. During normal operation, SYNC is asserted for the entire period of slot 0 (the tag phase) which is 16 cycles of BIT_CLK.

2. SDATA_IN does not meet the AC '97 specification of driving a 47.5 pF capacitive load within the rise time constraints of $2 \text{ ns} \leq \text{Trise} \leq 6 \text{ ns}$. However, even at maximum capacitive loading the codec provides sufficient SDATA_IN data setup margin to prevent any functional issues.

Workaround Solution- Minimize SDATA_IN trace length during board layout and keep the total capacitive loading to 22 pF or less.

If there are any questions concerning this information,
Please contact: 1-800-888-5016 ext.3438
