Data Sheet | July 2000 | File Number 4857

14A, 370V N-Channel, Logic Level, Voltage Clamping IGBTs

This N-Channel IGBT is a MOS gated, logic level device which is intended to be used as an ignition coil driver in automotive ignition circuits. Unique features include an active voltage clamp between the collector and the gate which provides Self Clamped Inductive Switching (SCIS) capability in ignition circuits. Internal diodes provide ESD protection for the logic level gate. Both a series resistor and a shunt resister are provided in the gate circuit.

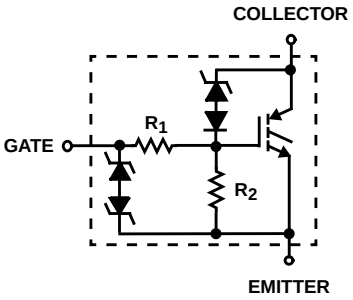
Formerly Developmental Type TA49169.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGT1S14N37G3VLS	TO-263AB	14N37GVL
HGTP14N37G3VL	TO-220AB	14N37GVL

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB in tape and reel, i.e. HGT1S14N37G3VLS9A

Symbol

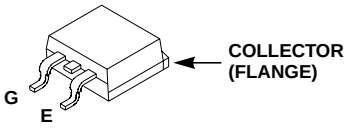


Features

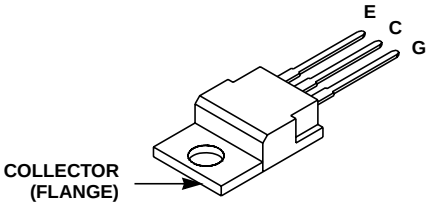
- Logic Level Gate Drive
- Internal Voltage Clamp
- ESD Gate Protection
- $T_J = 175^oC$
- Internal Series and Shunt Gate Resistors
- Low Conduction Loss
- Ignition Energy Capable

Packaging

JEDEC TO-263AB



JEDEC TO-220AB



INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGT1S14N37G3VLS, HGTP14N37G3VL	UNITS
Collector to Emitter Breakdown Voltage at 10mA	BV_{CER}	380	V
Emitter to Collector Breakdown Voltage at 10mA	BV_{ECS}	24	V
Collector Current Continuous at V_{GE} = 5V, $T_C = 25^oC$	I_{C25}	25	A
at V_{GE} = 5V, $T_C = 110^oC$	I_{C110}	18	A
Gate to Emitter Voltage (Note 1)	V_{GEM}	±10	V
Inductive Switching Current at L = 3mH, $T_C = 25^oC$	I_{SCIS}	15	A
at L = 3mH, $T_C = 150^oC$	I_{SCIS}	11.5	A
Collector to Emitter Avalanche Energy at L = 3 mH, $T_C = 25^oC$	E_{AS}	340	mJ
Power Dissipation Total at $T_C = 25^oC$	P_D	136	W
Power Dissipation Derating $T_C > 25^oC$		0.91	$W/^oC$
Storage Junction Temperature Range	T_{STG}	-55 to 175	^oC
Operating Junction Temperature Range	T_J	-55 to 175	^oC
Electrostatic Voltage HBM at 250pF, 1500Ω All Pin Configurations	ESD	5	kV
Electrostatic Voltage MM at 200pF, 0Ω All Pin Configurations	ESD	2	kV
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{PKG}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. May be exceeded if I_{GEM} is limited to 10mA.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CER}	I_C = 10mA, R_G = 1kΩ, V_{GE} = 0V, $T_J = -55^oC$ to 175^oC (Figure 16)		320	350	380	V
Gate to Emitter Plateau Voltage	V_{GEP}	I_C = 6.5A, V_{CE} = 12V		-	2.76	-	V
Gate Charge	$Q_{G(ON)}$	I_C = 6.5A, V_{CE} = 12V, V_{GE} = 5V (Figure 16)		-	27	-	nC
Collector to Emitter Clamp Breakdown Voltage	$BV_{CE(CL)}$	I_C = 15A, R_G = 1kΩ		320	350	380	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	I_C = 10mA		24	28	-	V
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = 300V, V_{GE} = 0V (Figure 13)	$T_J = 25^oC$	-	-	40	μA
			$T_J = 175^oC$	-	-	250	μA
		V_{CE} = 250V, V_{GE} = 0V (Figure 13)	$T_J = 25^oC$	-	-	10	μA
			$T_J = 175^oC$	-	-	75	μA
Emitter to Collector Leakage Current	I_{ECS}	V_{EC} = -24V, V_{GE} = 0V (Figure 13)	$T_J = 25^oC$	-	-	10	mA
			$T_J = 175^oC$	-	-	50	mA
Collector to Emitter On-State Voltage	$V_{CE(ON)}$	I_C = 6A, V_{GE} = 4.0V (Figures 3 through 9)	$T_J = -55^oC$	-	1.3	1.45	V
			$T_J = 25^oC$	-	1.25	1.6	V
		I_C = 10A, V_{GE} = 4.5V (Figures 3 through 9)	$T_J = 25^oC$	-	1.45	1.75	V
			$T_J = 175^oC$	-	1.5	1.9	V
		I_C = 14A, V_{GE} = 5V (Figures 3 through 9)	$T_J = 25^oC$	-	1.6	2	V
			$T_J = 175^oC$	-	1.7	2.3	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1mA, V_{CE} = V_{GE} (Figure 12)		1.3	1.8	2.2	V
Gate Series Resistance	R_1			-	70	150	Ω
Gate to Emitter Resistance	R_2			10	18	26	kΩ
Gate to Emitter Leakage Current	I_{GES}	V_{GE} = ±10V		±310	±500	±1000	μA

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Gate to Emitter Breakdown Voltage	BV_{GES}	$I_{GES} = \pm 2mA$		±12	±14	-	V
Current Turn-On Delay Time - Resistive Load	$t_{d(ON)I}$	$I_C = 6.5A$, $R_G = 1k\Omega$, $V_{GE} = 5V$, $R_L = 2.1\Omega$, $V_{DD} = 14V$, $T_J = 150^oC$ (Figure 14)		-	1	4	µs
Current Turn-On Rise Time - Resistive Load	t_{rI}	$I_C = 6.5A$, $R_G = 1k\Omega$ $V_{GE} = 5V$, $R_L = 2.1\Omega$ $V_{DD} = 14V$, $T_J = 150^oC$ (Figure 14)		-	3	7	µs
Current Turn-Off Time - Inductive Load	$t_{d(OFF)I} + t_{fI}$	$I_C = 6.5A$, $R_G = 1k\Omega$ $V_{GE} = 5V$, $L = 300\mu H$ $V_{DD} = 300V$, $T_J = 150^oC$ (Figure 14)		-	10	30	µs
Inductive Use Test	I_{SCIS}	$L = 3mH$, $V_G = 5V$, $R_G = 1k\Omega$ (Figures 1 and 2)	$T_C = 150^oC$	11.5	-	-	A
			$T_C = 25^oC$	15	-	-	A
Thermal Resistance	$R_{\theta JC}$	(Figure 18)		-	-	1.1	$^oC/W$

Typical Performance Curves Unless Otherwise Specified

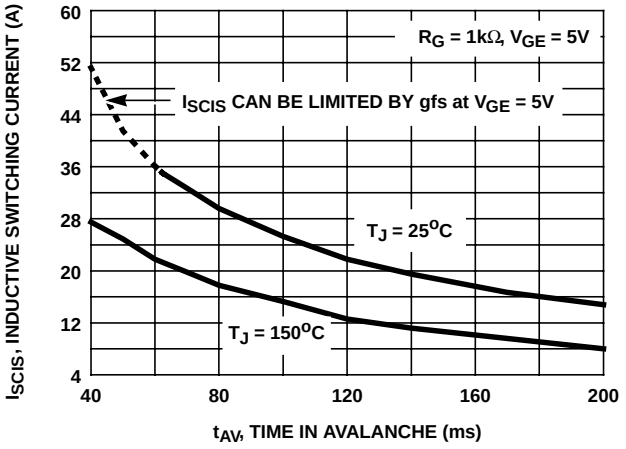


FIGURE 1. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs TIME IN AVALANCHE

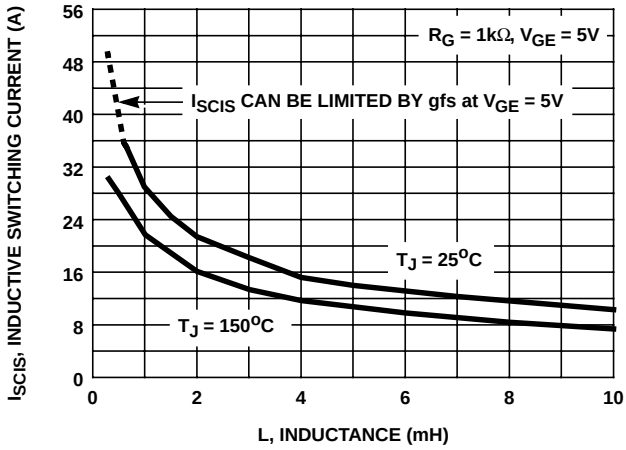


FIGURE 2. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs INDUCTANCE

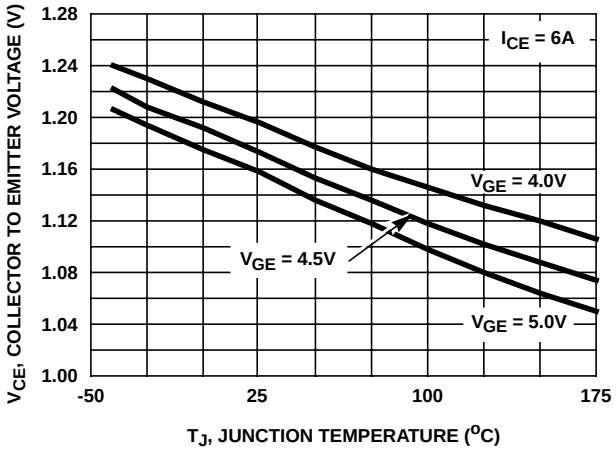


FIGURE 3. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERARURE

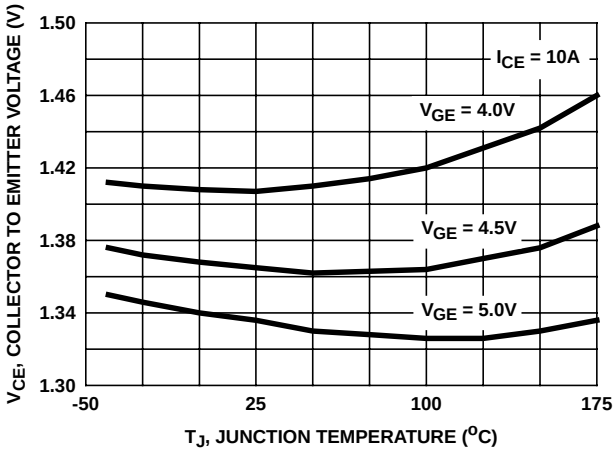


FIGURE 4. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

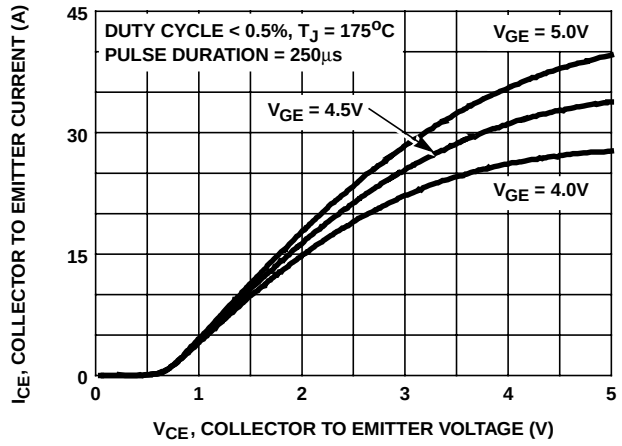


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

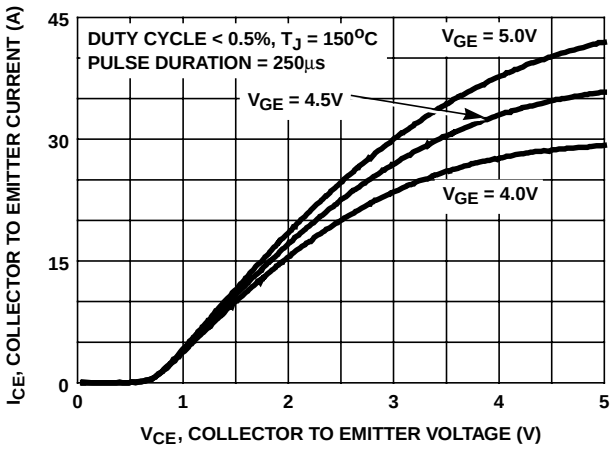


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

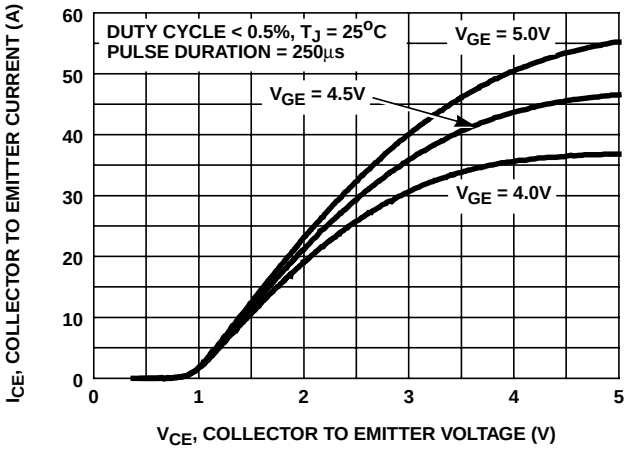


FIGURE 7. COLLECTOR TO EMITTER ON-STATE VOLTAGE

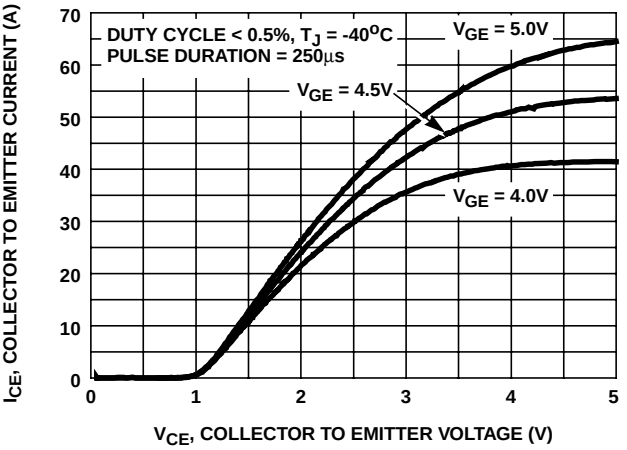


FIGURE 8. COLLECTOR TO EMITTER ON-STATE VOLTAGE

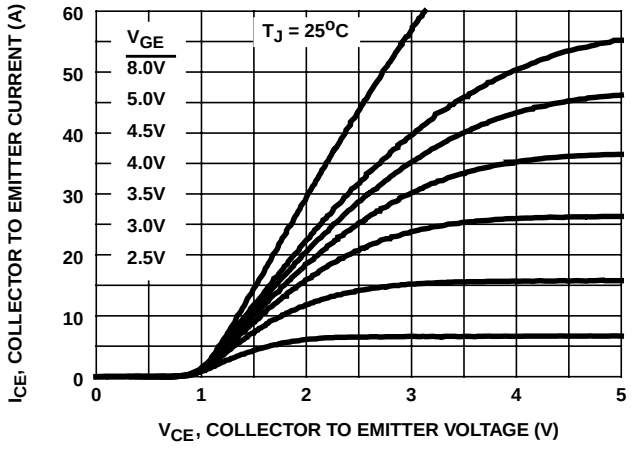


FIGURE 9. COLLECTOR TO EMITTER ON-STATE VOLTAGE

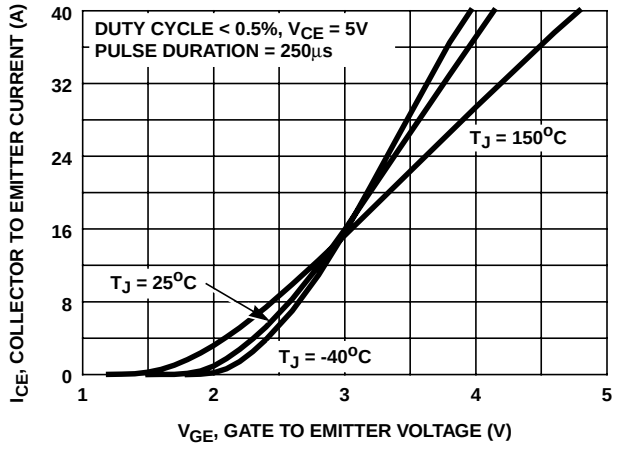


FIGURE 10. TRANSFER CHARACTERISTIC

Typical Performance Curves Unless Otherwise Specified (Continued)

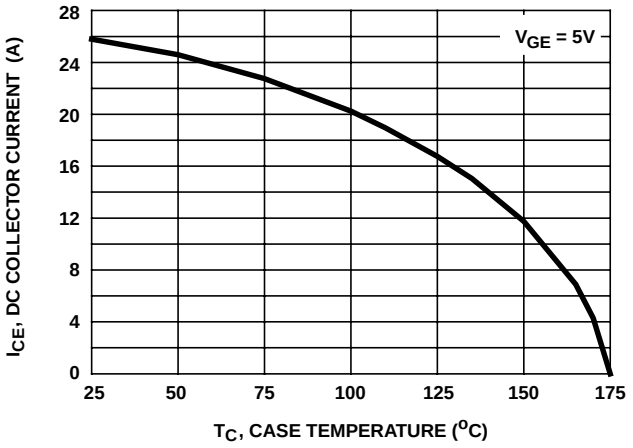


FIGURE 11. DC COLLECTOR CURRENT vs CASE TEMPERATURE

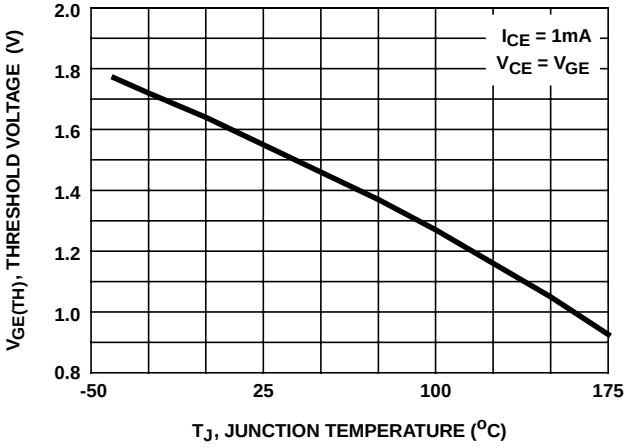


FIGURE 12. THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

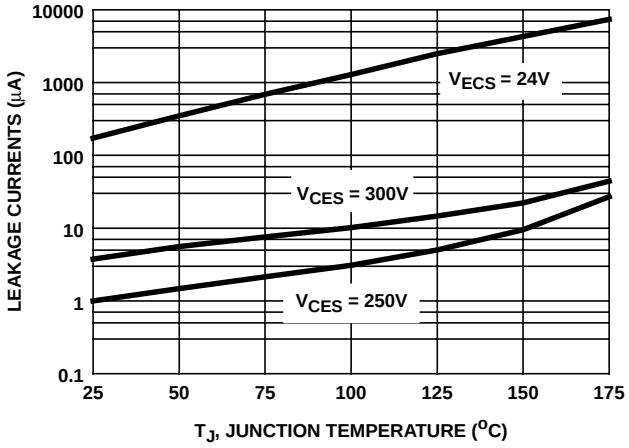


FIGURE 13. LEAKAGE CURRENT vs JUNCTION TEMPERATURE

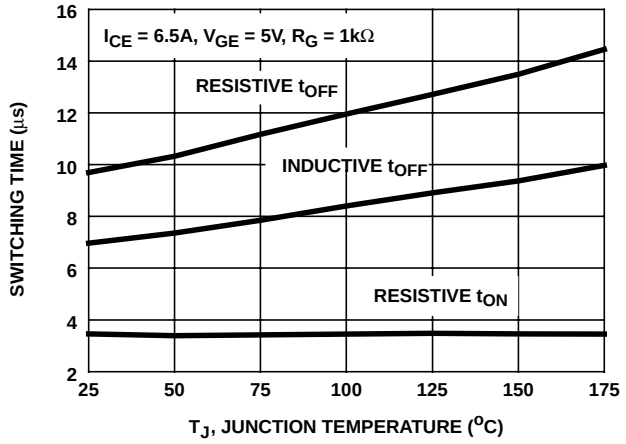


FIGURE 14. SWITCHING TIME vs JUNCTION TEMPERATURE

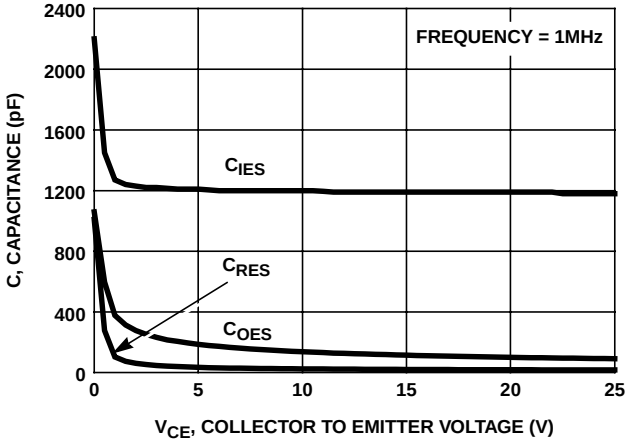


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

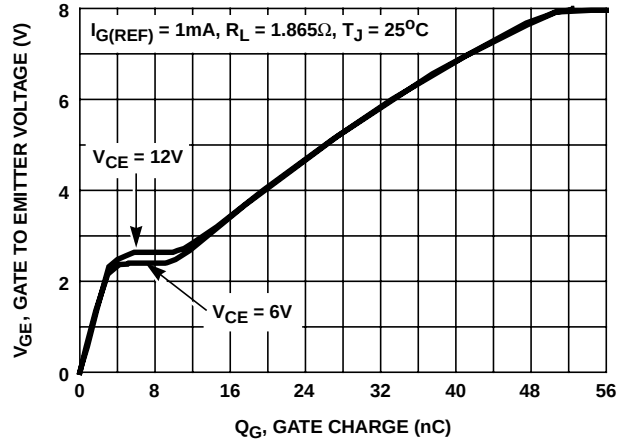


FIGURE 16. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified (Continued)

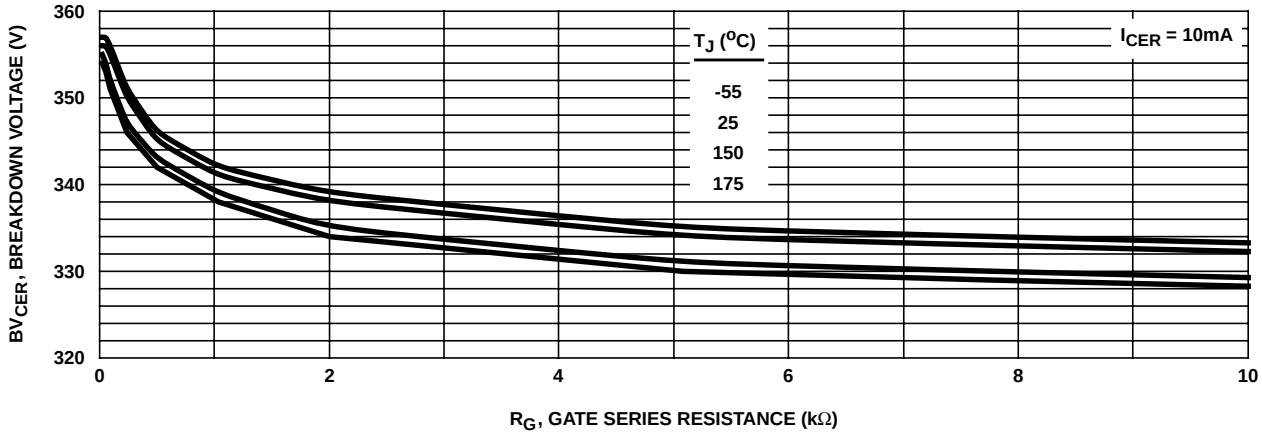


FIGURE 17. BREAKDOWN VOLTAGE vs SERIES GATE RESISTANCE

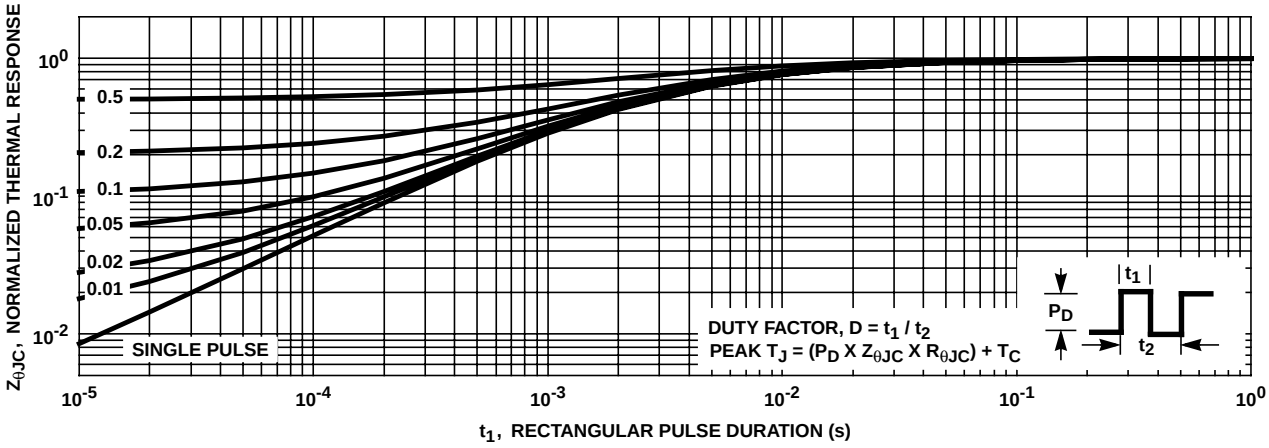


FIGURE 18. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuits

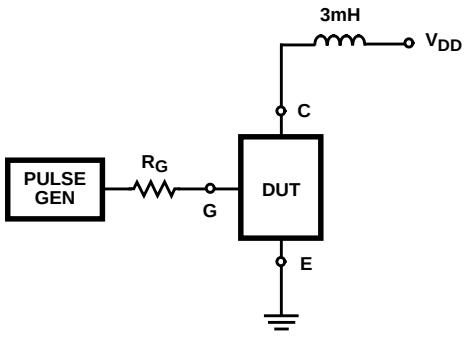


FIGURE 19. INDUCTIVE SWITCHING TEST CIRCUIT

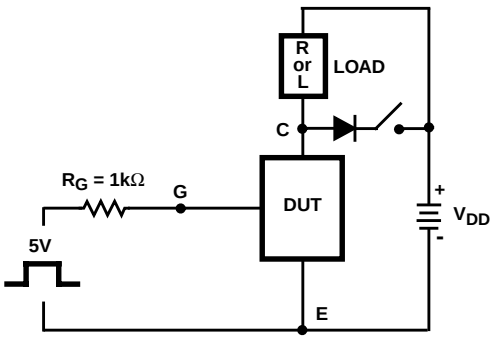
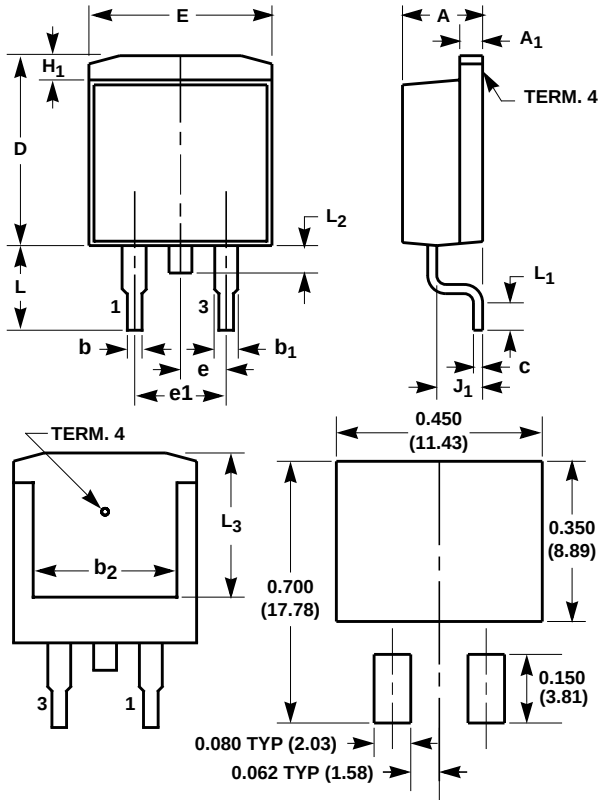


FIGURE 20. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE

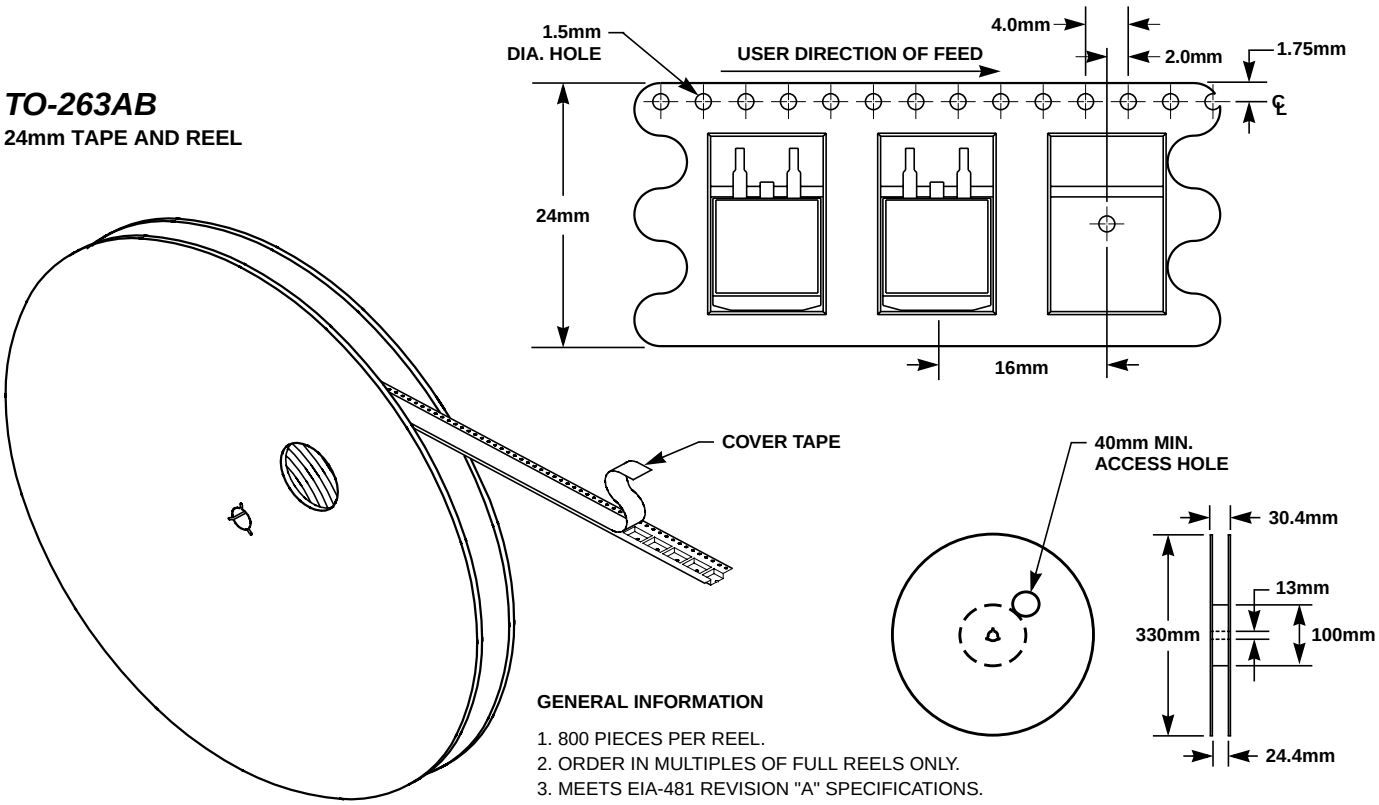


MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:
1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 10 dated 5-99.

TO-263AB
24mm TAPE AND REEL

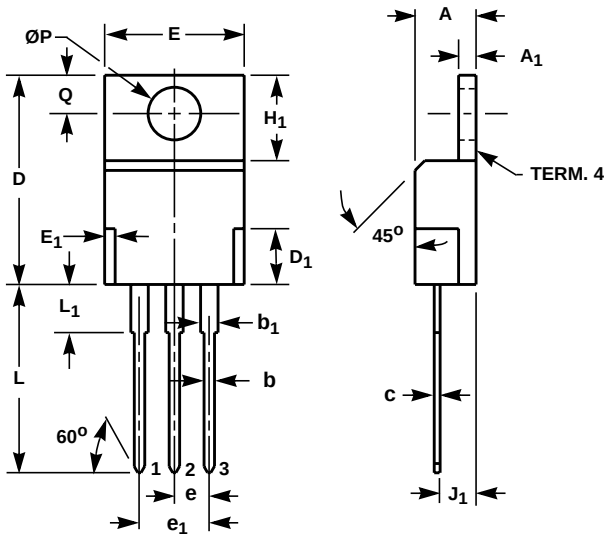


GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



LEAD	TERMINAL
Lead No. 1	Gate
Lead No. 2	Collector
Lead No. 3	Emitter
Term. No. 4	Collector
Mounting Flange	

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

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