PRELIMINARY

Integrated Circuit Systems, Inc.

ICS854057

4:1 OR 2:1 LVDS CLOCK MULTIPLEXER WITH INTERNAL INPUT TERMINATION

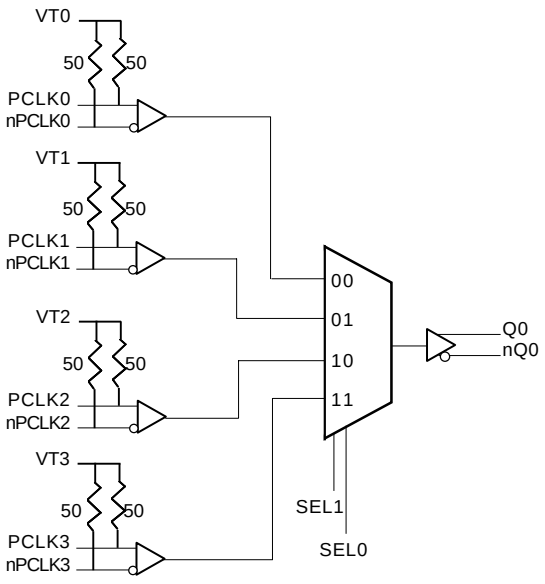
GENERAL DESCRIPTION

The ICS854057 is a 4:1 or 2:1 LVDS Clock Multiplexer which can operate up to 2GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The PCLK, nPCLK pairs can accept most standard differential input levels. Internal termination is provided on each differential input pair. The ICS854057 operates using a 2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. The select pins have internal pulldown resistors. Leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

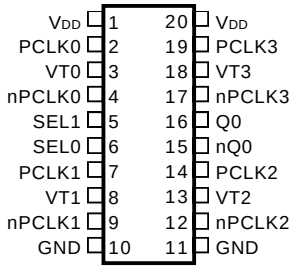
FEATURES

- High speed differential multiplexer. The device can be configured as either a 4:1 or 2:1 multiplexer
- Single LVDS output
- 4 selectable PCLK, nPCLK inputs with internal termination
- PCLK, nPCLK pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2GHz
- Part-to-part skew: TBD
- Propagation delay: 725ps (typical)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS854057
20-Lead TSSOP
4.40mm x 6.50mm x 0.90mm body package
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 20	V_{DD}	Power		Positive supply pins.
2	PCLK0	Input		Non-inverting LVPECL differential clock input.
3	VT0	Input		Termination input. For LVDS input, leave floating. 50Ω termination to VT0.
4	nPCLK0	Input		Inverting LVPECL differential clock input. 50Ω termination to VT0.
5	SEL1	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
6	SEL0	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
7	PCLK1	Input		Non-inverting LVPECL differential clock input.
8	VT1	Input		Termination input. For LVDS input, leave floating. 50Ω termination to VT1.
9	nPCLK1	Input		Inverting LVPECL differential clock input. 50Ω termination to VT1.
10, 11	GND	Power		Power supply ground.
12	nPCLK2	Input		Inverting LVPECL differential clock input. 50Ω termination to VT2.
13	VT2	Input		Termination input. For LVDS input, leave floating. 50Ω termination to VT2.
14	PCLK2	Input		Non-inverting LVPECL differential clock input.
15, 16	nQ0, Q0	Output		Differential output pairs. LVDS interface levels.
17	nPCLK3	Input		Inverting LVPECL differential clock input. 50Ω termination to VT3.
18	VT3	Input		Termination input. For LVDS input, leave floating. 50Ω termination to VT3.
19	PCLK3	Input		Non-inverting LVPECL differential clock input.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				TBD	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			50		KΩ
R_T	Input Termination Resistor			50		Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs		Clock Out
SEL1	SEL0	PCLK
0	0	PCLK0, nPCLK0
0	1	PCLK1, nPCLK1
1	0	PCLK2, nPCLK2
1	1	PCLK3, nPCLK3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			55		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	SEL0, SEL1		-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA

TABLE 4C. DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, PCLK1, PCLK2, PCLK3	V_{DD} = V_{IN} = 2.625V				µA
		nPCLK0, nPCLK1, nPCLK2, nPCLK3	V_{DD} = V_{IN} = 2.625V				µA
I_{IL}	Input Low Current	PCLK0, PCLK1, PCLK2, PCLK3	V_{DD} = 2.625V, V_{IN} = 0V				µA
		nPCLK0, nPCLK1, nPCLK2, nPCLK3	V_{DD} = 2.625V, V_{IN} = 0V				µA
V_{PP}	Peak-to-Peak Voltage				0.15		V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.2			V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, T_A = -40°C TO 85°C

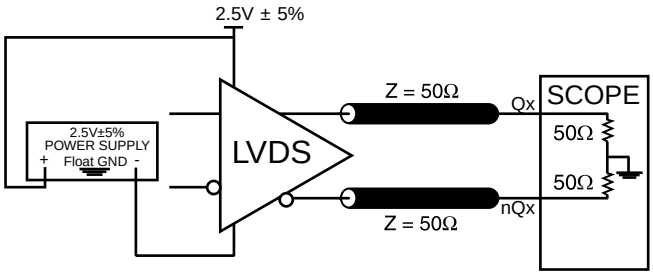
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change			4	35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, T_A = -40°C TO 85°C

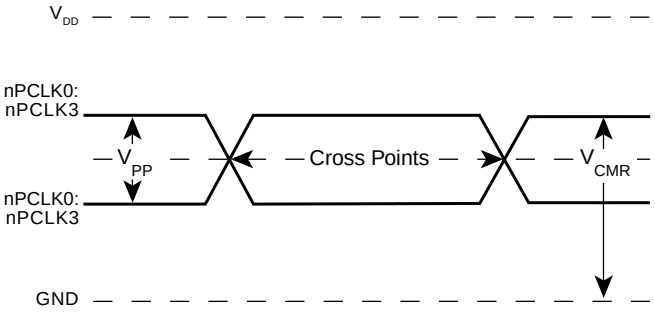
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			>2		GHz
t_{PD}	Propagation Delay; NOTE 1			725		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		160		ps
odc	Output Duty Cycle			50		%
$mux_{ISOLATION}$	Isolation					dB

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

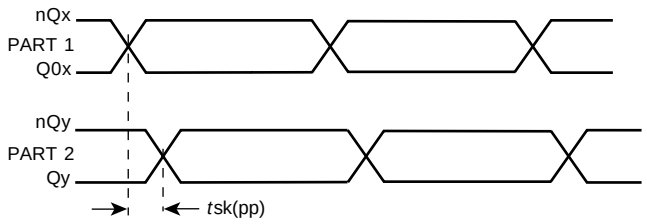
PARAMETER MEASUREMENT INFORMATION



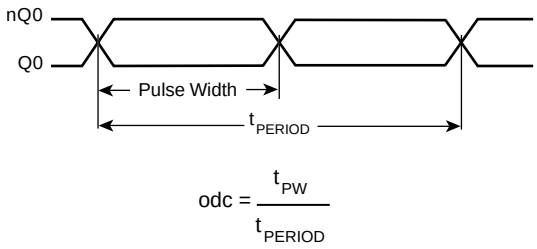
2.5V OUTPUT LOAD AC TEST CIRCUIT



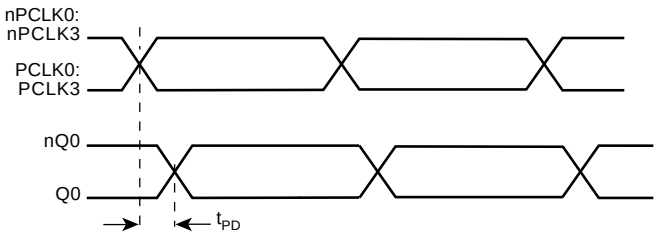
DIFFERENTIAL INPUT LEVEL



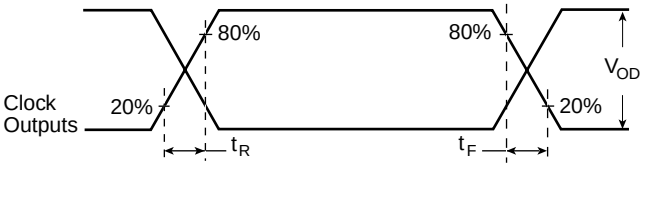
PART-TO-PART SKEW



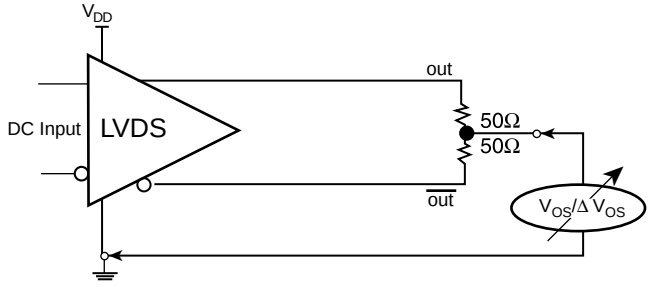
odc & t_{PERIOD}



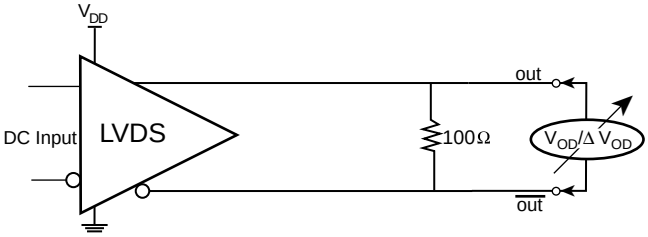
PROPAGATION DELAY



OUTPUT RISE/FALL TIME



V_{OS} SETUP



V_{OD} SETUP

APPLICATION INFORMATION

2.5V LVDS DRIVER TERMINATION

Figure 1 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

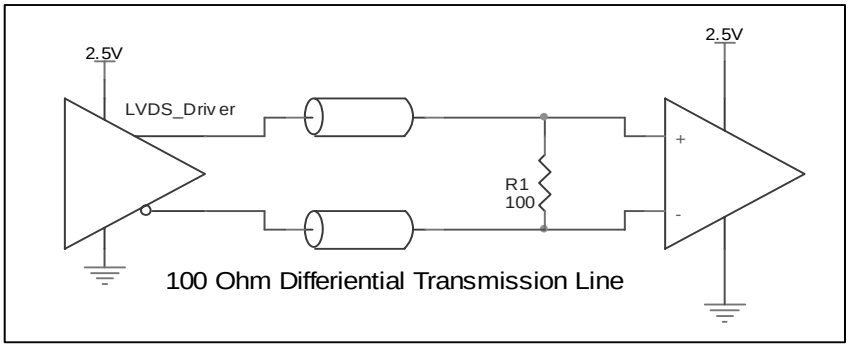


FIGURE 1. TYPICAL LVDS DRIVER TERMINATION

2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pull up and pull down connect to true and compliment of the unused input as shown in *Figure 2.*

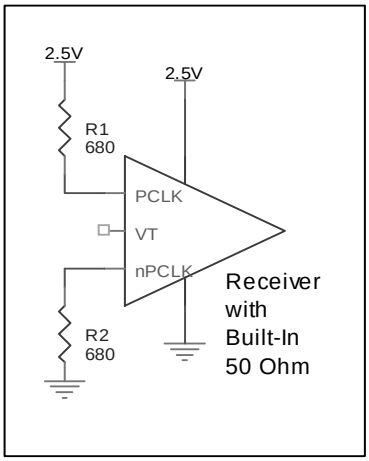


FIGURE 2. UNUSED INPUT HANDLING

PCLK/nPCLK INPUT WITH BUILT-IN 50Ω TERMINATION INTERFACE

The PCLK /nPCLK with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS PCLK/nPCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

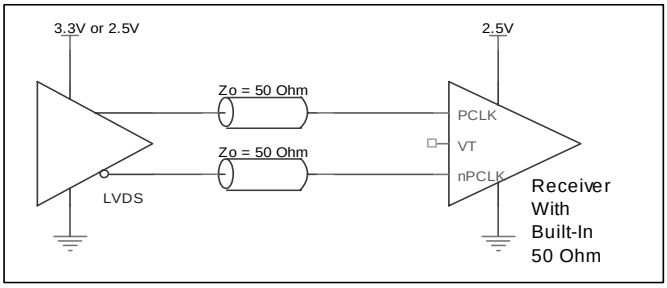


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

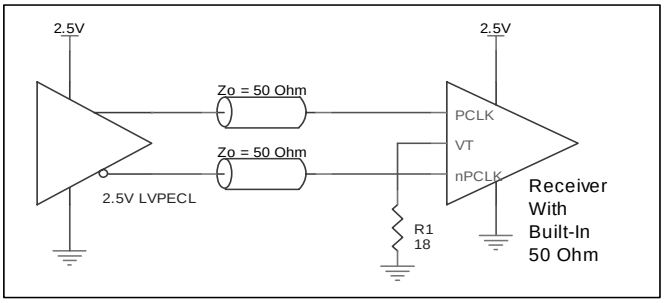


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

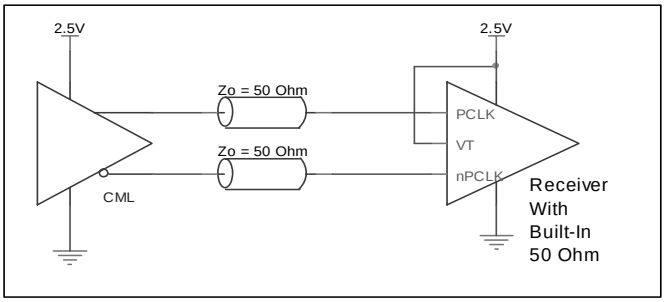


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER

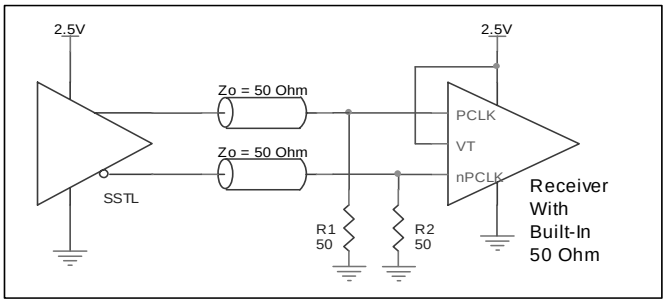


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

SCHEMATIC EXAMPLE

Figure 4 shows a schematic example of the ICS854057. In this example, the PCLK0/nPCLK0 and PCLK1/nPCLK1 inputs are used. The decoupling capacitors should be physically located near the power pin.

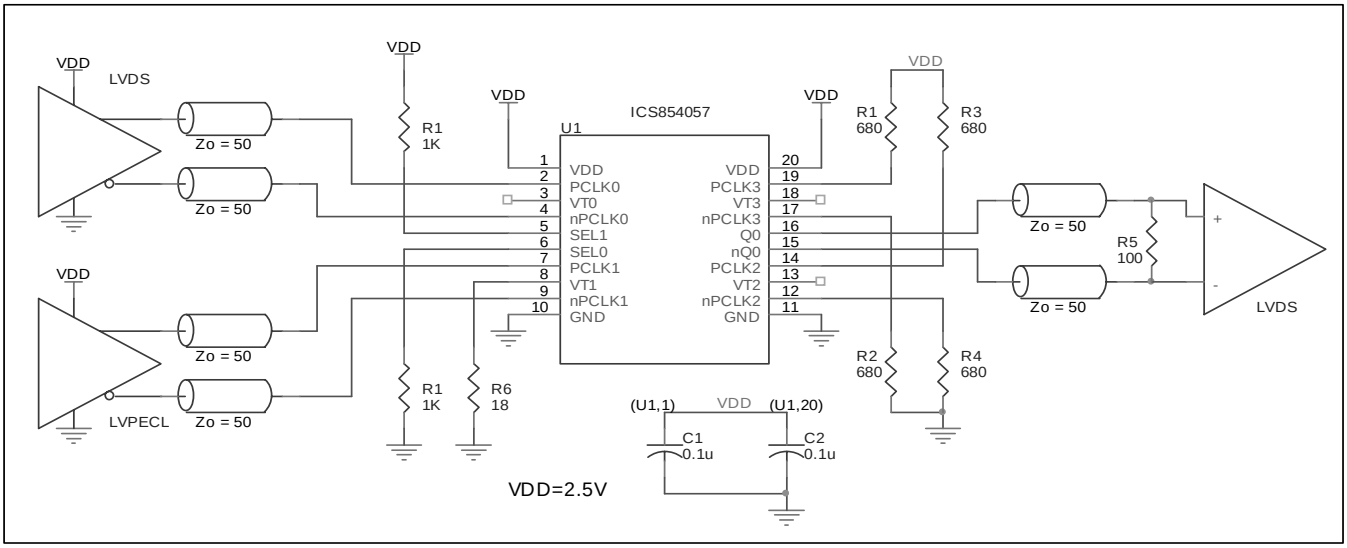


FIGURE 4. EXAMPLE ICS854057 LVDS SCHEMATIC

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854057-01 is: 346

PACKAGE OUTLINE - G SUFFIX

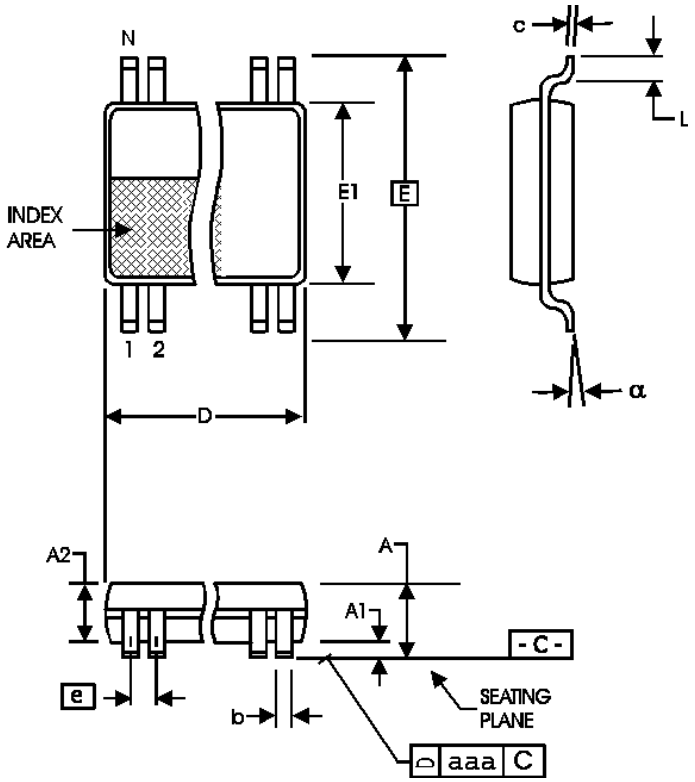


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS854057AG	ICS854057AG	20 lead TSSOP	74 per tube	-40°C to 85°C
ICS854057AGT	ICS854057AG	20 lead TSSOP on Tape and Reel	2500	-40°C to 85°C