Integrated Circuit Systems, Inc.

ICS8701-01

LOW SKEW, ÷1, ÷2
LVCMOS/ LVTTL CLOCK GENERATOR W/POLARITY CONTROL

GENERAL DESCRIPTION

The ICS8701-01 is a low skew, ÷1, ÷2 LVCMOS/ LVTTL Clock Generator and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

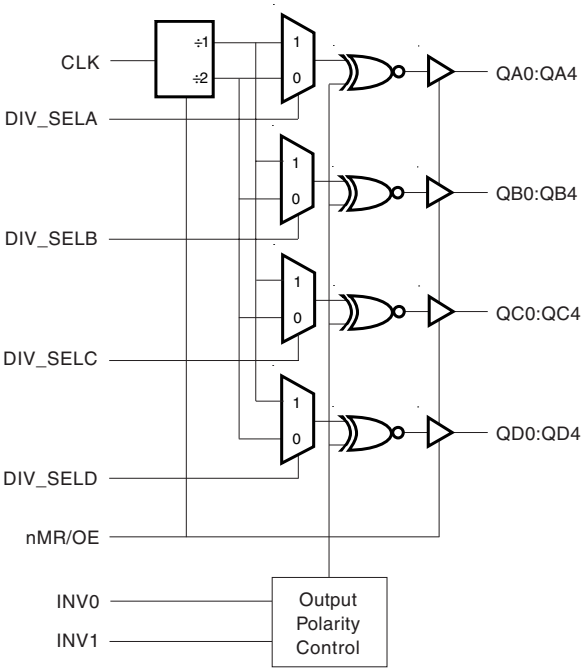
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset/output enable input, nMR/OE, resets the internal dividers and controls the active and high impedance states of all outputs. The output polarity inputs, INV0:1, control the polarity (inverting or non-inverting) of the outputs of each bank. Outputs QA0-QA4 are inverting for every combination of the INV0:1 input. The timing relationship between the inverting and non-inverting outputs at different frequencies is shown in the Timing Diagrams.

The ICS8701-01 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the ICS8701-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

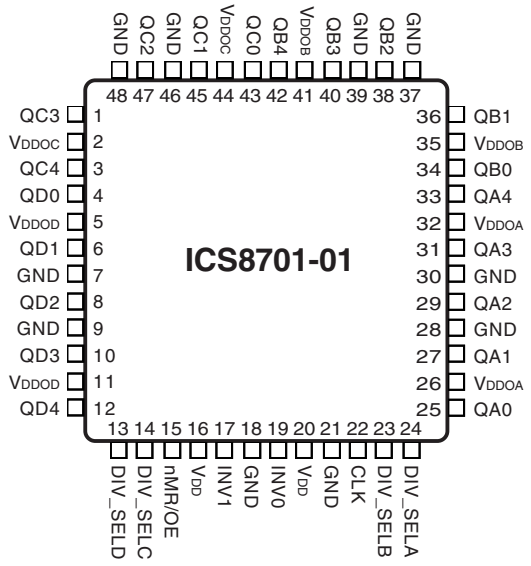
FEATURES

- 20 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- 1 LVCMOS/LVTTL clock input
- Maximum output frequency: 250MHz
- Selectable inverting and non-inverting outputs
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- Output skew: 300ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Bank skew: 250ps (maximum)
- Multiple frequency skew: 350ps (maximum)
- 3.3V or mixed 3.3V input, 2.5V output operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Pin LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 43, 45, 47	QC3, QC4, QC0, QC1, QC2	Output		Bank C outputs. LVCMOS interface levels. 7Ω typical output impedance.
2, 44	V_{DDOC}	Power		Output Bank C supply pins.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. LVCMOS interface levels. 7Ω typical output impedance.
5, 11	V_{DDOD}	Power		Output Bank D supply pins.
7, 9, 18, 21, 28, 30, 37, 39, 46, 48	GND	Power		Power supply ground.
13	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS interface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS interface levels.
15	nMR/OE	Input	Pullup	Master Reset and output enable. When HIGH, output drivers are enabled. When LOW, output drivers are in HiZ and dividers are reset. LVCMOS interface levels.
16, 20	V_{DD}	Power		Core supply pins.
17, 19	INV1, INV0	Input	Pullup	Determines polarity of outputs by banks. LVCMOS interface levels.
22	CLK	Input	Pullup	LVCMOS clock input.
23	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. LVCMOS interface levels.
24	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS interface levels.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. LVCMOS interface levels. 7Ω typical output impedance.
26, 32	V_{DDOA}	Power		Output Bank A supply pins.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. LVCMOS interface levels. 7Ω typical output impedance.
35, 41	V_{DDOB}	Power		Output Bank B supply pins.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, *V_{DDOx} = 3.465			15	pF
R_{OUT}	Output Impedance		5	7	12	Ω

*NOTE: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, and V_{DDOD}.

TABLE 3. FUNCTION TABLE

Inputs				Outputs				
nMR/OE	DIV_SELx	INV1	INV0	Bank A	Bank B	Bank C	Bank D	Qx Frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Inverting	Non-inverting	Non-inverting	Non-inverting	fIN/2
1	0	0	1	Inverting	Inverting	Non-inverting	Non-inverting	fIN/2
1	0	1	0	Inverting	Inverting	Inverting	Non-inverting	fIN/2
1	0	1	1	Inverting	Inverting	Inverting	Inverting	fIN/2
1	1	0	0	Inverting	Non-inverting	Non-inverting	Non-inverting	fIN
1	1	0	1	Inverting	Inverting	Non-inverting	Non-inverting	fIN
1	1	1	0	Inverting	Inverting	Inverting	Non-inverting	fIN
1	1	1	1	Inverting	Inverting	Inverting	Inverting	fIN

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 3.3V±5% OR 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current; NOTE 2				95	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, and V_{DDOD}.
NOTE 2: I_{DD} contributes 50mA; I_{DDOx} contributes 45mA.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 3.3V±5% OR 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, INV0, INV1, nMR/OE		2		V_{DD} + 0.3	V
		CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, INV0, INV1, nMR/OE		-0.3		0.8	V
		CLK		-0.3		1.3	V
I_{IH}	Input High Current		V_{DD} = V_{IN} = 3.465V, V_{DD} = V_{IN} = 2.625V			5	µA
I_{IL}	Input Low Current		V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		*V_{DDOx} = 3.465V	2.6			V
			*V_{DDOx} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDOx}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

*NOTE: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDOx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.0		3.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on the Falling Edge			250	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on the Falling Edge			300	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7				350	ps
*t*sk(pp)	Part to Part Skew; NOTE 5, 7				700	ps
t_R	Output Rise Time; NOTE 6	20% to 80%	150		700	ps
t_F	Output Fall Time; NOTE 6	20% to 80%	150		700	ps
t_{PW}	Output Pulse Width	f ≤ 200MHz	$t_{Period}/2 - 0.5$	$t_{Period}/2$	$t_{Period}/2 + 0.5$	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6				6	ns
t_{DIS}	Output Disable Time; NOTE 6				6	ns

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDOx}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOx}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDOx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
*t*sk(inv)	Inverting Skew; NOTE 1, 2	f = 66.7MHz			400	ps

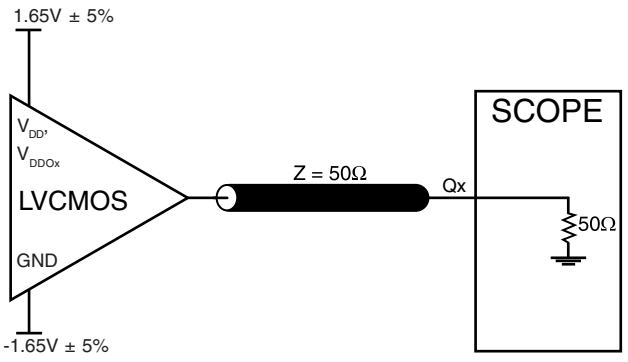
NOTE 1: Defined as skew across banks of outputs switching in opposite directions operating at the same frequency with the same supply voltages and equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOx} = 2.5V±5%, T_A = 0°C TO 70°C

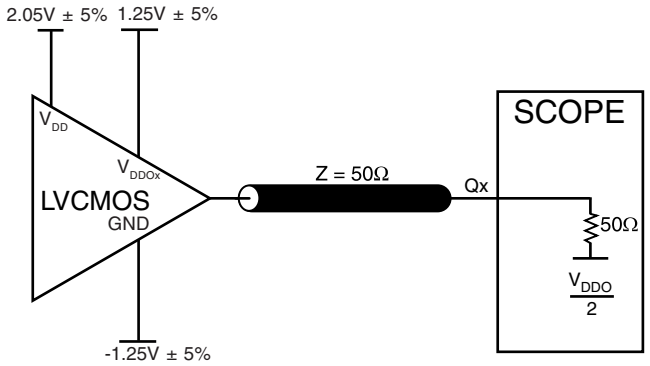
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.0		3.5	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on the Falling Edge			300	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on the Falling Edge			300	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7				350	ps
*t*sk(pp)	Part to Part Skew; NOTE 5, 7				700	ps
t_R	Output Rise Time; NOTE 6	20% to 80%	150		720	ps
t_F	Output Fall Time; NOTE 6	20% to 80%	150		720	ps
t_{PW}	Output Pulse Width	f ≤ 200MHz	$t_{Period}/2$ - 0.5	$t_{Period}/2$	$t_{Period}/2$ + 0.5	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6				6	ns
t_{DIS}	Output Disable Time; NOTE 6				6	ns

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDOx}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 5: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOx}/2$.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

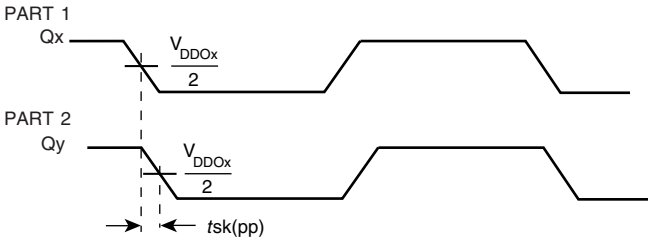
PARAMETER MEASUREMENT INFORMATION



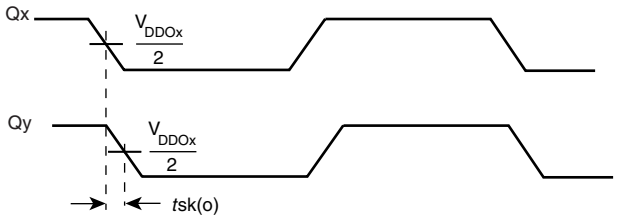
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



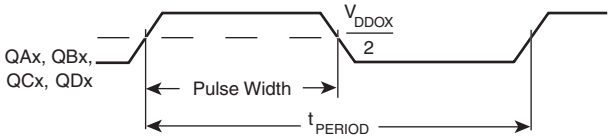
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



PART-TO-PART SKEW

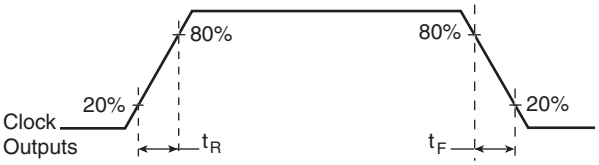


OUTPUT SKEW

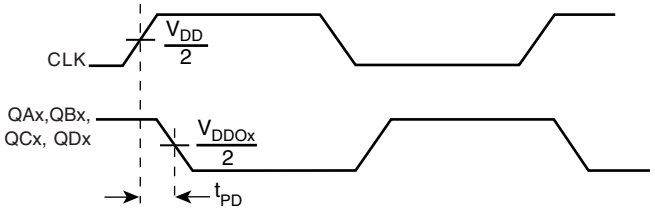


$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

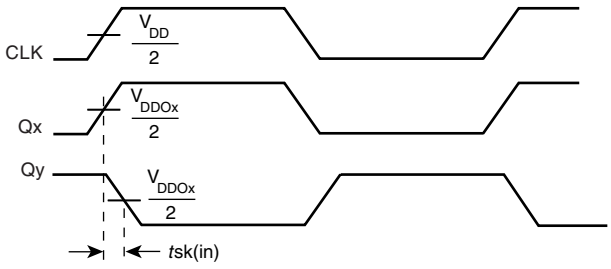
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



INVERTING SKEW

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8701-01 is: 1819

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

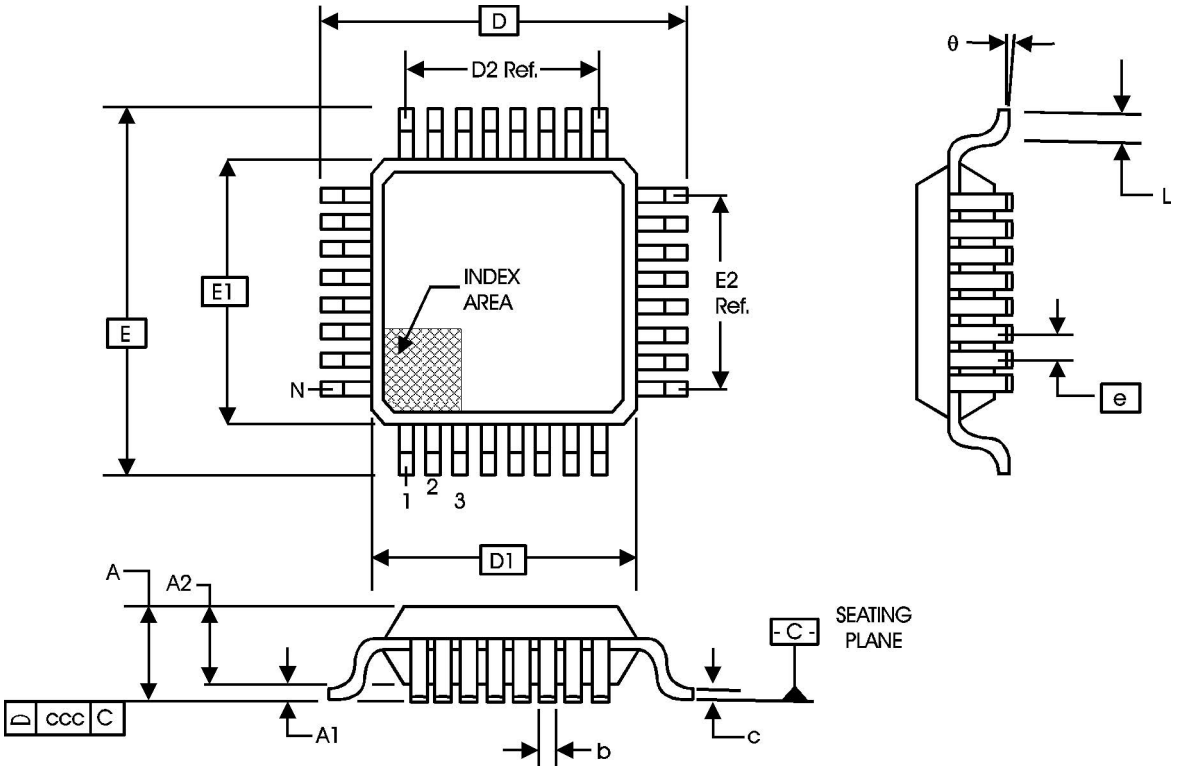


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8701AY-01	ICS8701AY-01	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8701AY-01T	ICS8701AY-01	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4A & T4C	4 & 6	DC Characteristics tables revised. I_{DD} row, value changed from 70mA Max. to 95mA Max.	8/1/01
B	T5A & T5B	5 & 7	AC Characteristics tables revised: t_{PD} symbol (Propagation Delay row), changed to $tp_{HL.}$ Added test conditions to Bank and Output Skews. Revised notes.	8/7/01
B	T2 T5A & T5B	2 4 & 5	Pin Characteristics table, added 15pF Max. to C_{PD} row. Revised notes in AC tables.	8/29/01
C	T5B	4	Added extra AC characteristics table to include Inverting Skew parameters.	2/8/02
C	T1	2	Pin Description Table, revised nMR/OE description.	8/21/02
D	T2 T4A T4B T5A & T5B	2 3 3 4 & 5	Pin Characteristics Table - changed C_{IN} max. 4pF to 4pF typical. Added 5Ω min. and 12Ω max. to R_{OUT}. Combined 3.3V and Mixed 3.3V/2.5V Power Supply Tables. LVCMOS Table - changed V_{IH} max. from 3.765V to V_{DD} + 0.3V. Combined 3.3V and Mixed 3.3V/2.5V LVCMOS Tables. AC Characteristics Tables - deleted tp_{HL} row. Changed tp_{LH} to t_{PD}. Updated format throughout data sheet.	11/17/03
E	T5A & T5B	4 & 5 6	AC Characteristics Tables - changed t_{PD} min. from 2.5ns to 2.0ns. Parameter Measurement Section - Propagation Delay Diagram, Qx should be inverted and measurement should be from rising edge of clk to falling edge of Qx. Output Skew and Part-to-Part Skew Diagram should be measured on falling edge. Added Inverting Skew Diagram.	12/15/03