ICS87332I-01

÷2 Differential-to-2.5V/3.3V ECL/LVPECL Clock Generator

Integrated Circuit Systems, Inc.

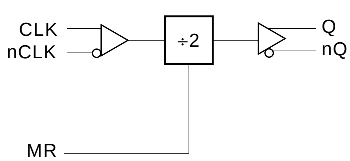
General Description

The ICS87332I-01 is a high performance ÷2 Differential-to-2.5V/3.3V ECL/LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels The ICS87332I-01 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS87332I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

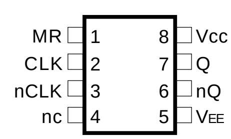
Features

- 1 ÷2 differential 2.5V/3.3V LVPECL / ECL output
- 1 CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 500MHz
- Maximum input frequency: 1GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Part-to-part skew: 400ps (maximum)
- Propagation delay: 1.6ns (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -2.375V to -3.8V
- -40°C to 85°C ambient operating temperature
- Compatible to part number MC100EP32

Block Diagram



Pin Assignment



ICS87332I-01

8-Lead SOIC
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR	Input	Pulldown	Master reset. When LOW, outputs are enabled. When HIGH, divider is reset forcing Q output LOW and nQ output HIGH. LVCMOS / LVTTL interface level.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
4	nc	Unused		No connect.
5	V_{EE}	Power		Negative supply pin.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

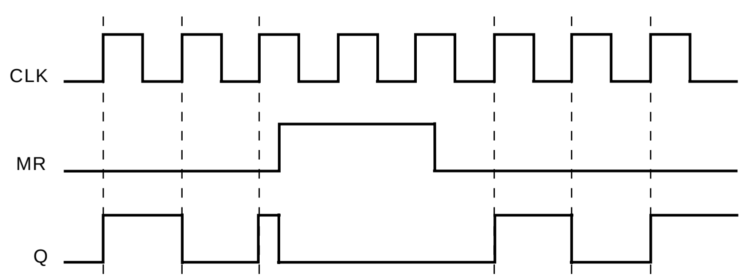


FIGURE 1 - TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, V_{EE} = 0, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				30	mA

TABLE 3B. LVCMOS DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, V_{EE} = 0, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	MR		-0.3		0.8	V
I_{IH}	Input High Current	MR	$V_{CC} = V_{IN}$ = 3.8V			150	µA
I_{IL}	Input Low Current	MR	V_{CC} = 3.8V, V_{IN} = 0V	-5			µA

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, V_{EE} = 0, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN}$ = 3.8V			150	µA
		nCLK	$V_{CC} = V_{IN}$ = 3.8V			5	µA
I_{IL}	Input Low Current	CLK	V_{CC} = 3.8V, V_{IN} = 0V	-5			µA
		nCLK	V_{CC} = 3.8V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.

TABLE 3D. LVPECL DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, V_{EE} = 0, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.65		0.9	V

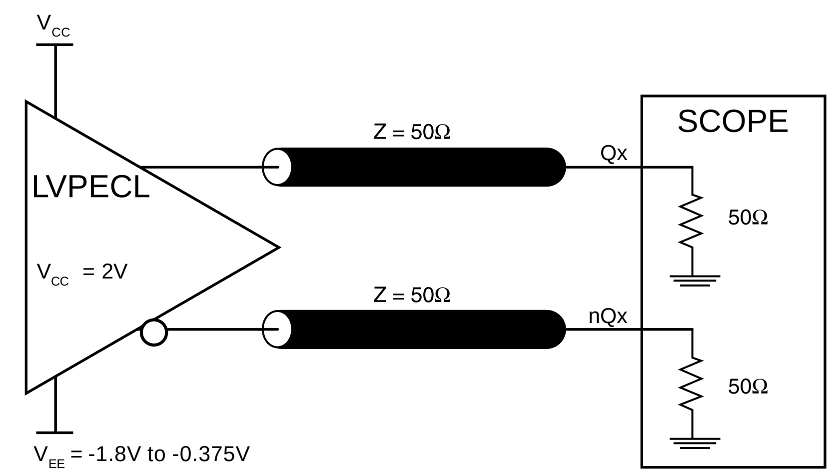
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4. AC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, V_{EE} = 0, TA = -40°C TO 85°C

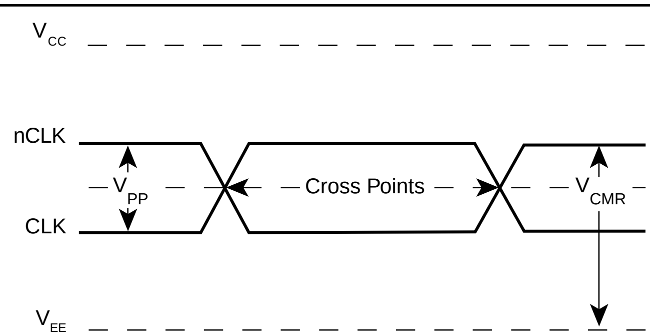
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				1	GHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 1GHz	1.1	1.4	1.6	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				400	ps
t_R	Output Rise Time	20% to 80%	200		700	ps
t_F	Output Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		49		51	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

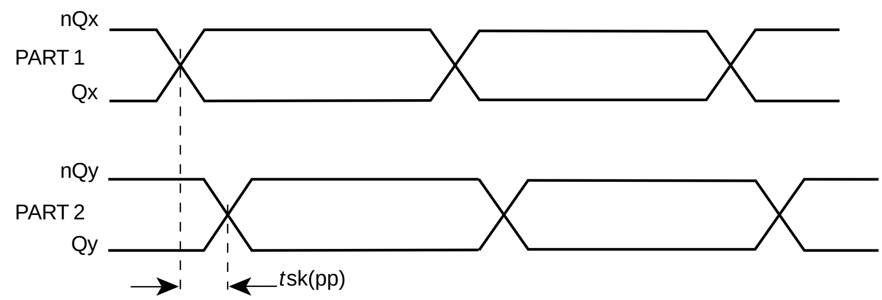
PARAMETER MEASUREMENT INFORMATION



OUTPUT LOAD TEST CIRCUIT

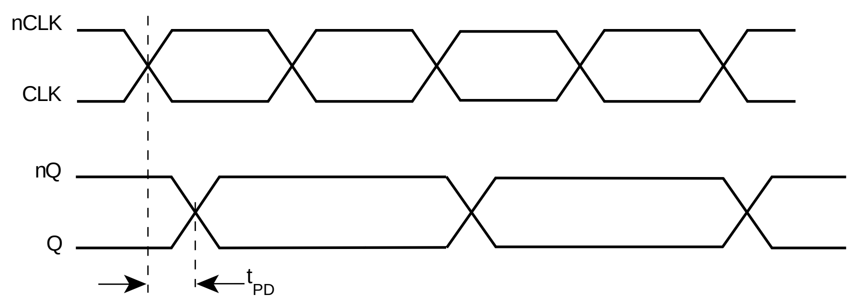


DIFFERENTIAL INPUT LEVEL

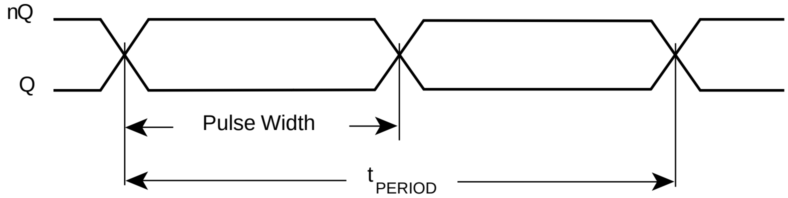


PART-TO-PART SKEW

INPUT AND OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87332-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87332-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 30mA = **114mW**
- Power $(outputs)_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30.2mW = **30.2mW**

Total Power $_{\_MAX}$ (3.8V, with all outputs switching) = 114mW + 30.2mW = **144.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.144W * 103.3°C/W = 99.9°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 5. THERMAL RESISTANCE θ_{JA} FOR 8-PIN SOIC, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 2.*

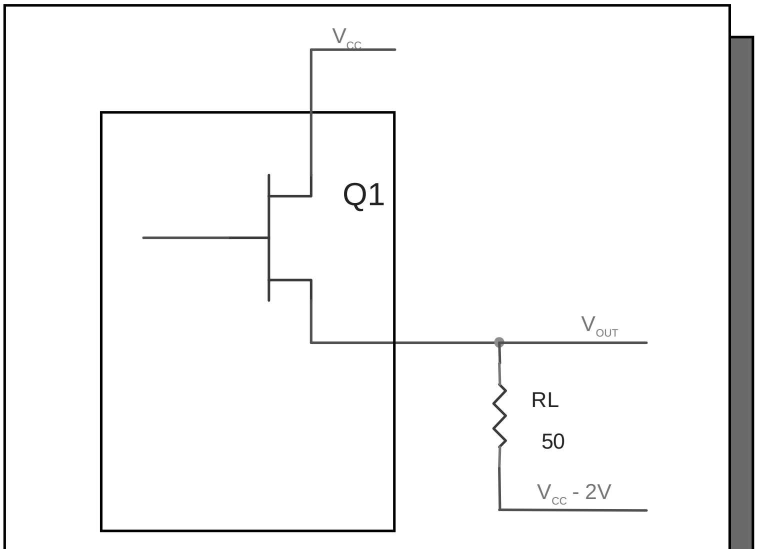


FIGURE 2 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.0V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87332I-01 is: 383

PACKAGE OUTLINE - M SUFFIX

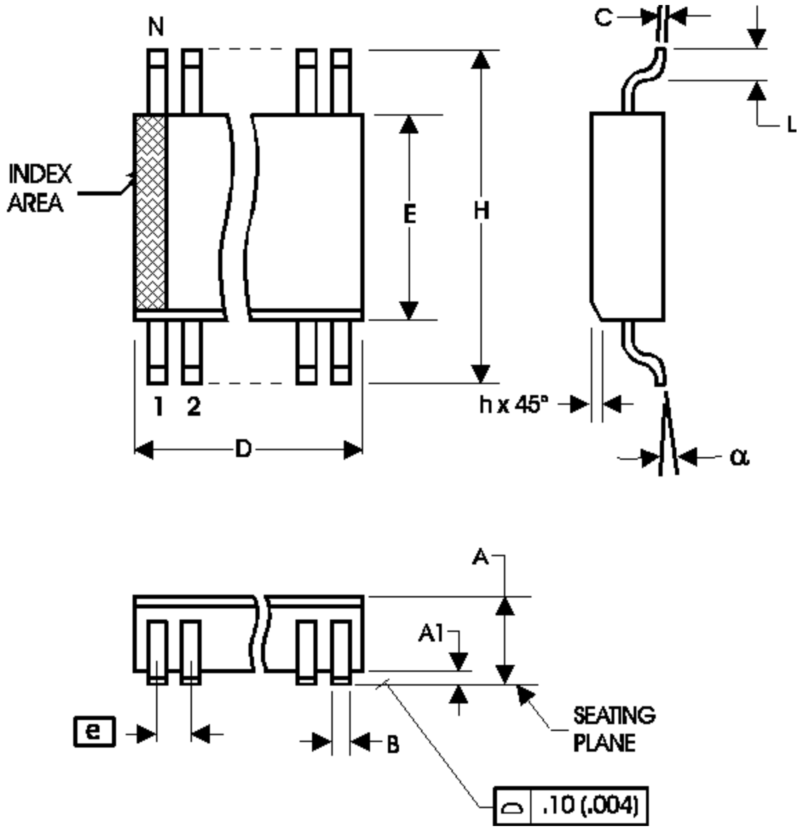


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87332AMI-01	332AI01	8 lead SOIC	96 per tube	-40°C to 85°C
ICS87332AMI-01T	332AI01	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C