Integrated Circuit Systems, Inc.

ICS87972I

LOW SKEW, 1-TO-12 LVCMOS/LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

GENERAL DESCRIPTION

The ICS87972I is a low skew, LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87972I has three selectable inputs and provides 14 LVCMOS/LVTTL outputs.

The ICS87972I is a highly flexible device. Using the crystal oscillator input, it can be used to generate clocks for a system. All of these clocks can be the same frequency or the device can be configured to generate up to three different frequencies among the three output banks. Using one of the single ended inputs, the ICS87972I can be used as a zero delay buffer/multiplier/divider in clock distribution applications.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 8.33MHz to125MHz. Input frequency range is 5MHz to 120MHz.

The ICS87972I also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period of the faster clock prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

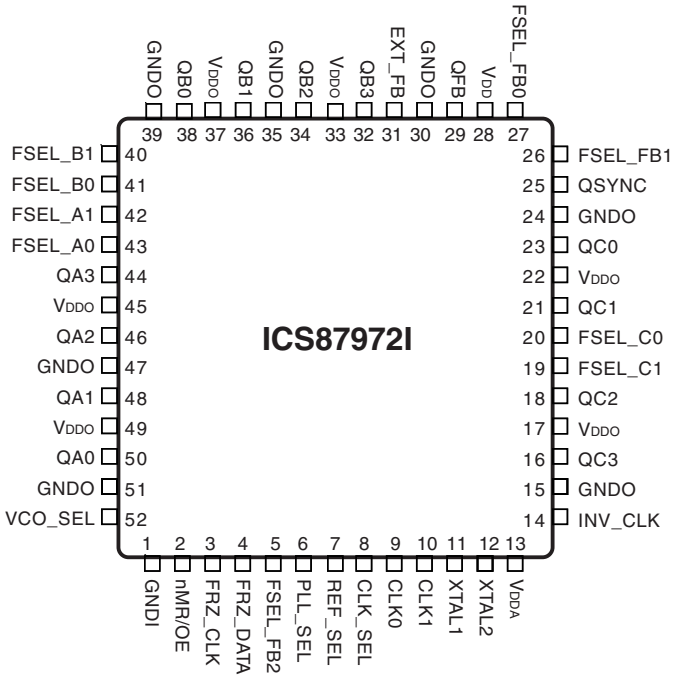
Example Applications:

1. *System Clock generator:* Use a 16.66 MHz Crystal to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
2. *Line Card Multiplier:* Multiply 19.44MHz from a back plane to 77.76MHz for the line Card ASICs and Serdes.
3. *Zero Delay buffer for Synchronous memory:* Fan out up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

FEATURES

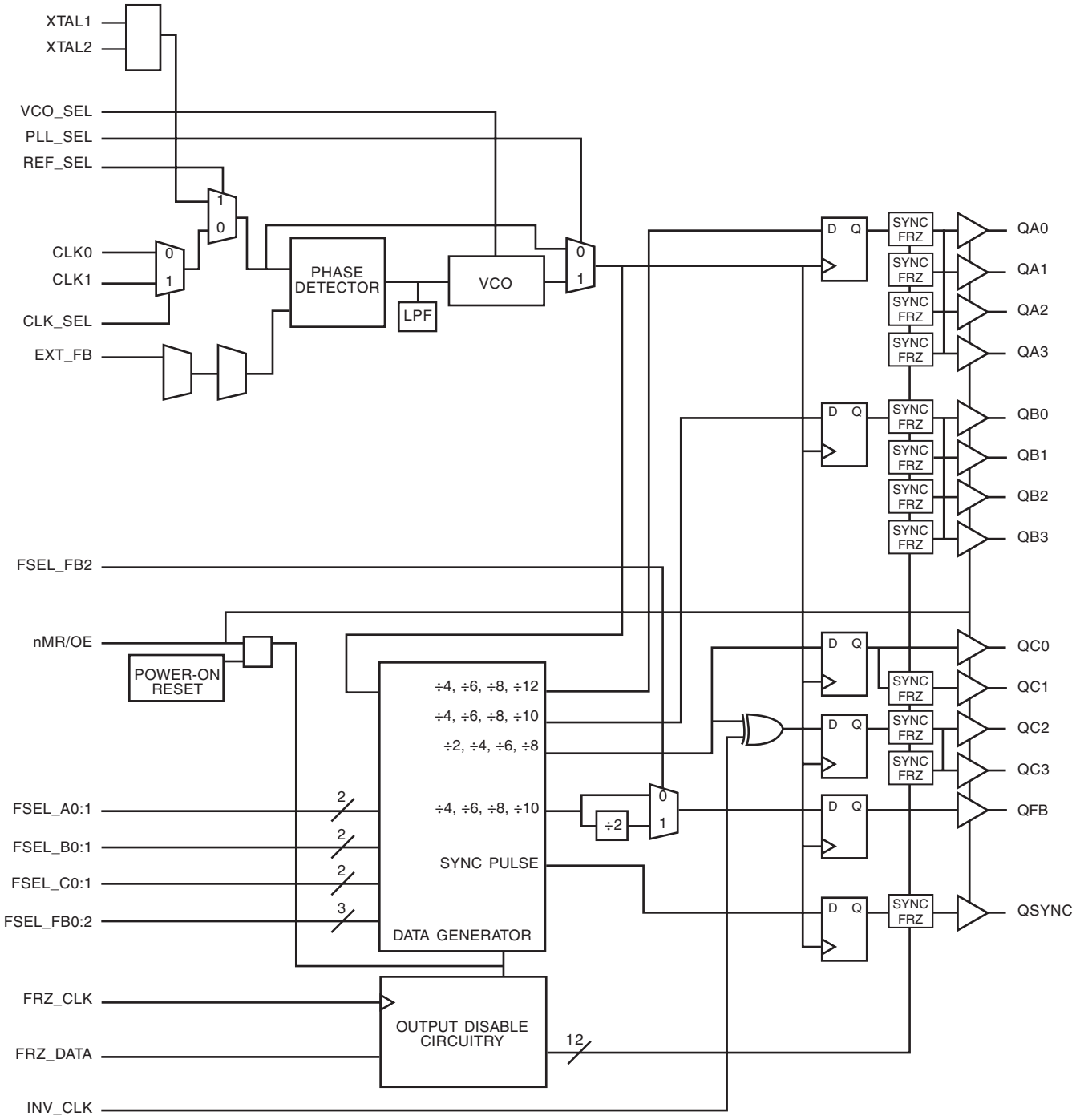
- Fully integrated PLL
- 14 LVCMOS/LVTTL outputs; (12)clocks, (1)feedback, (1)sync
- Selectable crystal oscillator interface or LVCMOS/LVTTL reference clock inputs
- CLK0, CLK1 can accept the following input levels: LVCMOS or LVTTL
- Output frequency range: 8.33MHz to 125MHz
- VCO range: 200MHz to 480MHz
- Output skew: 550ps (maximum)
- Cycle-to-cycle jitter: ±100ps (typical)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC972
- Compatible with PowerPC™ and Pentium™ Microprocessors

PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

BLOCK DIAGRAM



SIMPLIFIED BLOCK DIAGRAM

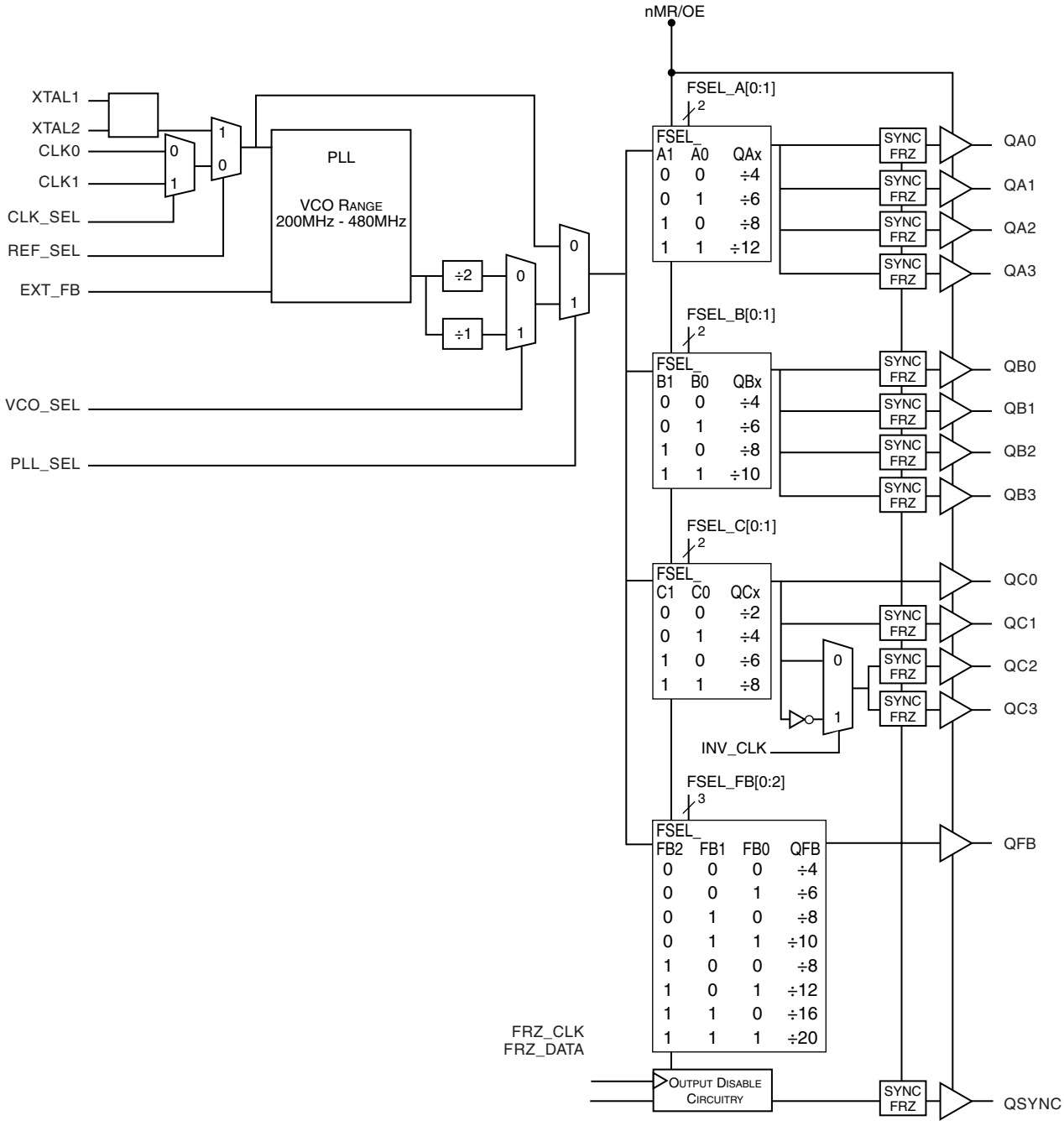


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVCMOS / LVTTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVCMOS / LVTTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVCMOS / LVTTL interface levels.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL and reference clocks. LVCMOS / LVTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between crystal and reference clock. When LOW, selects CLK0 or CLK1. When HIGH, selects crystal inputs. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTL interface levels.
11, 12	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
13	V_{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVCMOS / LVTTL interface levels.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17, 22, 33 37, 45, 49	V_{DDO}	Power		Output supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVCMOS / LVTTL interface levels.
25	QSYNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVCMOS / LVTTL interface levels.
28	V_{DD}	Power		Core supply pins.
29	QFB	Output		Feedback clock output. LVCMOS / LVTTL interface levels.
31	EXT_FB	Input	Pullup	External feedback. LVCMOS / LVTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Bank B clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVCMOS / LVTTL interface levels.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVCMOS / LVTTL interface levels.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Bank A clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DD}, V_{DDO} = 3.465V			18	pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

TABLE 3B. FEEDBACK CONFIGURATION SELECT FUNCTION TABLE

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

TABLE 3C. CONTROL INPUT SELECT FUNCTION TABLE

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	XTAL
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

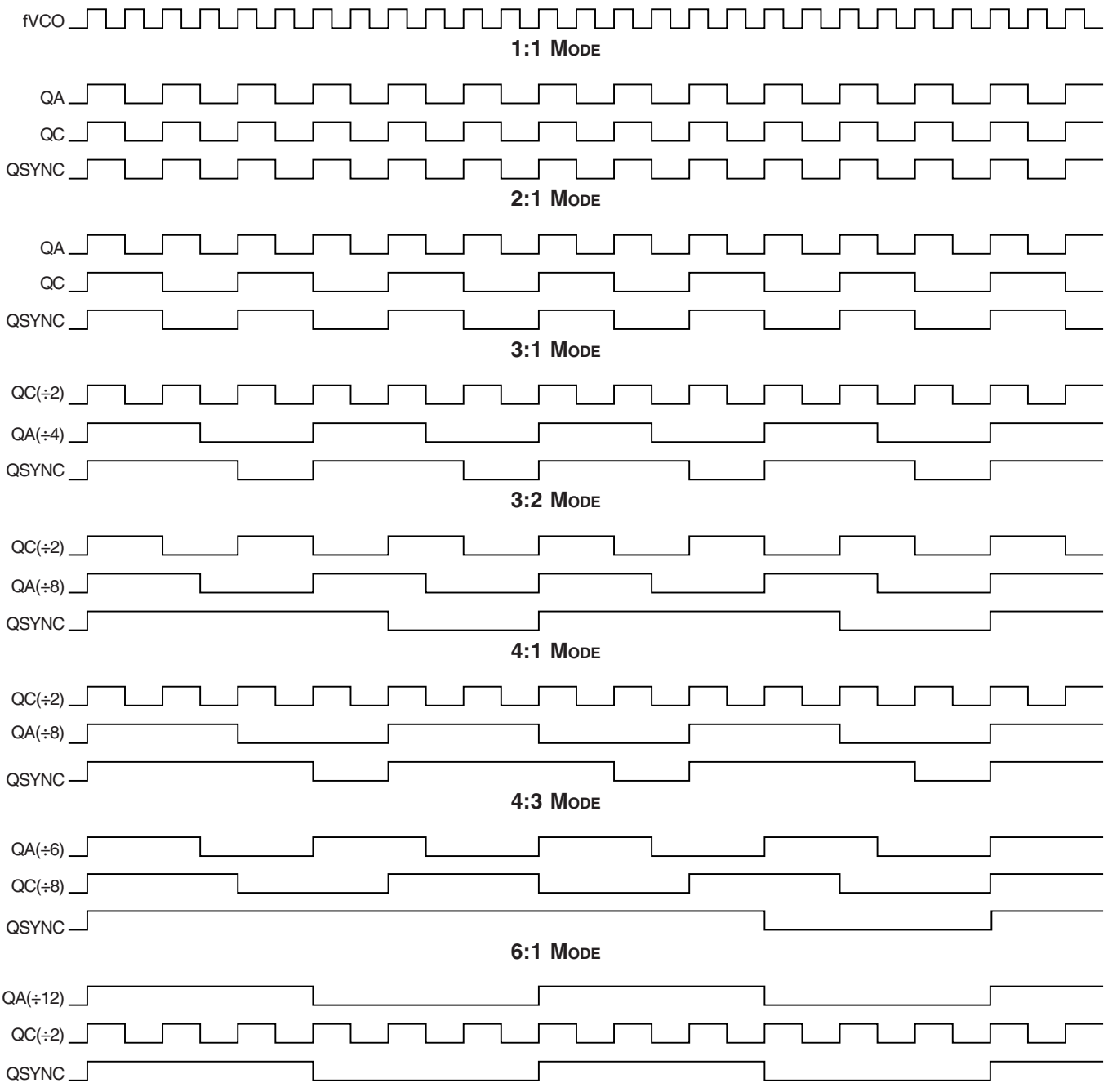


FIGURE 1. TIMING DIAGRAMS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.935	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	All power pins			250	mA
I_{DDA}	Analog Supply Current				20	mA

NOTE: Special thermal handling may be required in some configurations.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		3.6	V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current				±120	µA
V_{OH}	Output High Voltage	I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 20mA			0.5	V

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, CLK1; NOTE 1				120	MHz
		XTAL1, XTAL2		10		25	MHz
		FRZ_CLK				20	MHz

NOTE 1: Input frequency depends on the feedback divide ratio to ensure "clock * feedback divide" is in the VCO range of 200MHz to 480MHz.

TABLE 6. CRYSTAL CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

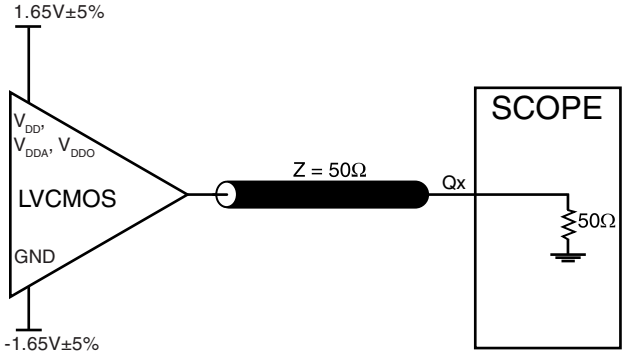
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 7. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

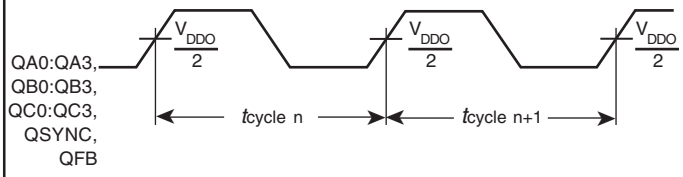
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		÷2			125	MHz
			÷4			120	MHz
			÷6			80	MHz
			÷8			60	MHz
t(Ø)	Static Phase Offset; NOTE 1	CLK0	QFB ÷ 8 In Frequency = 50MHz	-270	130	530	ps
		CLK1		-330	70	470	ps
*t*sk(o)	Output Skew; NOTE 2, 4					550	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4				±100		ps
f_{VCO}	PLL VCO Lock Range			200		480	MHz
t_{LOCK}	PLL Lock Time; NOTE 3					10	ms
t_R / t_F	Output Rise/Fall Time; NOTE 3		0.8V to 2V	0.15		1.2	ns
t_{PW}	Output Pulse Width			$t_{PERIOD}/2$ - 750	$t_{PERIOD}/2$ ± 500	$t_{PERIOD}/2$ + 750	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 3					10	ns
t_{PLZ}, t_{PHZ}	Output Disable TIme; NOTE 3					8	ns

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

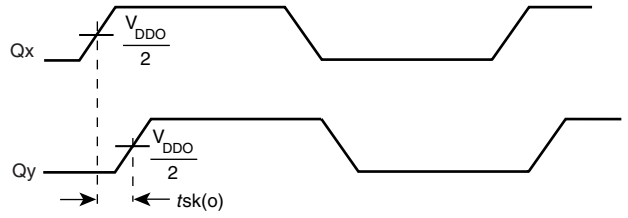


3.3V OUTPUT LOAD AC TEST CIRCUIT

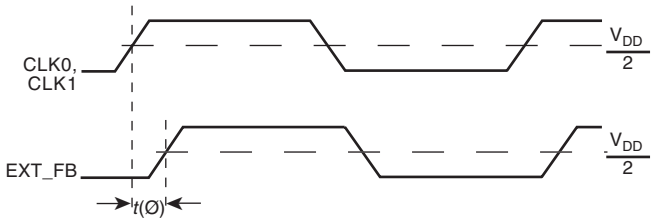


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

CYCLE-TO-CYCLE JITTER



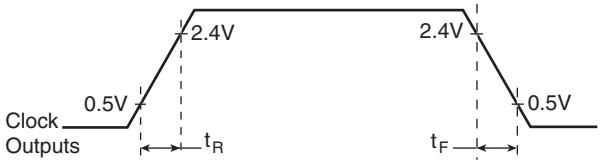
OUTPUT SKEW



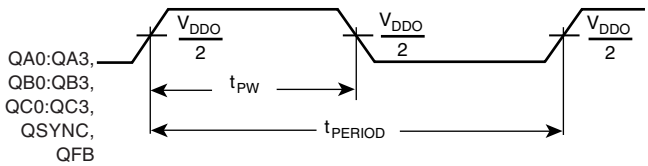
$t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

STATIC PHASE OFFSET



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

USING THE OUTPUT FREEZE CIRCUITRY

OVERVIEW

To enable low power states within a system, each output of ICS87972I (Except QC0 and QFB) can be individually frozen (stopped in the logic "0" state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the ICS87972I serial interface are FPGA's and ASICs.

PROTOCOL

The Serial interface consists of two pins, FRZ_Data (Freeze Data) and FRZ_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic "0" start bit followed by 12NRZ freeze enable bits. The period of each FRZ_DATA bit equals the period of the FRZ_CLK signal. The FRZ_DATA serial transmission should be timed so the ICS87972I can sample each FRZ_DATA bit with the rising edge of the FRZ_CLK signal. To place an output in the freeze state, a logic "0" must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic "1" must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic "0", it is used for the start bit of the next cycle; otherwise, the device will wait and won't start the next cycle until it sees a logic "0" bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

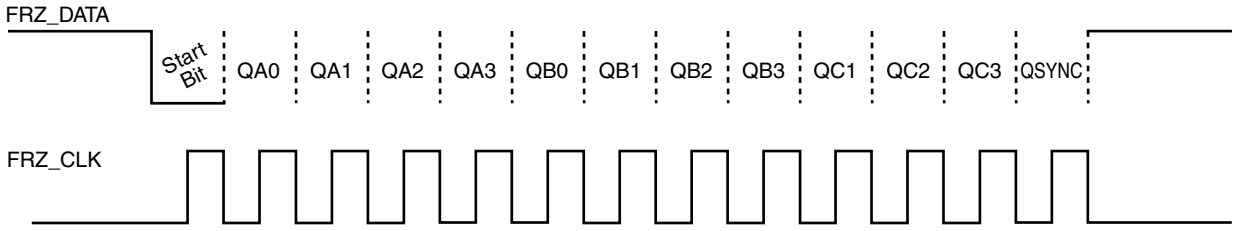


FIGURE 2A. FREEZE DATA INPUT PROTOCOL

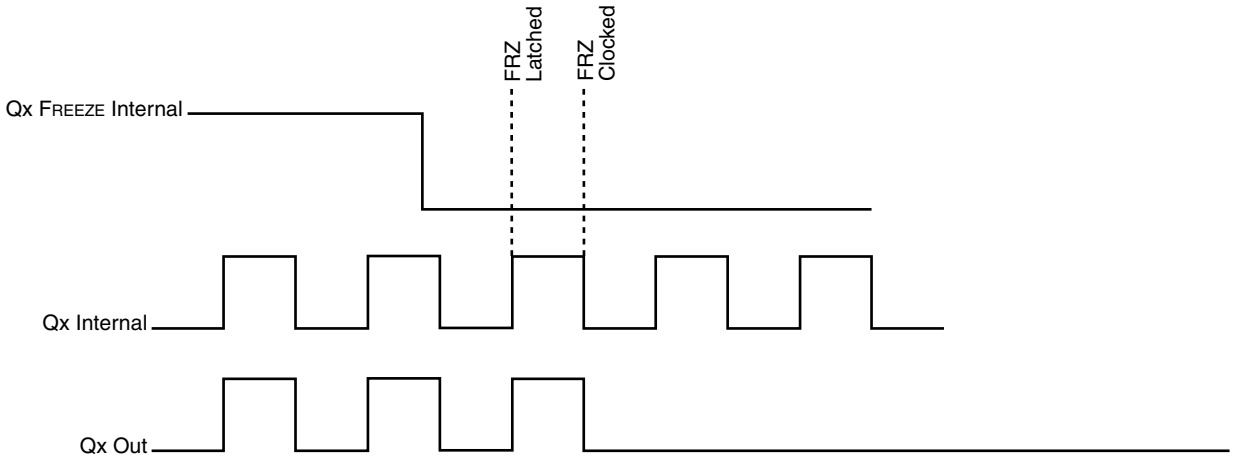


FIGURE 2B. OUTPUT DISABLE TIMING

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87972I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 3* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

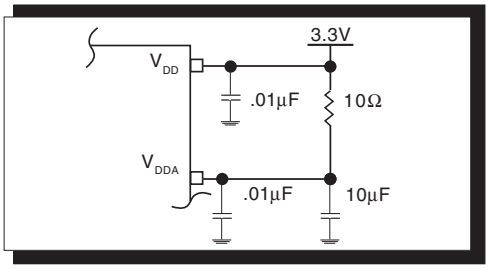


FIGURE 3. POWER SUPPLY FILTERING

APPLICATION SCHEMATIC EXAMPLE

Figure 4 shows an application schematic example of ICS87972I. This example provides general handling of input/output termination, logic control input and power supply filtering. In this example, the clock inputs are driven by LVCMOS drivers. Series termination for LVCMOS drivers is shown. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. The logic control input can be either hardwired on the board or controlled by LVCMOS drivers. In this example, both hardwired and LVCMOS driver controlling the logic input are shown. For the power supply pins, it is recommended at least one decoupling capacitor per power pin. The decoupling capacitors should be placed as close to the power pins as possible.

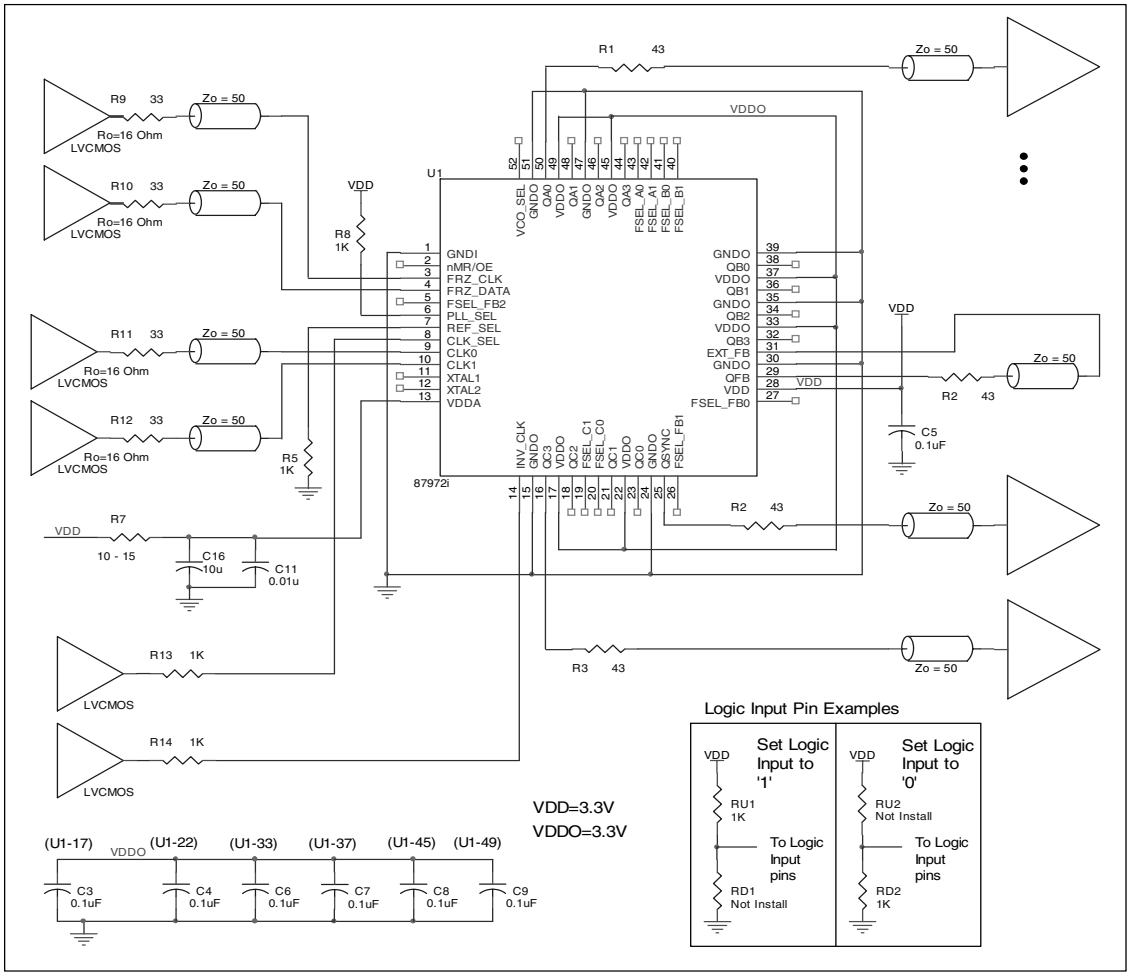


FIGURE 4. ICS87972I LAYOUT SCHEMATIC

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 52 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87972I is: 8364

PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP

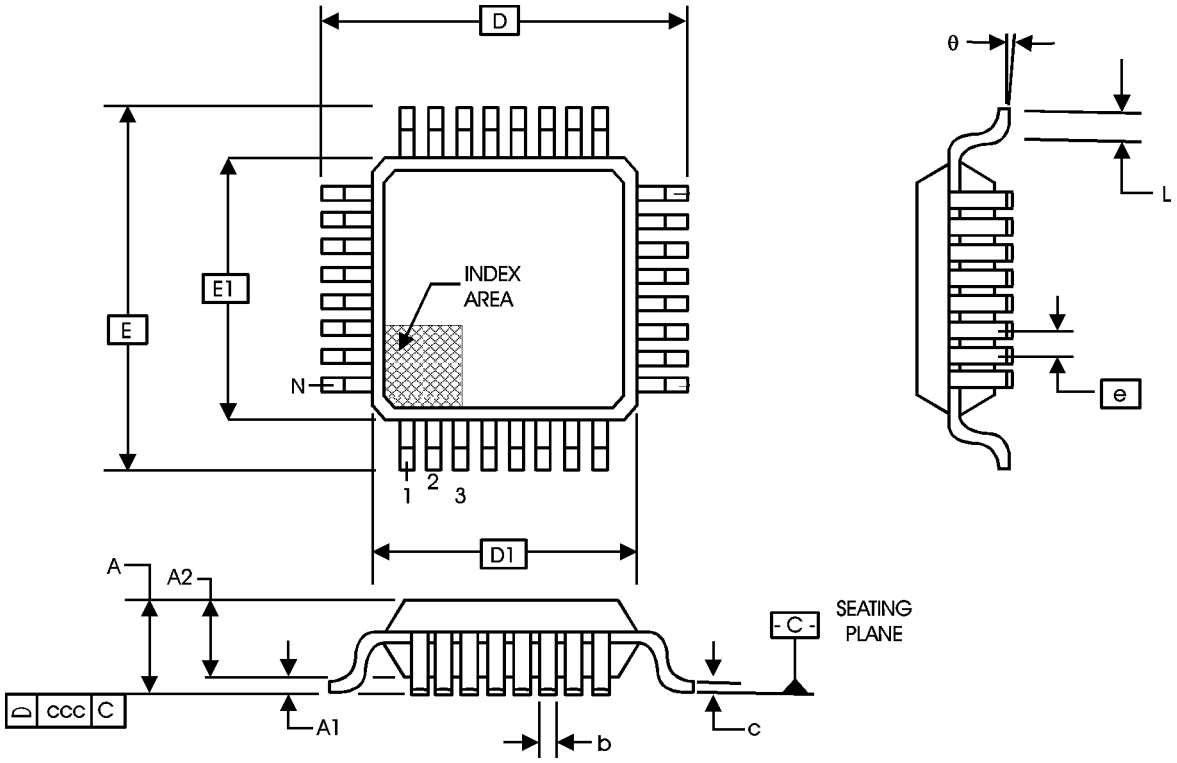


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87972DYI	ICS87972DYI	52 Lead LQFP	160 per tray	-40°C to 85°C
ICS87972DYIT	ICS87972DYI	52 Lead LQFP on Tape and Reel	500	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	1	4	Pin Description Table - added pins 20 and 21.	9/9/02
A		2	Block Diagram - added missing dividers to the Data Generator.	10/18/02
A		12	Revised Package Outline diagram.	12/5/02
B	T2 T4A	5 7 11	Pin Characteristics - changed the C_{PD} limit from 25pF typical to 18pf max. Power Supply Table - changed the I_{DD} limit from 215mA max. to 250mA max. Application Information: Added section, "Power Supply Filtering Techniques".	3/24/03
B	T2	5 10	Pin Characteristics - changed C_{IN} from 4pF max. to 4pF typical. Corrected Freeze Data labeling on Figure 2A.	5/8/03
C	T4A T6	7 8	Power Supply Table - changed minimum V_{DDA} from 3.135V to 2.935V. Crystal Table - changed ESR from 80Ω to 50Ω.	6/27/03
C		11	Added Schematic Layout	12/28/04