SONY

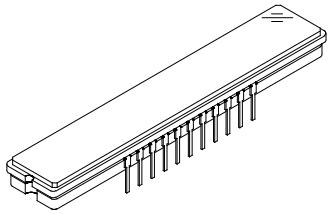
ILX528K

5000 × 3 pixel CCD Linear Sensor (Color)

Description

The ILX528K is a reduction type CCD linear sensor developing for color DPPC. This sensor reads A3-size documents at a density of 400 DPI.

22 pin DIP (Cer-DIP)



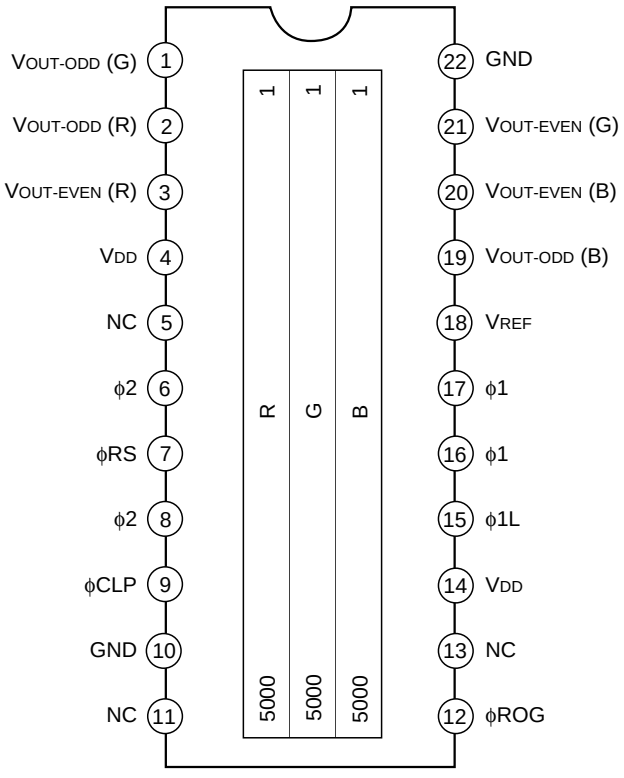
Features

- Number of effective pixels: 15000 pixels (5000 pixels × 3)
- Pixel size: 8µm × 8µm (8µm pitch)
- Distance between line: 64µm (8 lines)
- Maximum data rate: 40MHz/color
- Built-in clamp circuit
- Ultra low lag/High sensitivity
- Single 9V power supply
- Input Clock Pulse: CMOS 5V drive
- Number of output: 6 (2/color)
- Package: 22pin DIP (400mil)

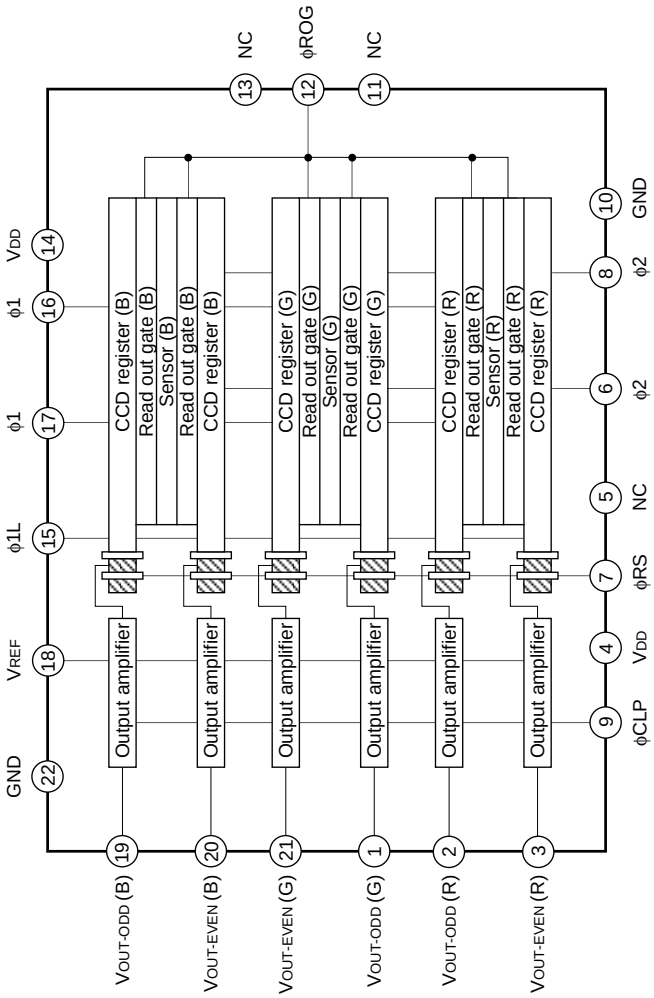
Absolute Maximum Ratings

• Supply voltage	V_{DD}	11	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



E97307-PS

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$V_{OUT-ODD}$ (G)	Signal output (G)	12	φROG	Clock pulse input
2	$V_{OUT-ODD}$ (R)	Signal output (R)	13	NC	NC
3	$V_{OUT-EVEN}$ (R)	Signal output (R)	14	V_{DD}	9V power supply
4	V_{DD}	9V power supply	15	φ1L	Clock pulse input
5	NC	NC	16	φ1	Clock pulse input
6	φ2	Clock pulse input	17	φ1	Clock pulse input
7	φRS	Clock pulse input	18	V_{REF}	Power supply (Clamp)
8	φ2	Clock pulse input	19	$V_{OUT-ODD}$ (B)	Signal output (B)
9	φCLP	Clock pulse input	20	$V_{OUT-EVEN}$ (B)	Signal output (B)
10	GND	GND	21	$V_{OUT-ODD}$ (G)	Signal output (G)
11	NC	NC	22	GND	GND

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	8.55	9	9.45	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φ1, φ2	$C_{\phi 1}$, $C_{\phi 2}$	—	900	—	pF
Input capacity of φ1L	$C_{\phi 1L}$	—	60	—	pF
Input capacity of φRS	$C_{\phi RS}$	—	60	—	pF
Input capacity of φCLP	$C_{\phi CLP}$	—	60	—	pF
Input capacity of φROG	$C_{\phi ROG}$	—	10	—	pF

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φ1L, φRS, φCLP	$f_{\phi 1}$, $f_{\phi 2}$, $f_{\phi 1L}$, $f_{\phi RS}$, $f_{\phi CLP}$	—	1	20	MHz

Input Clock Pulse Voltage

Item		Min.	Typ.	Max.	Unit
φ1, φ2, φ1L, φRS, φCLP, φROG Pulse Voltage	High level	4.75	5.0	5.25	V
	Low level	–0.3	0	0.1	V

Electrooptical Characteristics (Note 1)

Ta = 25°C, V_{DD} = 9V, f_{RS} = 1MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	1.19	1.7	2.21	V/(lx · s)	Note 2
	Green	R_G	2.17	3.1	4.03		
	Blue	R_B	1.47	2.1	2.73		
Sensitivity nonuniformity		PRNU	—	5	15	%	Note 3
Saturation output voltage		V_{SAT}	1	1.5	—	V	Note 4
Saturation exposure	Red	SE_R	0.35	0.68	—	lx · s	Note 5
	Green	SE_G	0.25	0.48	—		
	Blue	SE_B	0.3	0.58	—		
Dark voltage average		V_{DRK}	—	1.5	3	mV	Note 6
Dark signal nonuniformity		DSNU	—	1.5	5	mV	Note 6
Image lag		IL	—	0.02	—	%	Note 7
Supply current		I_{VDD}	—	45	60	mA	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	170	—	Ω	—
Offset level		V_{OS}	—	4.4	—	V	Note 8
Dynamic range		DR	333	1000	—	—	Note 9

Notes

1) In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D20, D22 to D118. The odd black level is defined as average value of D19, D21 to D117.
2) For the sensitivity test light is applied with a uniform intensity of illumination.
3) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

   V_{OUT} = 500mV

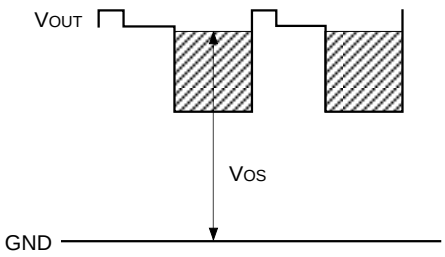
   $$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   Where the 5000 pixels are divided to blocks of 100, even and odd pixels, respectively. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4) Use below the minimum value of the saturation output voltage.
5) Saturation exposure is defined as follows.

   $$SE = \frac{V_{SAT}}{R}$$

6) Optical signal accumulated time τint stands at 10ms.
7) V_{OUT} = 500mV
8) Vos is defined as indicated bellow.

   V_{OUT} indicates $V_{OUT-EVEN}$ (R), $V_{OUT-ODD}$ (R), $V_{OUT-EVEN}$ (G), $V_{OUT-ODD}$ (G), $V_{OUT-EVEN}$ (B), $V_{OUT-ODD}$ (B)

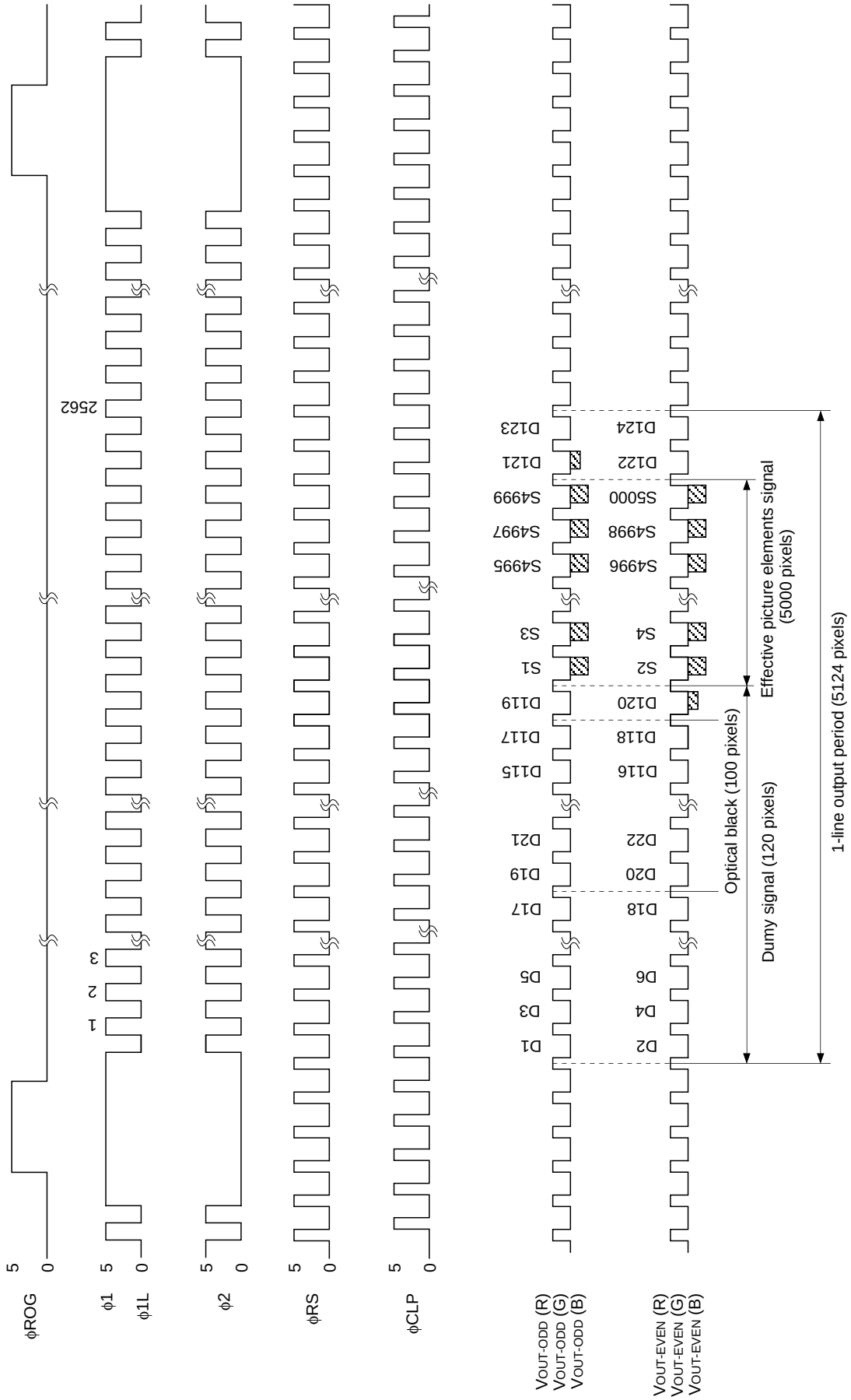


9) Dynamic range is defined as follows.

   $$DR = \frac{V_{SAT}}{V_{DRK}}$$

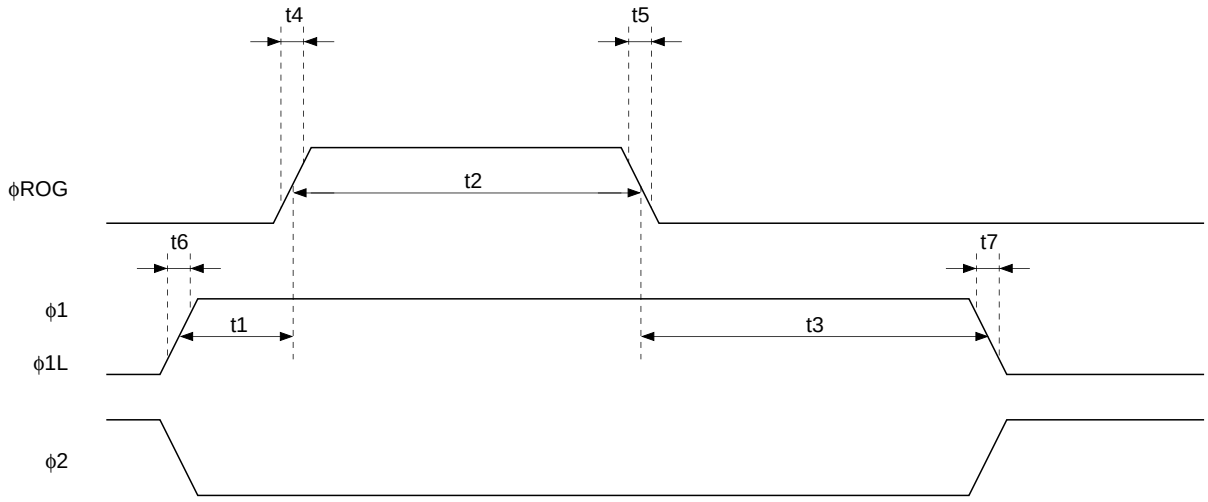
   When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.

Clock Timing Chart 1

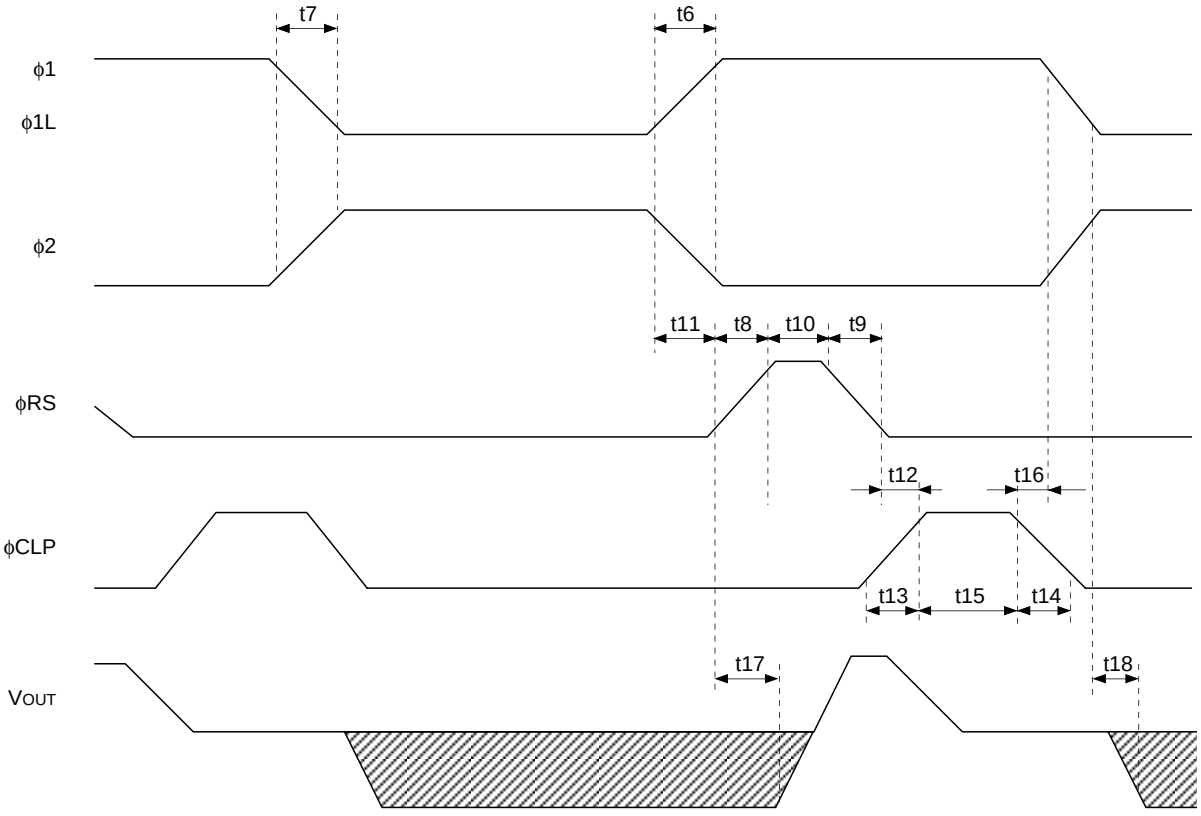


Note) The transfer pulses (φ1, φ2, φ1L) must have more than 2562 cycles.

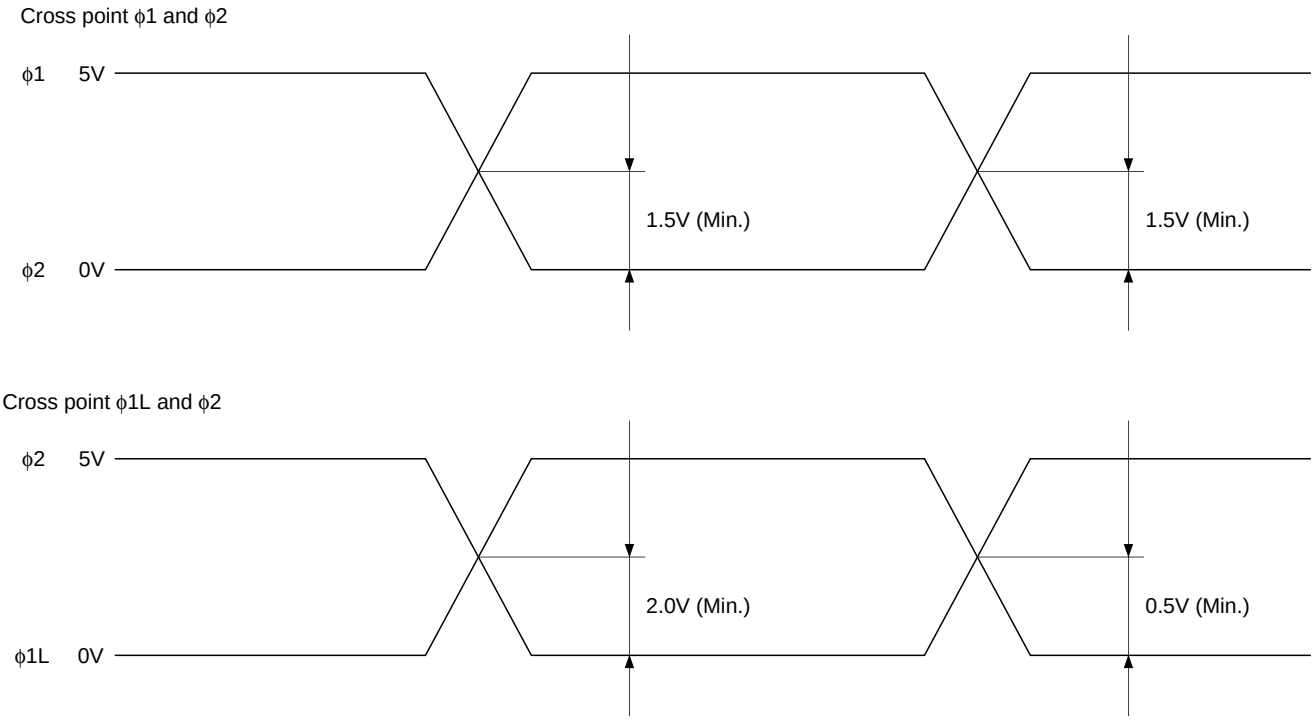
Clock Timing Chart 2



Clock Timing Chart 3



Clock Timing Chart 4

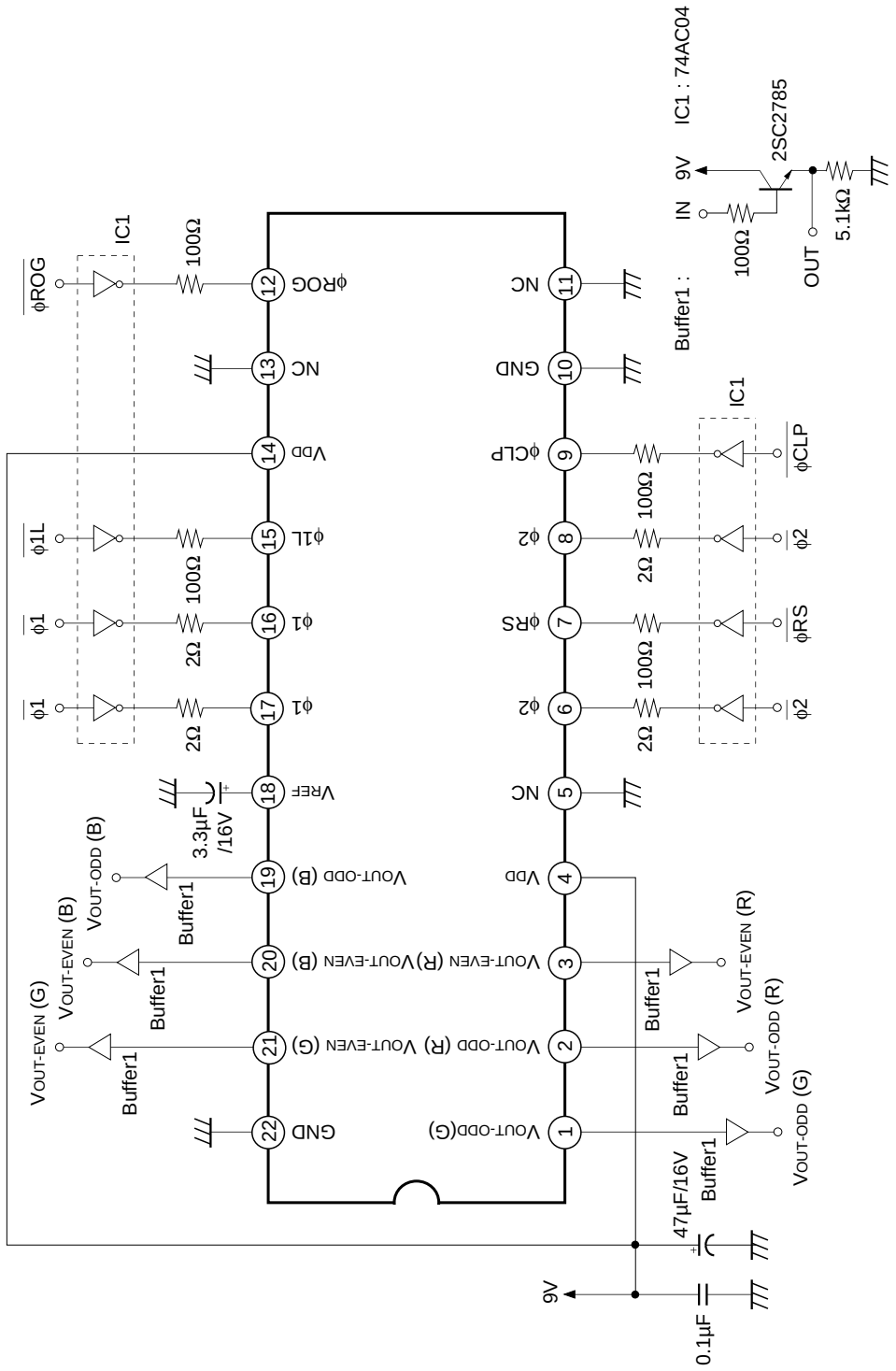


Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
ϕROG, ϕ1 pulse timing	t1	50	100	—	ns
ϕROG pulse high level period	t2	600	1000	—	ns
ϕROG, ϕ1 pulse timing	t3	400	1000	—	ns
ϕROG pulse rise time	t4	0	5	10	ns
ϕROG pulse fall time	t5	0	5	10	ns
ϕ1 pulse rise time /ϕ2 pulse fall time	t6	0	5	10	ns
ϕ1 pulse fall time /ϕ2 pulse rise time	t7	0	5	10	ns
ϕRS pulse rise time	t8	0	5	10	ns
ϕRS pulse fall time	t9	0	5	10	ns
ϕRS pulse high level period	t10	10	200*1	—	ns
ϕRS, ϕ1L pulse timing	t11	0	5	—	ns
ϕRS, ϕCLP pulse timing	t12	0	5	—	ns
ϕCLP pulse rise time	t13	0	5	10	ns
ϕCLP pulse fall time	t14	0	5	10	ns
ϕCLP pulse high level period	t15	10	200*1	—	ns
ϕCLP ϕ1L pulse timing	t16	5	100*1	—	ns
Signal output delay time	t17	—	12	—	ns
	t18	—	12	—	ns

*1 These timing is the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*

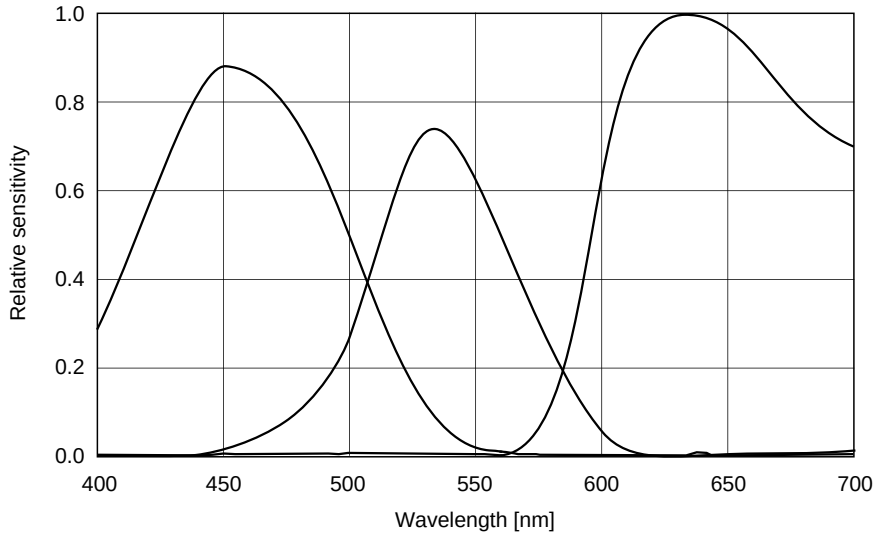


* Data rate fφRS = 1MHz.

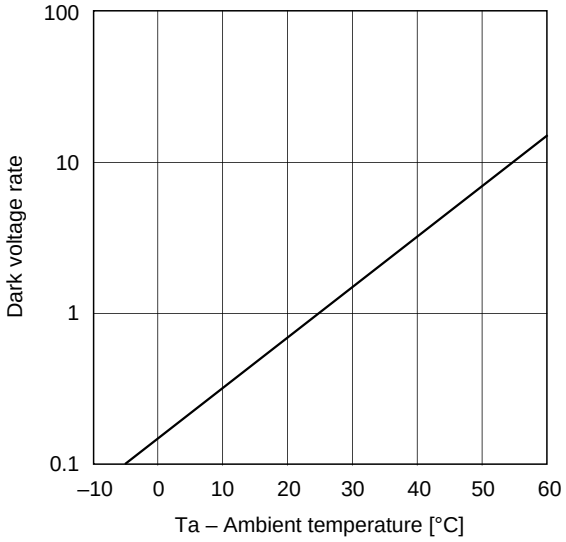
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 9V, Ta = 25°C)

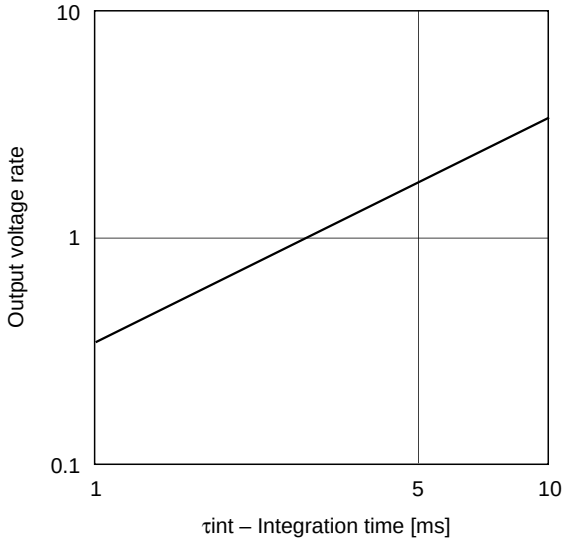
Spectral sensitivity characteristics (Standard characteristics)



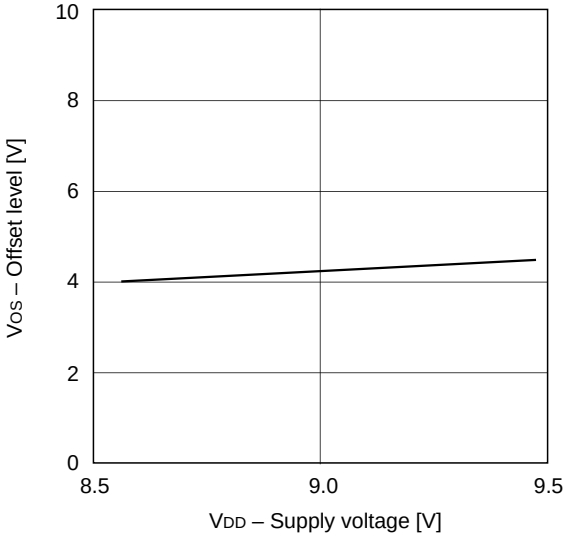
Dark voltage rate vs. Ambient temperature (Standard characteristics)



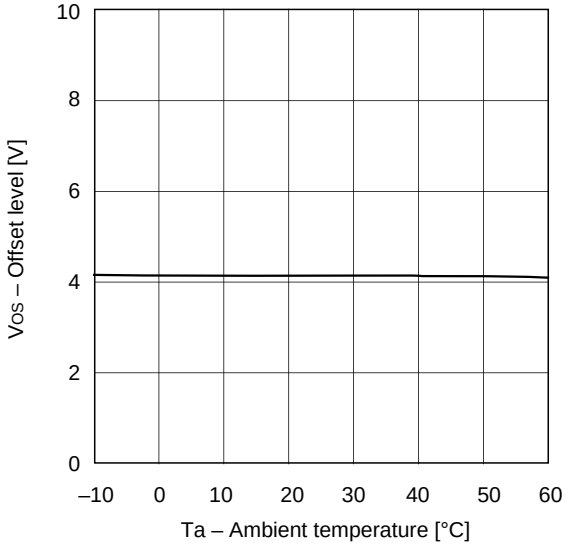
Output voltage rate vs. Integration time (Standard characteristics)



Offset level vs. Supply voltage (Standard characteristics)



Offset level vs. Ambient temperature (Standard characteristics)



Notes of Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

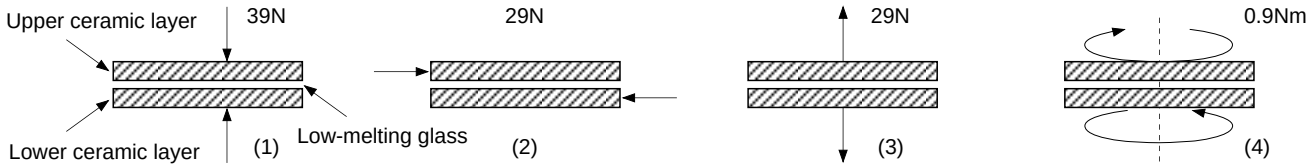
a) Remain within the following limits when applying static load to the ceramic portion of the package:

(1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with soldering iron.

(3) Rapid cooling or heating

(4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

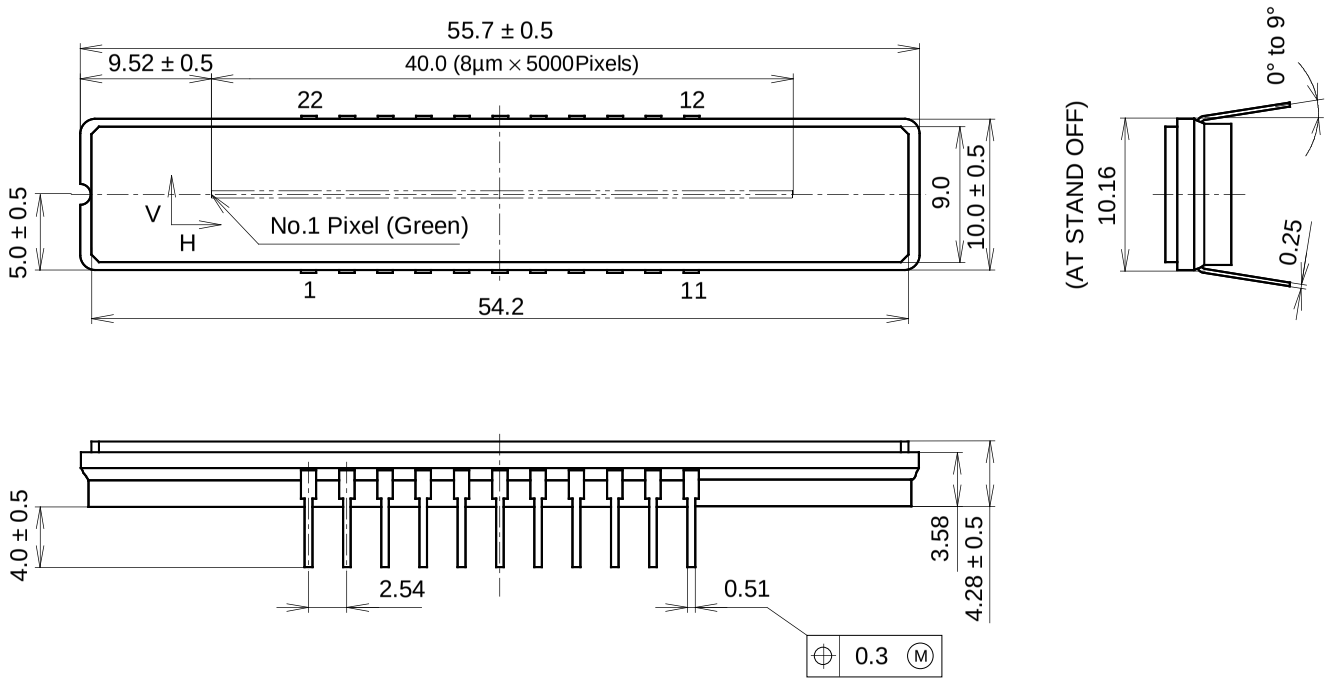
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Note that the normal output signal is not obtained immediately after the device power is turned on.

Package Outline Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	7.1g