Data Sheet No. PD60206_B

International
IOR Rectifier

IR2085S

HIGH SPEED, 100V, SELF OSCILLATING 50% DUTY CYCLE, HALF-BRIDGE DRIVER

Features

- Simple primary side control solution to enable half-bridge DC-Bus Converters for 48V distributed systems with reduced component count and board space.
- Integrated 50% duty cycle oscillator & half-bridge driver IC in a single SO-8 package
- Programmable switching frequency with up to 500kHz max per channel
- +/- 1A drive current capability optimized for low charge MOSFETs
- Adjustable dead-time 50nsec – 200nsec
- Floating channel designed for bootstrap operation up to +100Vdc
- High and low side pulse width matching to +/- 25nsec
- Adjustable overcurrent protection
- Undervoltage lockout and internal soft start

Product Summary

$V_{CC\ (max)}$	25V
$V_{offset(max)}$	100Vdc
High/low side output freq (f_{osc})	500kHz
Output Current (I_O)	+/-1.0A(typ.)
High/low side pulse width matching	+/- 25ns

Package

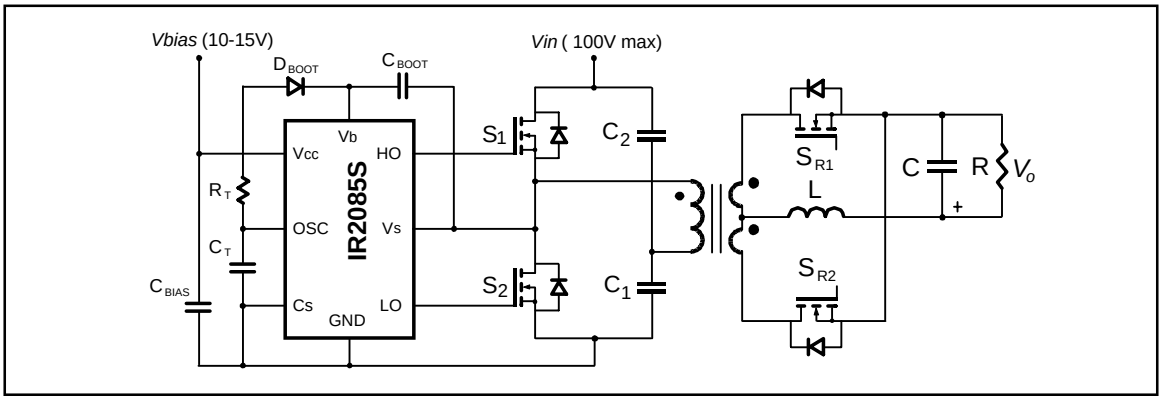
SO-8

Description

The IR2085S is a self oscillating half-bridge driver IC with 50% duty cycle ideally suited for 36V-75V half-bridge DC-bus converters. This product is also suitable for push-pull converters without restriction on input voltage.

Each channel frequency is equal to f_{osc}, where f_{osc} can be set by selecting R_T & C_T, where $f_{osc} \approx 1/(2*R_T.C_T)$. Dead-time can be controlled through proper selection of C_T and can range from 50 to 200nsec. Internal soft-start increases the pulse width during power up and maintains pulse width matching for the high and low outputs throughout the start up cycle. The IR2085S initiates a soft start at power up and after every overcurrent condition. Undervoltage lockout prevents operation if V_{CC} is less than 7.5Vdc.

Simplified Circuit Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. All currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_b	High side floating supply voltage	-0.3	150	V
V_{CC}	Low side supply voltage	—	25	
V_S	High side floating supply offset voltage	V_b - 25	V_b + 0.3	
V_{HO}	High side floating output voltage	V_b - 0.3	V_b + 0.3	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
OSC	OSC pin voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Cs pin voltage	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset voltage slew rate	-50	+50	V/ns
I_{CC}	Supply current	—	20	mA
P_D	Package power dissipation	—	1.0	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	-55	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
Vb	High side floating supply voltage	V_{dd} -0.7	15	Vdc
V_S	Steady state high side floating supply offset voltage	-5	100	
V_{CC}	Supply voltage	10	15	
I_{CC}	Supply current (Note 2)	—	5	mA
R_T	Timing resistor	10	100	KΩ
C_T	Timing capacitor	47	1000	pF
fosc(max)	Operating frequency (per channel)	—	500	KHz
T_J	Junction temperature	-40	125	°C

Note1: Care should be taken to avoid output switching conditions where the Vs node flies inductively below ground by more than 5V.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, C_{LOAD} = 1000 pF, and T_A = 25°C unless otherwise specified.

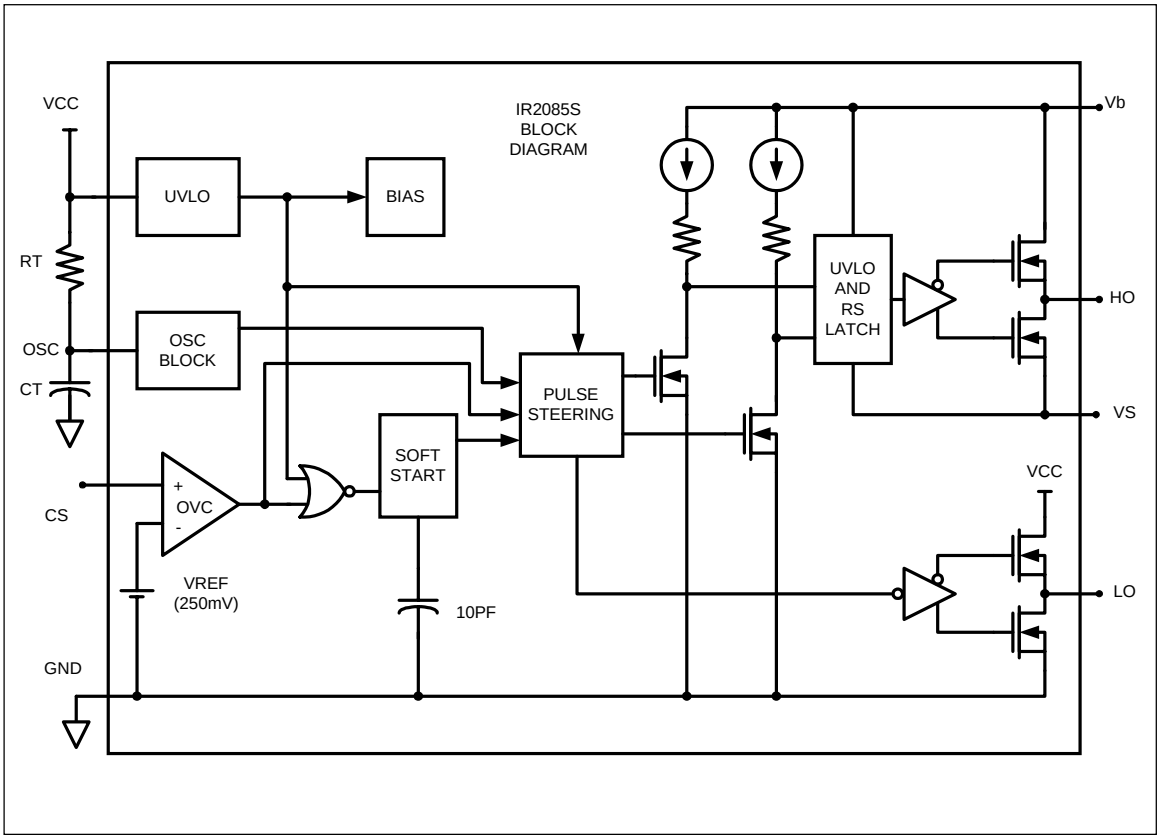
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_r	Turn-on rise time	—	40	60	nsec	V_S = 0V
t_f	Turn-off fall time	—	20	30		
fosc	Per channel output frequency	500	—	—	KHz	C_T =100pF, R_T =10Kohm
tdt	High/low output dead time	50	—	—	nsec	
t_{dcs}	Overcurrent shut down delay	—	200	—		pulse on CS
PM	High/low pulse width mismatch	-25	—	25		V_S = 0V ~ 100V

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 12V, C_{LOAD} = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{OH}	High level output voltage, (V_{BIAS} - V_O)	—	—	1.5	V	
V_{OL}	Low level output voltage	—	—	0.1		
I_{leak}	Offset supply leakage current	—	—	50	µA	
I_{QBS}	Quiescent V_{BS} supply current	—	—	150		
I_{QCC}	Quiescent V_{CC} supply current	—	—	1.5	mA	
V_{CS+}	Overcurrent shutdown threshold	250	300	350	mV	
V_{CS-}	Overcurrent shutdown threshold	150	200	250	mV	
U_{VCC+}	Undervoltage positive going threshold	6.8	7.3	7.8	V	
U_{VCC-}	Undervoltage negative going threshold	6.3	6.8	7.3		
U_{VBS+}	High side undervoltage positive going threshold	6.8	7.3	7.8		
U_{VBS-}	High side undervoltage negative going threshold	6.3	6.8	7.3		
I_{O+}	Output high short circuit current	—	1.0	—	A	
I_{O-}	Output low short circuit current	—	1.0	—		

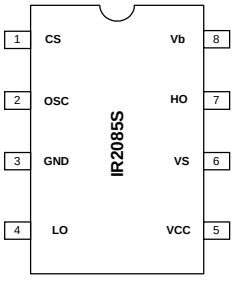
Functional Block Diagrams



Lead Definitions

Symbol	Description
V_{CC}	Logic supply
GND	Logic supply return
Vb	High side floating supply
V_S	Floating supply return
HO	High side output
LO	Low side output
CS	Current sense input
OSC	Oscillator pin

Lead Assignments



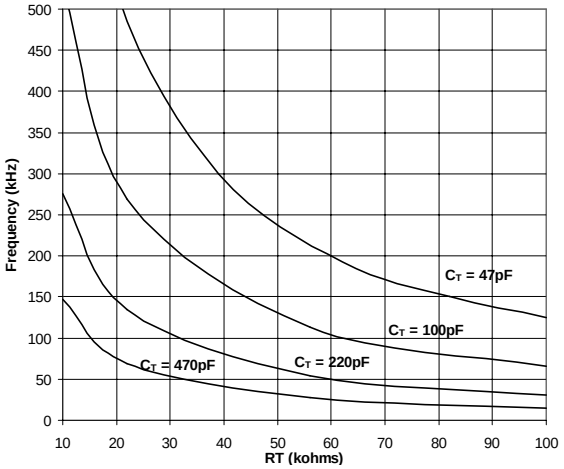


Fig. 1 Typical Output Frequency (-25°C to 125°C)

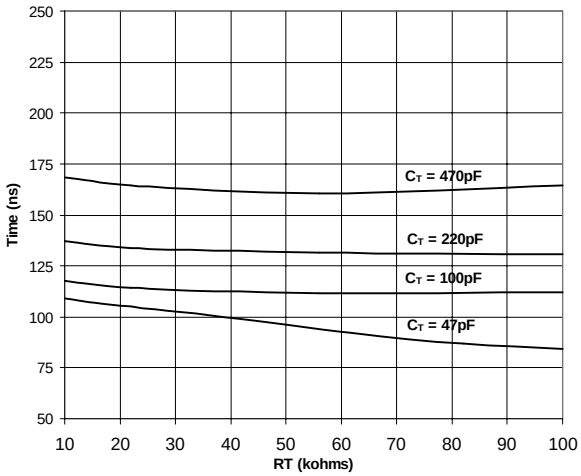


Fig. 2 Typical Dead Time (@25°C)

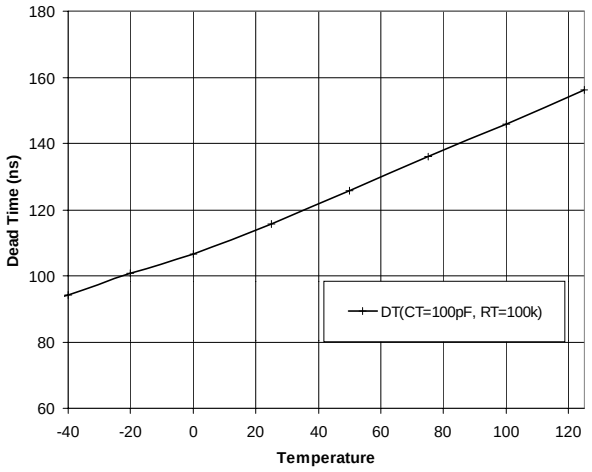


Fig. 3 Typical Dead Time vs Temperature

Pin descriptions

CS: The input pin to the overcurrent comparator. Exceeding the overcurrent threshold value specified in static electrical parameters section will terminate the output pulses and start a new soft-start cycle as soon as the voltage on the pin reduces below the threshold value.

OSC: The oscillator-programming pin. Only two components are required to program the oscillator frequency, a resistor (tied to the V_{CC} and CS pins), and a capacitor (tied to the CS and GND pins). The approximate oscillator frequency is determined by the following simple formula:

$$f_{OSC} = 1/ (2*R_T.C_T)$$

Where f_{OSC} frequency is in hertz (Hz), R_T resistance in ohms (Ω) and C_T capacitance in farads (F). The recommended range for the timing resistor is between 10kW and 100kW and the recommended range for the timing capacitor is between 47pF and 470pF. It is not recommended to use timing resistors less than 10kΩ.

For best performance, keep the timing component placement as close as possible to the IR2085S. It is recommended to separate the ground and V_{CC} traces to the timing components.

GND: Signal ground and power ground for all functions. Due to high current and high frequency operation, a low impedance circuit board ground plane is highly recommended.

HO, LO: High side and low side gate drive pins. The high and low side drivers can be used to drive the gate of a power MOSFET directly, without external buffers. The drivers are capable of 1.2A peak source and sink currents. It is recommended that the high and low side drive pins should be located very close to the gates of the high side and low side MOSFETs to prevent any delay and distortion of the drive signals. The power MOSFETs should be low charge to prevent any shoot through current.

V_b: The high side power input connection. The high side supply is derived from a bootstrap circuit using a low-leakage schottky diode and a ceramic capacitor. To prevent noise, the schottky diode and bypass capacitor should be located very close to the IR2085S and separated V_{CC} traces are recommended.

V_s: The high side power return connection. V_S should be connected directly to the source terminal of the high side MOSFET with the trace as short as possible.

V_{cc}: The IC bias input connection for the device. Although the quiescent V_{CC} current is very low, total supply current will be higher, depending on the MOSFET gate charge connected to the HO and LO pins, and the programmed oscillator frequency. Total V_{CC} current is the sum of quiescent V_{CC} current and the average current at HO and LO. Knowing the operating frequency and the MOSFET gate charge (Q_G), the average current can be calculated from:

$$I_{ave} = Q_G \text{ X } f_{osc}$$

To prevent noise problems, a bypass ceramic capacitor connected to V_{CC} and GND should be placed as close as possible to the IR2085S.

The IR2085S has an under voltage lockout feature for the IC bias supply, V_{CC}. The minimum voltage required on V_{CC} to make sure that the IC will work within specifications is 9.5V. Asymmetrical gate signals on HO and LO pins are expected when V_{CC} is between 7.5V and 8.5V.

Application Information

A 220 kHz half-bridge application circuit with full wave synchronous rectification is shown in figure 4. On the primary side, the IR2085S drives two IRF7493 - next generation low charge power MOSFETs. The primary side bias is obtained through a linear regulator from the input voltage for start-up, and then from the transformer in steady state. The IRF7380, a dual 80V power MOSFET in an SO8 package is used for the primary side bias function. Two IRF6603 - novel DirectFET

power MOSFETs are used on the secondary side in a self-driven synchronous rectification topology. DirectFETs practically eliminate MOSFET packaging resistance, which maximizes circuit efficiency. The DirectFET construction includes a copper "clip" across the backside of the silicon, which enables top-sided cooling and improved thermal performance. The DirectFET gate drive voltage is clamped to an optimum value of 7.5V with the IRF9956 dual SO-8 MOSFET. The secondary side bias scheme is designed to allow outputs of two bus converters to be connected in parallel, while operating from different input voltages, and also to allow continuing output current if one of the two input sources is shorted or disconnected.

Two ferrite cores are used for the transformer and inductor. The transformer core is a PQ20/16 (3F3) with 3:1 turns ratio and 1mil gap. The inductor core is an E14/3.5/5 (3F3) with one turn and a 5mil gap. The PCB has eight layers, with two layers for primary windings that are connected in parallel and each has three turns. Four layers are used for the secondary windings. Each layer has one turn and two layers are connected in parallel to get two sets of secondary windings. 4 oz Cu PCB is recommended for the primary and secondary windings. Each primary side winding is placed between the two sets of the secondary windings to balance the secondary side current.

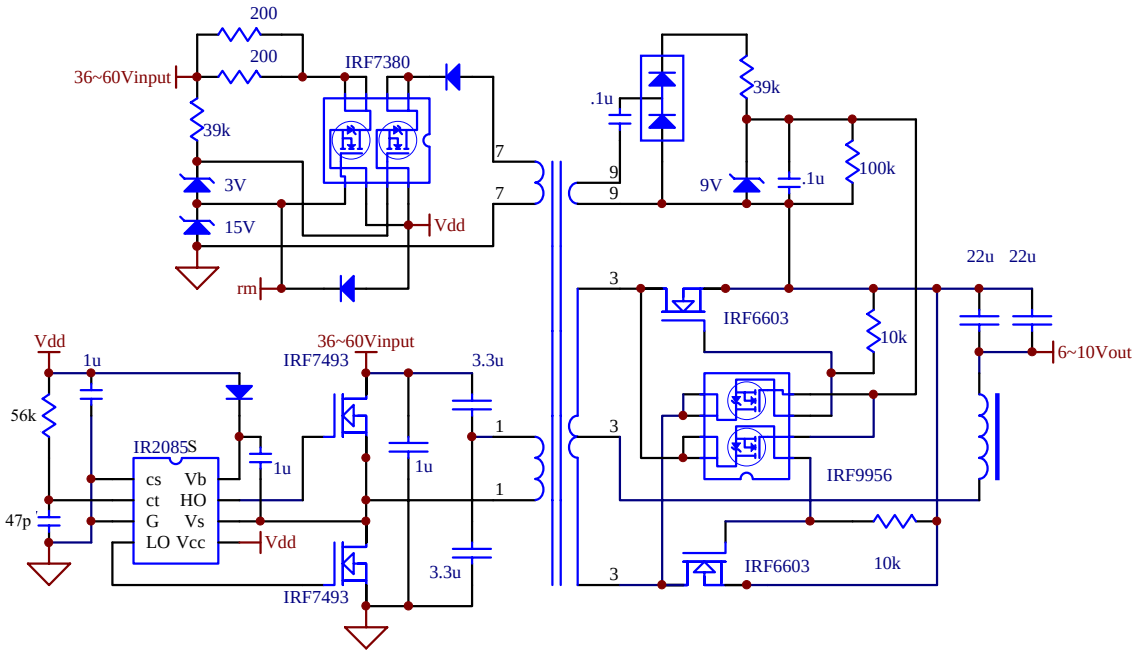
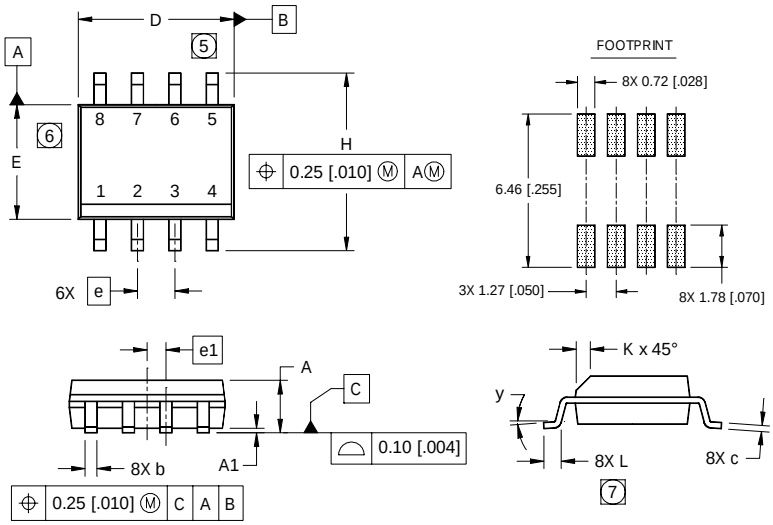


Figure 4 – IR2085S DC Bus converter reference design.

Case outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8-Lead SOIC

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This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web Site *http://www.irf.com/***.**
Data and specifications subject to change without notice
WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105
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