ispLSI™ 1032

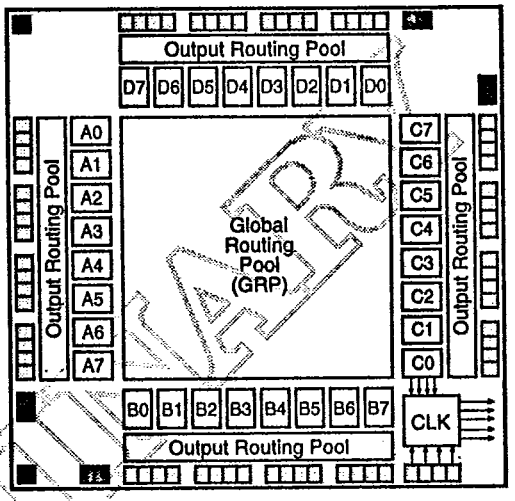
in-system programmable Large Scale Integration

T-46-19-07

Features

- In-system programmable HIGH DENSITY LOGIC
  - Member of Lattice's ispLSI Family
  - Fully Compatible with Lattice's pLSI™ Family
  - High Speed Global Interconnects
  - 64 I/O Pins, Eight Dedicated Inputs
  - 192 Registers
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - f_{max} = 80 MHz Maximum Operating Frequency
  - t_{pd} = 15 ns Propagation Delay
  - Low Power Consumption (I_{cc} 135mA Typ.)
  - TTL Compatible Inputs and Outputs
- In-system programmable 5-VOLT ONLY
  - Change Logic and Interconnects "on-the-fly" in Seconds
  - Reprogram Soldered Device for Debugging
  - Non-Volatile E²CMOS Technology
  - 100% Tested
- COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS
  - Complete Programmable Device can Combine Glue Logic and Structured Designs
  - 100% Routable at 80% Utilization
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Allows Global Interconnectivity
- pLSI/ispLSI™ DEVELOPMENT SYSTEM (pDS™)
  - Boolean Logic Compiler
  - Automatic Place and Route
  - Manual Partitioning
  - PC Platform
  - Easy to Use Windows Interface
- ADVANCED pLSI/ispLSI DEVELOPMENT SYSTEM
  - Industry Standard, Third Party Design Environments
  - Schematic Capture
  - Fully Automatic Partitioning
  - Automatic Place and Route
  - Comprehensive Logic and Timing Simulation
  - PC and Workstation Platforms

Functional Block Diagram



Description

The Lattice ispLSI 1032 is a High Density Programmable Logic Device featuring 5-Volt in-system programmability and in-system diagnostic capabilities. The device contains 192 Registers, 64 Universal I/O pins, eight Dedicated Input Pins, four Dedicated Clock Input Pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. It is the first device which offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 1032 device, but multiplexes four of the dedicated input pins to control in-system programming.

The basic unit of logic on the ispLSI 1032 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see figure 1). There are a total of 32 GLBs in the ispLSI 1032 device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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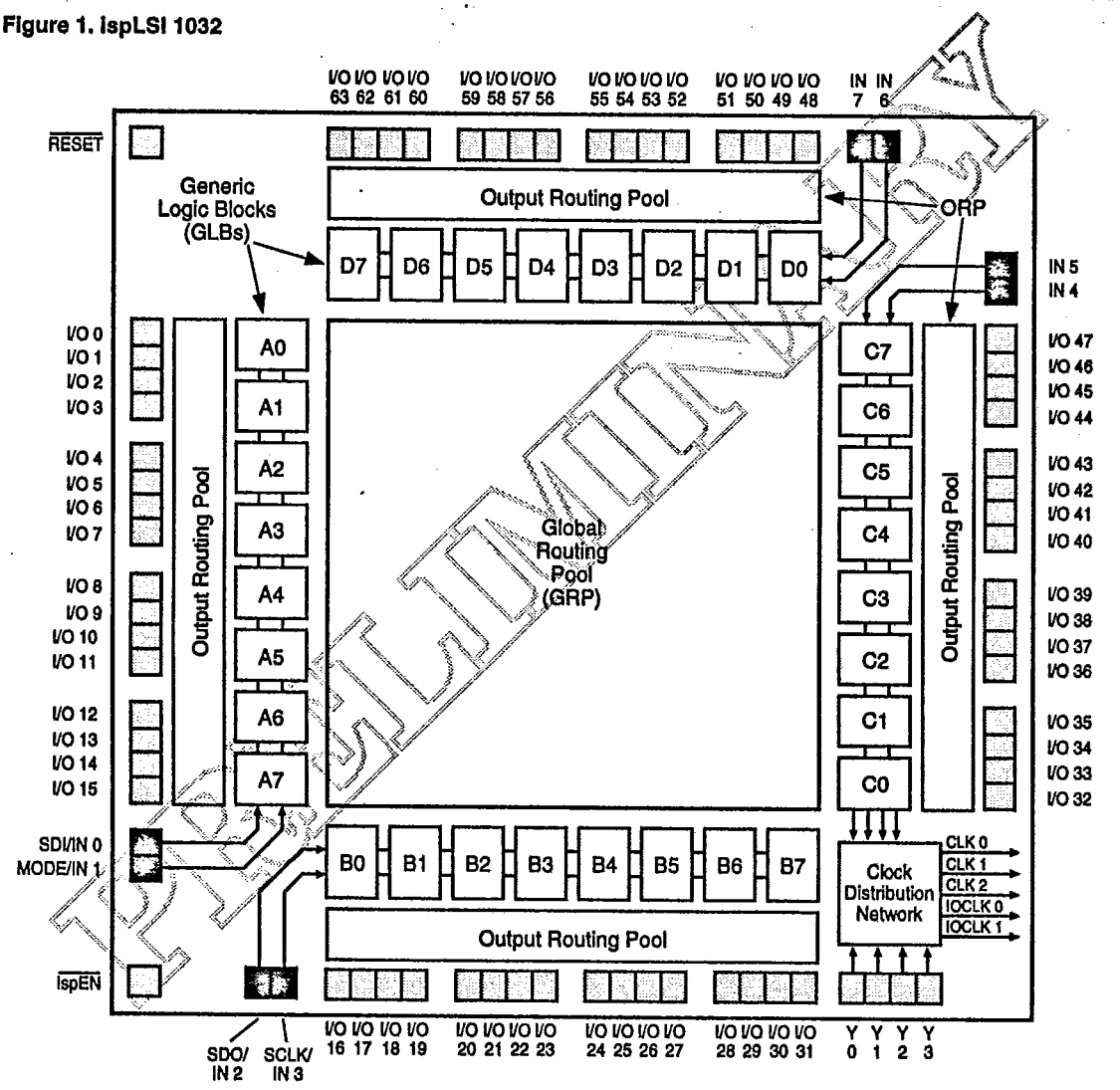
The device also has 64 I/O Cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

Functional Block Diagram

Figure 1. ispLSI 1032



Description (continued)

The 64 I/O Cells are grouped into four sets of 16 each. as shown in figure 1. Each of these I/O groups is associated with a logic Megablock through the use of the Output Routing Pool (ORP) and shares a common Output Enable (OE) signal.

Eight GLBs, 16 I/O Cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The ispLSI 1032 Device contains four of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 1032 device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0 to Y3) are brought into the distribution network, and five outputs (CLK 0 to CLK 2 and IOCLK 0, IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (C0 on the ispLSI 1032 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

The ispLSI 1032 device is part of Lattice's in-system programmable Large Scale Integration (ispLSI) family. This family contains a range of devices from the ispLSI 1016, with 96 registers, to the ispLSI 1048 with 288 registers. The ispLSI Family Product Selector Guide below lists key attributes of the devices along with the number of resources available.

ispLSI Family Product Selector Guide

DEVICE	ispLSI 1016	ispLSI 1024	ispLSI 1032	ispLSI 1048
GLBs	16	24	32	48
Registers	96	144	192	288
I/O Pins	32	48	64	96
Dedicated Inputs	4	6	8	10
Pin Count	44	68	84	120

Ordering Information

ispLSI 1032 – XX X X X

- Device Number
- Speed
  - -80 = 80 MHz fmax
  - -50 = 50 MHz fmax
- Power
  - L = Low
- Package
  - J = PLCC
- Grade
  - Blank = Commercial

Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 4 - IN 7	67, 84, 2, 19	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	23	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0	25	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1	42	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 2	44	Input/Output – This pin performs two functions. It is a dedicated clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 3	61	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	24	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	20	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	66	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	63	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O Cell on the device.
Y3	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O Cell on the device.
GND	1, 22, 43, 64	Ground (GND)
VCC	21, 65	V_{CC}

Absolute Maximum Ratings[1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 125°C

Ambient Temp. with Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC}	V

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O, Y Capacitance	10	pf	V_{CC}=5.0V, VI/O, Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

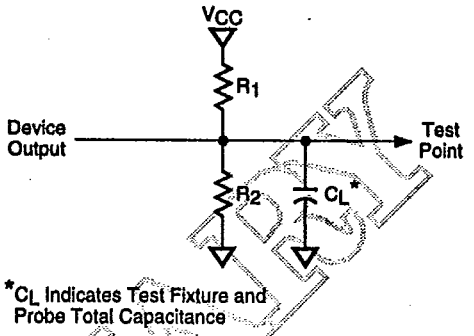
PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	1000	CYCLES

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L Indicates Test Fixture and Probe Total Capacitance

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA.	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA.	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$	–	–	10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V; V_{IH} = 3.0V F_{TOGGLE} = 20 MHz	–	135	195	mA

1. One output at a time for a maximum duration of one second. (Vout = 0.5V)
2. Measured at a frequency of 20 MHz using eight 16-bit counters.

External Switching Characteristics[1,2,3] ispLSI 1032-80

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	15	ns
t_{pd2}	1	2	Data Propagation Delay	–	15	20	ns
t_{co1}[5]	1	3	External Clock to Output Delay, ORP bypass	–	8	11	ns
t_{co2}[5]	1	4	External Clock to Output Delay	–	9	14	ns
t_{co3}	1	5	Internal Synch. Clock to Output Delay	–	15	20	ns
t_{co4}	1	6	Asynchronous Clock to Output Delay	–	13	20	ns
t_{r1}	1	7	External Pin Reset to Output Delay	–	13	20	ns
t_{r2}	1	8	Asynchronous PT Reset to Output Delay	–	15	22	ns
t_{en}	2	9	Input to Output Enable	–	13	20	ns
t_{dis}	3	10	Input to Output Disable	–	13	20	ns

External AC Recommended Operating Conditions[1,2,3] ispLSI 1032-80

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
f_{max}[4]	1	11	Clock Frequency with Internal Feedback	–	100	80	MHz
f_{max} (External)	1	12	Clock Frequency with External Feedback	–	70	50	MHz
t_{su1}	–	13	Setup Time before External Synch. Clock, 4PT bypass	9	6	–	ns
t_{su2}	–	14	Setup Time before External Synch Clock	12	8	–	ns
t_{su3}	–	15	Setup Time before Internal Synch. Clock	9	3	–	ns
t_{su4}	–	16	Setup Time before Asynchronous Clock	9	4	–	ns
t_{h1}	–	17	Hold time after External Synchronous Clock, 4PT bypass	2	-1	–	ns
t_{h2}	–	18	Hold time after External Synchronous Clock	2	-1	–	ns
t_{h3}	–	19	Hold time after Internal Synchronous Clock	8	2	–	ns
t_{h4}	–	20	Hold time after Asynchronous Clock	8	1	–	ns
t_{rw1}	–	21	External Reset Pulse Duration	10	8	–	ns
t_{rw2}	–	22	Asynchronous Reset Pulse Duration	10	8	–	ns
t_{wh1}, t_{wl1}	–	23,24	External Synchronous Clock Pulse Duration, High, Low	6	5	–	ns
t_{wh2}, t_{wl2}	–	25,26	Asynchronous Clock Pulse Duration, High, Low	6	5	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Standard 16-bit counter implementation using GRP feedback.
5. Clock to output specifications include a maximum skew of 2 ns.
6. Refer to Switching Test Conditions section.

Using I/O Cell

PARAMETER	TEST[4] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
tsu5	–	27	Setup Time before External Synchronous Clock	5	0	–	ns
tsu6	–	28	Setup Time before Internal Synchronous Clock	0	-3	–	ns
th5	–	29	Hold Time after External Synchronous Clock	8	4	–	ns
th6	–	30	Hold Time after Internal Synchronous Clock	15	11	–	ns
twh3, twl3	–	31,32	Clock Pulse Duration, High, Low	6	5	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Refer to Switching Test Conditions section.

External Switching Characteristics[1,2,3] ispLSI 1032-50

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	16	20	ns
t_{pd2}	1	2	Data Propagation Delay, ORP	–	19	25	ns
t_{co1}[5]	1	3	External Clock to Output Delay, ORP bypass	–	12	16	ns
t_{co2}[5]	1	4	External Clock to Output Delay	–	15	20	ns
t_{co3}	1	5	Internal Synch. Clock to Output Delay	–	21	28	ns
t_{co4}	1	6	Asynchronous Clock to Output Delay	–	21	28	ns
t_{r1}	–	7	External Pin Reset to Output Delay	–	21	28	ns
t_{r2}	–	8	Asynchronous PT Reset to Output Delay	–	24	30	ns
t_{en}	2	9	Input to Output Enable	–	21	28	ns
t_{dis}	3	10	Input to Output Disable	–	21	28	ns

External AC Recommended Operating Conditions[1,2,3] ispLSI 1032-50

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
f_{max}[4]	1	11	Clock Frequency with Internal Feedback	–	70	50	MHz
f_{max} (External)	1	12	Clock Frequency with External Feedback	–	45	33	MHz
t_{su1}	–	13	Setup Time before External Synch. Clock, 4PT bypass	14	10	–	ns
t_{su2}	–	14	Setup Time before External Synch Clock	17	13	–	ns
t_{su3}	–	15	Setup Time before Internal Synch. Clock	13	9	–	ns
t_{su4}	–	16	Setup Time before Asynchronous Clock	13	9	–	ns
t_{h1}	–	17	Hold time after External Synchronous Clock, 4PT bypass	7	3	–	ns
t_{h2}	–	18	Hold time after External Synchronous Clock	7	3	–	ns
t_{h3}	–	19	Hold time after Internal Synchronous Clock	11	5	–	ns
t_{h4}	–	20	Hold time after Asynchronous Clock	11	5	–	ns
t_{rw1}	–	21	External Reset Pulse Duration	15	13	–	ns
t_{rw2}	–	22	Asynchronous Reset Pulse Duration	15	13	–	ns
t_{wh1}, t_{wl1}	–	23,24	External Synchronous Clock Pulse Duration, High, Low	10	8	–	ns
t_{wh2}, t_{wl2}	–	25,26	Asynchronous Clock Pulse Duration, High, Low	10	8	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Standard 16-bit counter implementation using GRP feedback.
5. Clock to output specifications include a maximum skew of 2 ns.
6. Refer to Switching Test Conditions section.

Switching Characteristics[1,2,3] ispLSI 1032-50

Using I/O Cell

PARAMETER	TEST[4] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{su5}	–	27	Setup Time before External Synchronous Clock	10	5	–	ns
t_{su6}	–	28	Setup Time before Internal Synchronous Clock	0	-5	–	ns
t_{h5}	–	29	Hold Time after External Synchronous Clock	12	6	–	ns
t_{h6}	–	30	Hold Time after Internal Synchronous Clock	20	15	–	ns
t_{wh3}, t_{wl3}	–	31,32	Clock Pulse Duration, High, Low	10	8	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Refer to Switching Test Conditions section.

The Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of the Lattice High Density ispLSI Device. This GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections (see figure 3). The AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions. The AND array consists of 20 product terms which can produce the logical sum of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the 32 GLBs or inputs from the external I/O Cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes boolean logic reduction easier.

The PTSA takes the 20 product terms and allocates them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms (see figure 3). The output of any of these gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. If the users' main concern is speed, the PTSA can use a bypass circuit with four product terms to increase the performance of the cell (see figure 4). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an Exclusive OR Gate on the input. The Exclusive OR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K, or T-type flip-flop (see figure 5). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

Figure 3. GLB: Product Term Sharing Array

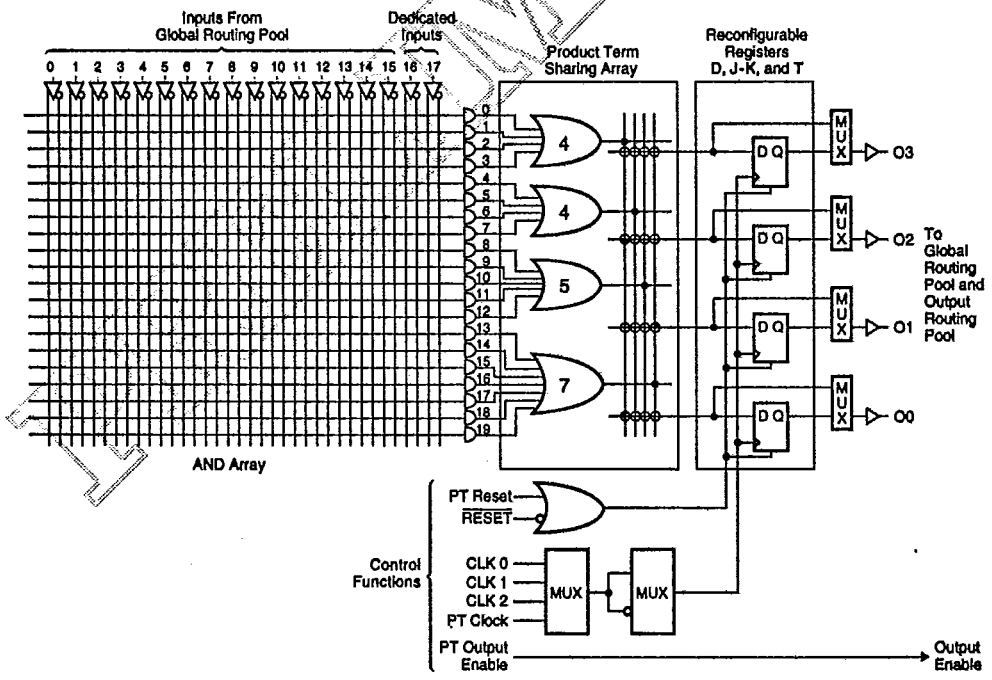


Figure 4. GLB: Four Product Term Bypass

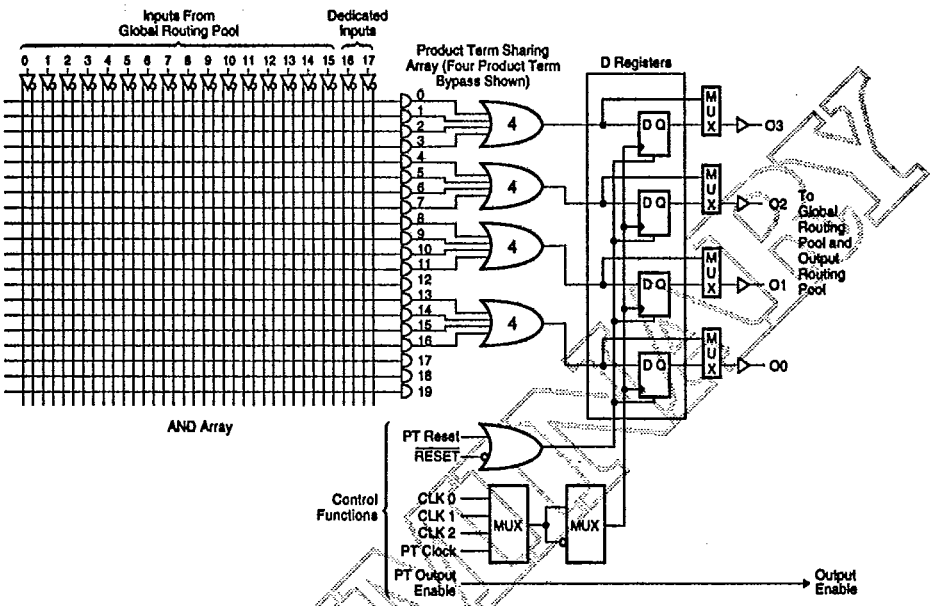
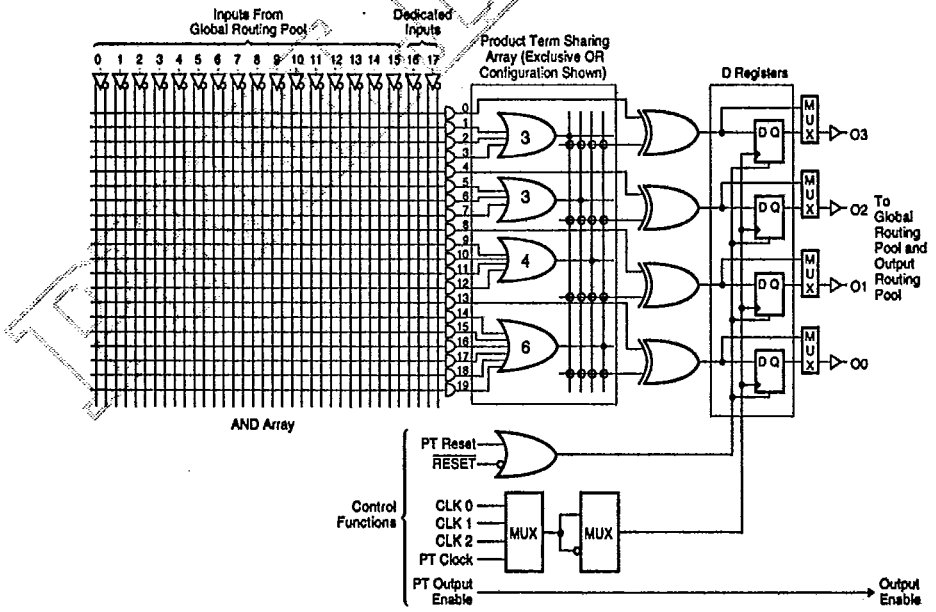


Figure 5. GLB: Exclusive OR Gate



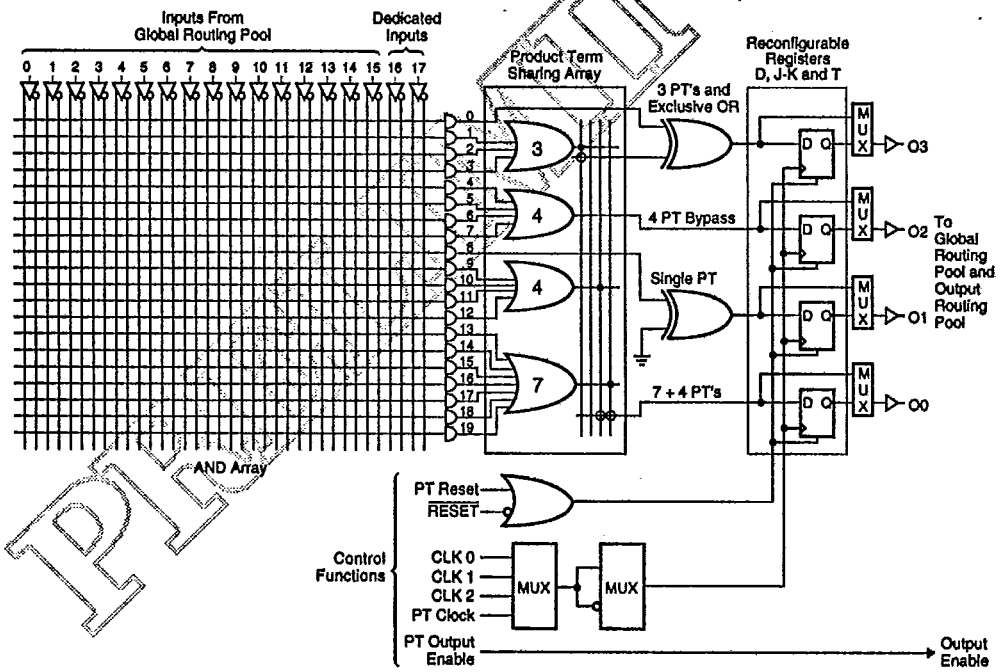
The Generic Logic Block (continued)

The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in figure 6, Output Three (O3) is configured using the XOR Gate and Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals which control the operation of the GLB are developed in the Control Function section. The clock for the registers can come from any of three sources developed in the Clock Distribution Network (See Clock Distribution Network Section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin or from a product term within the block. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the following table to determine which logic functions are affected.

There are additional features in a GLB which allow implementation of logic intensive functions. These features are accessible using the hard Macros from the software and require no intervention on the part of the user.

Figure 6. GLB: Various Logical Combinations



Product Term Sharing Matrix

Product Term #	Standard Configuration Output Number 3 2 1 0	Four Product Term Bypass Output Number 3 2 1 0	Single Product Term Output Number 3 2 1 0	XOR Function Output Number 3 3 2 2 1 1 0 0	Alternate Function
0	■ ■ ■ ■	■	■	■	
1	■ ■ ■ ■	■		■	
2	■ ■ ■ ■	■		■	
3	■ ■ ■ ■	■		■	
4	■ ■ ■ ■	■	■	■	
5	■ ■ ■ ■	■		■	
6	■ ■ ■ ■	■		■	
7	■ ■ ■ ■	■		■	
8	■ ■ ■ ■	■	■	■	
9	■ ■ ■ ■	■		■	
10	■ ■ ■ ■	■		■	
11	■ ■ ■ ■	■		■	
12	■ ■ ■ ■	■		■	■ CLK/Reset
13	■ ■ ■ ■	■	■	■	
14	■ ■ ■ ■	■		■	
15	■ ■ ■ ■	■		■	
16	■ ■ ■ ■	■		■	
17	■ ■ ■ ■	■		■	
18	■ ■ ■ ■	■		■	
19	■ ■ ■ ■	■		■	■ OE/Reset

This matrix shows how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the Exclusive OR (XOR) mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

The Megablock

The ispLSI family is structured into multiple "Megablocks". A Megablock consists of 8 GLBs, an Output Routing Pool (ORP) and 16 I/O Cells. Each of these will be explained in detail in the following sections. These elements are coupled together as shown in figure 7. This logic structure is referred to as the Megablock. The various members of the ispLSI family are created by combining from two to six Megablocks on a single device.

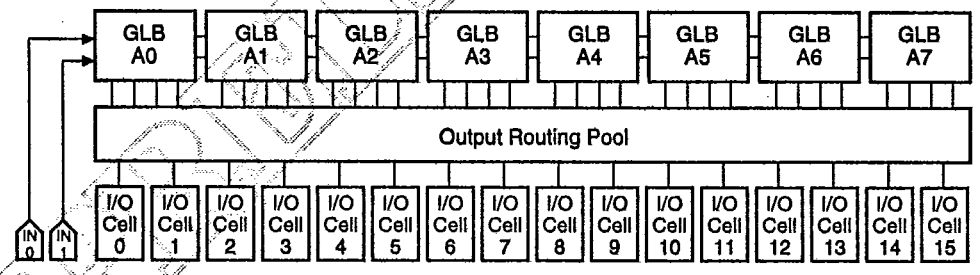
The Megablock shares two sets of resources. The eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-registered) inputs only and are automatically assigned by software. One Output Enable signal is generated within the Megablock and is common to all sixteen of the I/O Cells in the Megablock. The Output Enable signal can be generated using a product term in any of the eight GLBs within the Megablock (See the following section on the Output Enable Multiplexers).

Because of the shared logic within the Megablock, signals which share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

Megablocks in Each Device

DEVICE	MEGABLOCKS	GLBs	I/O CELLS
ispLSI 1016	2	16	32
ispLSI 1024	3	24	48
ispLSI 1032	4	32	64
ispLSI 1048	6	48	96

Figure 7. The Megablock

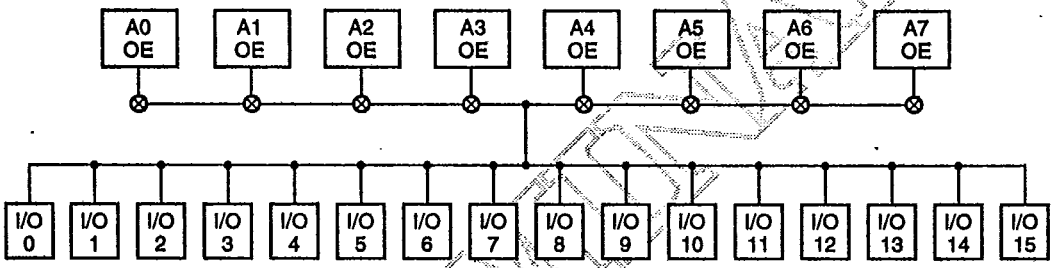


Note: The inputs from the I/O Cell are not shown in this figure, they go directly to the GRP.

The Output Enable Control

One Output Enable (OE) signal can be generated within each GLB using the OE Product Term 19. One of the eight OE signals from each GLB within a Megablock, is then routed to all of the I/O Cells within the Megablock (see figure 8). This OE signal can simultaneously control all of the 16 I/O cells which are used in 3-state mode. Individual I/O cells also have independent control for permanently enabling or disabling the output buffer (Refer to the I/O Cell Section). Only one OE signal is allowed per Megablock for 3-state operation. The advantage to this approach is that the OE signal can be generated in any GLB within the Megablock which happens to have an unused OE product term. This frees up the other OE product terms for use as logic.

Figure 8. Output Enable Controls



The Output Routing Pool

The Output Routing Pool (ORP) routes signals from the Generic Logic Block outputs to I/O Cells configured as outputs or bi-directional pins (see figure 9). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the programmable switch matrix in figure 9, it can be seen that a GLB output can be connected to one of four I/O Cells. Further flexibility is provided by using the PTSA, (Figures 3 through 7) which makes the GLB outputs completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see figure 10) further increase the flexibility of the device. The ORP bypass connect specific GLB outputs to specific I/O Cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

Figure 9. Output Routing Pool

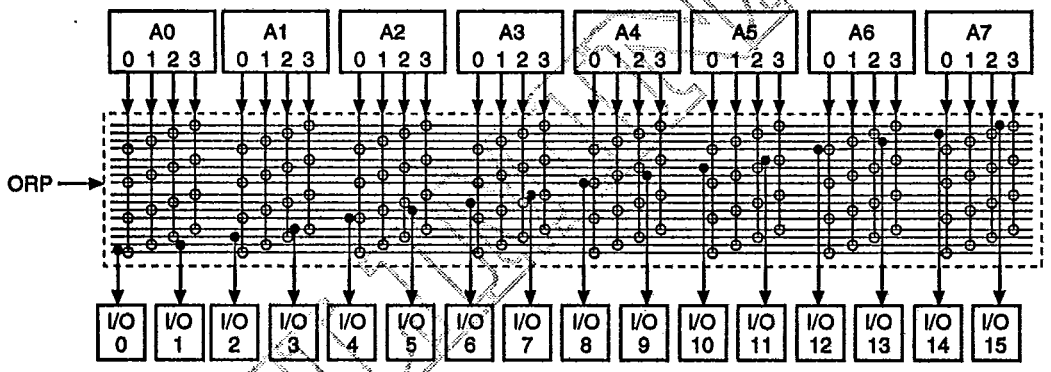
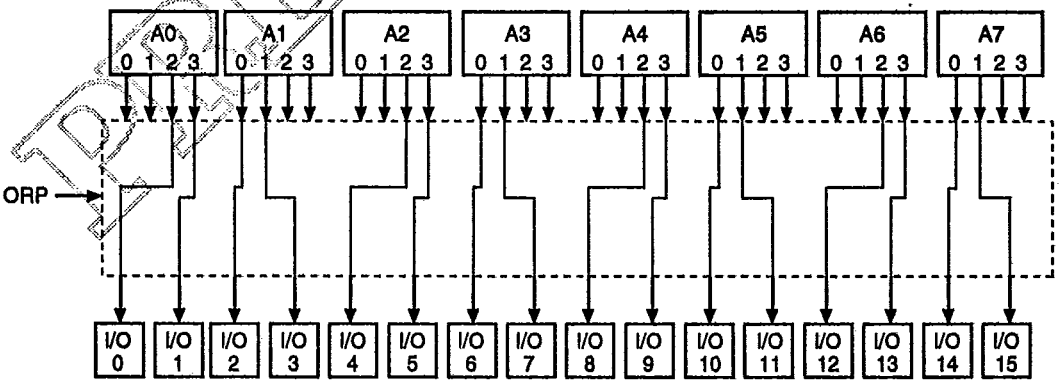


Figure 10. Output Routing Pool showing Bypass



I/O Cell

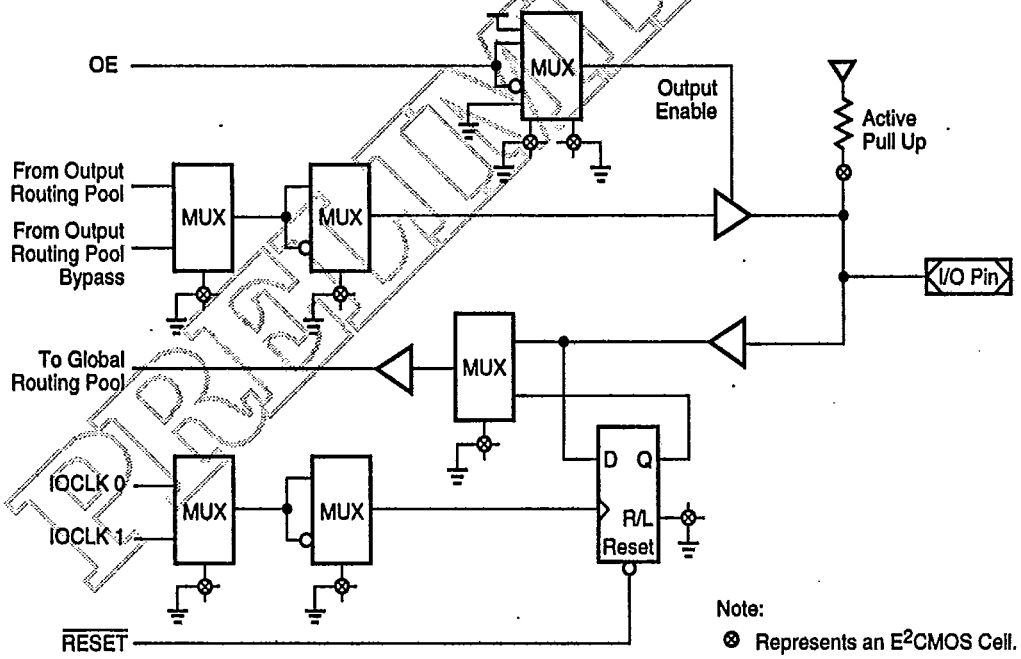
The I/O Cell (see figure 11) is used to route input, output or bidirectional signals connected to the I/O pin. The two logic inputs come from the ORP (see figure 7). One comes from the ORP, and the other comes from the faster ORP bypass. A pair of multiplexers select which signal will be used, and its polarity.

The OE signal comes from the Output Enable. As with the data path, a multiplexer selects the signal polarity. The Output Enable can be set to a logic high (Enabled) when a straight output pin is desired, or logic low (Disabled) when a straight input pin is needed. The Global Reset ($\overline{\text{RESET}}$) signal is driven by the active low chip reset pin. Each I/O Cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). These clock signals are generated by the Clock Distribution Network.

Using the multiplexers, the I/O Cell can be configured as an input, an output, a 3-stated output or a bidirectional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the in-coming data. Figure 12 illustrates some of the various I/O cell configurations possible.

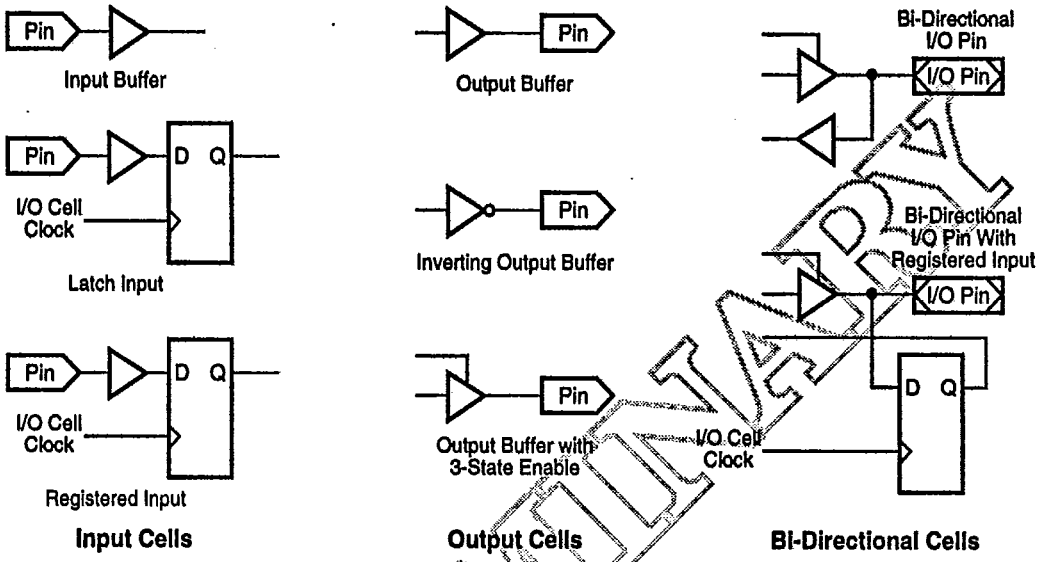
There is an Active Pullup resistor on the I/O pins which is automatically used when the pin is not connected. This prevents the pin from floating and inducing noise into the device or consuming additional power.

Figure 11. I/O Cell Architecture



Note:
⊗ Represents an E²CMOS Cell.

Figure 12. Example I/O Cell Configurations



2

Clock Distribution Network

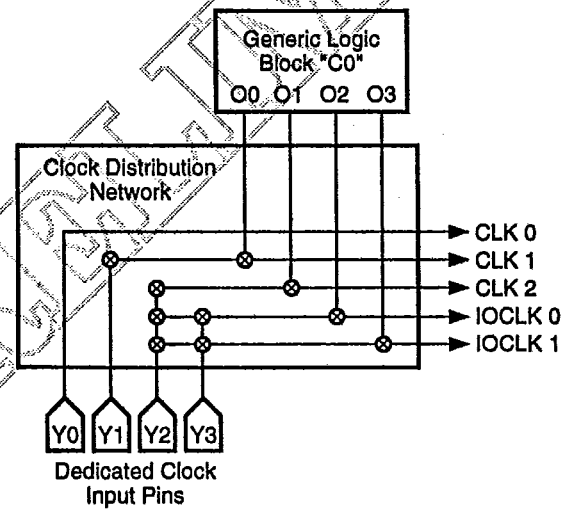
The Clock Distribution Network is shown in figure 13. It generates five global clock signals CLK 0, CLK 1, CLK 2 and IOCLK 0, IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 are used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O Cells in the device. There are four dedicated system clock pins (Y0, Y1, Y2, Y3) which can be directed to any GLB or any I/O Cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the 4 outputs of a dedicated clock GLB ("C0" for ispLSI 1032). These Clock GLB outputs can be used to create a user-defined internal clocking scheme.

Typically the clock GLB will be clocked using an external main clock pin Y0 connected to global clock signal CLK 0. The outputs of the clock GLB in turn will generate "divide by two" or "divide by four" phases of the CLK 0 which can be connected to CLK 1, CLK 2 or IOCLK 0, IOCLK 1 global clocks.

All GLBs also have the capability of generating their own asynchronous clocks using Product Term 12. CLK 0, CLK 1 and CLK 2 feed to their corresponding inputs on all the GLBs (see figure 3).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all 64 of the I/O cells and the user programs the I/O cell to use one of the two. When the Dedicated Clock Input pins Y2 or Y3 are used as one of the I/O Clocks, O2 or O3 from the Clock GLB (C0) cannot be used.

Figure 13. Clock Distribution Network



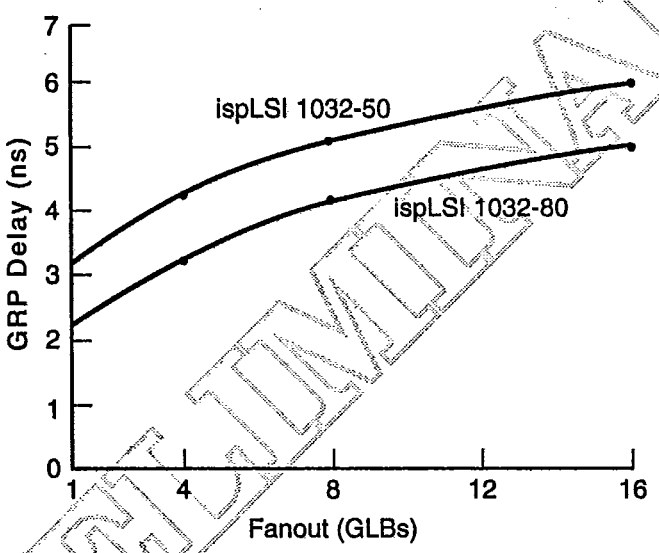
Note: Y3 pin should always be used first as an IOCLK 0 or IOCLK 1 before using Y2 pin.

Global Routing Pool

The Global Routing Pool (GRP) is a Lattice proprietary interconnect structure which offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the ispLSI device, the delays through the Global Routing Pool are both consistent and predictable. However, they are slightly affected by fanout. See the fanout delay graph (Figure 14).

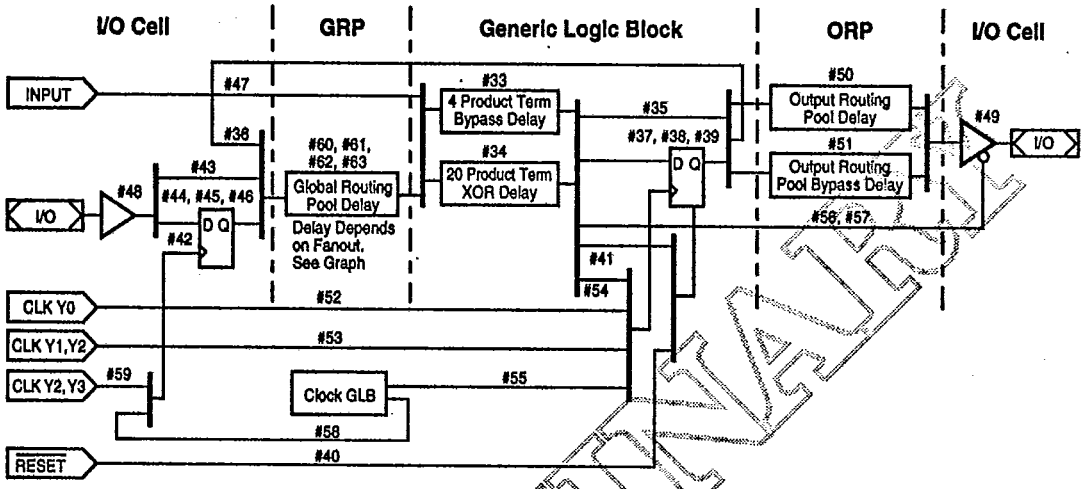
2

Figure 14. GRP Delay vs Fanout



Timing Model

Figure 15. ispLSI Timing Model



The task of determining the timing through the device is simple and straightforward. The device timing model is shown in figure 15. To determine the time that it takes for data to propagate through the device, simply determine the path the data is expected to follow, and add the various times. Some examples are shown for the critical timing paths used as Data Sheet parameters. Note that the internal timing parameters are given for reference only, and are not tested. (External timing parameters are tested and guaranteed on every device.)

t_{pd1}[1]	=	t_{ib}	+	t_{iobp}	+	t_{grp4}	+	t_{4pt}	+	t_{gbp}	+	t_{mxbp}	+	t_{ob}
#1	=	#48	+	#43	+	#60	+	#33	+	#35	+	#51	+	#49
15 ns	=	2	+	0	+	3	+	6	+	0	+	0	+	4
t_{pd2}[1]	=	t_{ib}	+	t_{iobp}	+	t_{grp4}	+	t_{xor20}	+	t_{gbp}	+	t_{mx}	+	t_{ob}
#2	=	#48	+	#43	+	#60	+	#34	+	#35	+	#50	+	#49
20 ns	=	2	+	0	+	3	+	7.5	+	0	+	1	+	4
f_{max}[1]	=	t_{gco}	+	t_{gfb}	+	t_{grp4}	+	t_{xor20}	+	t_{gsu}				
#11	=	#37	+	#36	+	#60	+	#34	+	#38				
1 / 14ns	=	2	+	0	+	3	+	7.5	+	0				
t_{su2}[1]	=	t_{ib}	+	t_{iobp}	+	t_{grp4}	+	t_{xor20}	-	t_{gy0}	-	t_{gsu}		
#14	=	#48	+	#43	+	#60	+	#34	-	#52	-	#38		
12 ns	=	2	+	0	+	3	+	7.5	-	4	-	0		
t_{co2}[1]	=	t_{gy0}	+	t_{gco}	+	t_{mx}	+	t_{ob}						
#4	=	#52	+	#37	+	#50	+	#49						
13 ns	=	4	+	2	+	1	+	4						

NOTE:
1. The internal delays are rounded and do not necessarily add up to the tested external delays.

Internal Timing Model Parameters are not tested and are for reference only

Generic Logic Block (GLB)[1]

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
t_{4pt}	33	4 Product Term Delay	–	6	ns
t_{xor20}	34	20 Product Term Delay	–	7.5	ns
t_{gbp}	35	GLB Register By-Pass Delay	–	0	ns
t_{gfb}	36	GLB Feedback Delay	–	0	ns
t_{gco}	37	GLB Clock to Output Delay	–	2	ns
t_{gsu}	38	GLB Setup Time before Clock	0	–	ns
t_{gh}	39	GLB Hold Time after Clock	2	–	ns

Reset Delays

PARAMETER	#	DESCRIPTION	MIN.	MAX.	UNITS
t_{ggr}	40	GLB Global Reset Delay	–	12	ns
t_{gar}	41	GLB Asynchronous Reset Delay	–	9	ns

Input/Output Cell (I/O Cell)

PARAMETER	#	DESCRIPTION	MIN.	MAX.	UNITS
t_{iat}	42	I/O Cell Latch Delay	–	1	ns
t_{iobp}	43	I/O Cell Register Latch By-Pass Delay	–	0	ns
t_{iosu}	44	I/O Cell Setup Time before Clock/LE	0	–	ns
t_{ioh}	45	I/O Cell Hold Time after Clock/LE	1	–	ns
t_{ioco}	46	I/O Cell Clock/LE to Output Delay	–	1	ns

Input and Output Delays

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
t_{din}	47	Dedicated Input Buffer Delay	–	6	ns
t_{ib}	48	Input Delay for I/O Buffer	–	2	ns
t_{ob}	49	Output Buffer Delay	–	4	ns
t_{mx}	50	Output ORP Delay	–	1	ns
t_{mxbp}	51	Output ORP Bypass Delay	–	0	ns

(Note: Parameter Numbers refer to the timing paths used in the Timing Model Diagram.)

Switching Characteristics — ispLSI 1032-80

Internal AC Characteristics and Conditions are not tested and are for reference only

Clock and Enable Delays, GLB and I/O Cell

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
tgy0	52	Clock Delay, Y0 to GLB	–	4	ns
tgy1/2	53	Clock Delay, Y1 or Y2 to GLB	–	4	ns
tgpt	54	Clock Delay, PT Clk to GLB	–	5	ns
tgcp	55	Clock Delay, Clk GLB to GLB	–	4	ns
tgen	56	Enable Delay, GLB to I/O Cell	–	7	ns
tgdis	57	Disable Delay, GLB to I/O Cell	–	7	ns
tiocp	58	Clock Delay, Clk GLB to I/O Cell	–	4	ns
tioy2/3	59	Clock Delay, Y2 or Y3 to I/O Cell	–	4	ns

GRP Delays

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
tgrp4	60	GRP Delay, Fanout 4	–	3	ns
tgrp8	61	GRP Delay, Fanout 8	–	4	ns
tgrp16	62	GRP Delay, Fanout 16	–	5	ns
tgrp32	63	GRP Delay, Fanout 32	–	8	ns

(Note: Parameter Numbers refer to the timing paths used in the Timing Model Diagram.)

Internal Timing Model Parameters are not tested and are for reference only

Generic Logic Block (GLB)[1]

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
t_{4pt}	33	4 Product Term Delay	–	7	ns
t_{xor20}	34	20 Product Term Delay	–	10	ns
t_{gbp}	35	GLB Register By-Pass Delay	–	0	ns
t_{gfb}	36	GLB Feedback Delay	–	0	ns
t_{gco}	37	GLB Clock to Output Delay	–	3	ns
t_{gsu}	38	GLB Setup Time before Clock	2	–	ns
t_{gh}	39	GLB Hold Time after Clock	4	–	ns

Reset Delays

PARAMETER	#	DESCRIPTION	MIN.	MAX.	UNITS
t_{ggr}	40	GLB Global Reset Delay	–	14	ns
t_{gar}	41	GLB Asynchronous Reset Delay	–	10	ns

Input/Output Cell (I/O Cell)

PARAMETER	#	DESCRIPTION	MIN.	MAX.	UNITS
t_{iat}	42	I/O Cell Latch Delay	–	2	ns
t_{iobp}	43	I/O Cell Register Latch By-Pass Delay	–	0	ns
t_{iosu}	44	I/O Cell Setup Time before Clock/LE	0	–	ns
t_{ioh}	45	I/O Cell Hold Time after Clock/LE	2	–	ns
t_{ioco}	46	I/O Cell Clock/LE to Output Delay	–	2	ns

Input and Output Delays

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
t_{din}	47	Dedicated Input Buffer Delay	–	7	ns
t_{ib}	48	Input Delay for I/O Buffer	–	3	ns
t_{ob}	49	Output Buffer Delay	–	5	ns
t_{mx}	50	Output ORP Delay	–	2	ns
t_{mxbp}	51	Output ORP Bypass Delay	–	0	ns

(Note: Parameter Numbers refer to the timing paths used in the Timing Model Diagram.)

Internal AC Characteristics and Conditions are not tested and are for reference only

Clock and Enable Delays, GLB and I/O Cell

PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
tgy0	52	Clock Delay, Y0 to GLB	–	6	ns
tgy1/2	53	Clock Delay, Y1 or Y2 to GLB	–	6	ns
tgpt	54	Clock Delay, PT Clk to GLB	–	7	ns
tgcp	55	Clock Delay, Clk GLB to GLB	–	5	ns
tgen	56	Enable Delay, GLB to I/O Cell	–	9	ns
tgdis	57	Disable Delay, GLB to I/O Cell	–	9	ns
tiocp	58	Clock Delay, Clk GLB to I/O Cell	–	5	ns
tioy2/3	59	Clock Delay, Y2 or Y3 to I/O Cell	–	5	ns

GRP Delays

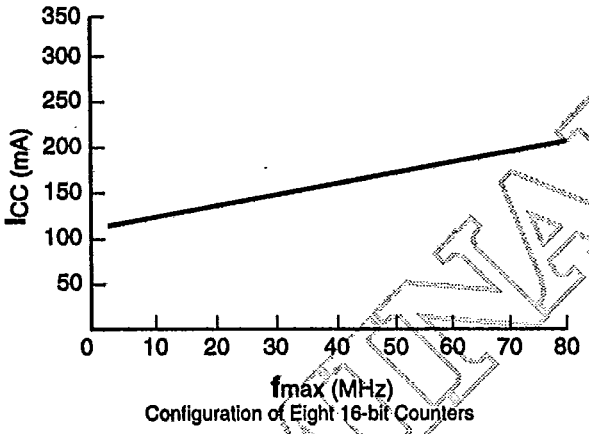
PARAMETER	#	DESCRIPTION	MIN.	MAX	UNITS
tgrp4	60	GRP Delay, Fanout 4	–	4	ns
tgrp8	61	GRP Delay, Fanout 8	–	6	ns
tgrp16	62	GRP Delay, Fanout 16	–	7	ns
tgrp32	63	GRP Delay, Fanout 32	–	10	ns

(Note: Parameter Numbers refer to the timing paths used in the Timing Model Diagram.)

Power Consumption

Power Consumption in the ispLSI 1032 device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 16 shows the relationship between power and operating speed.

Figure 16. Typical Device Power Consumption vs fmax



Security Cell

A security cell is provided in the ispLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

ispLSI devices are programmed using a Lattice-approved Device Programmer, available from a number of third party manufacturers or in-system using Lattice programming algorithms. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user.

Latch-up Protection

ispLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latchup. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

In-System Programmability

The ispLSI devices are the in-system programmable version of the Lattice high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, the programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable ($\overline{ispEN}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 17 illustrates the block diagram of one possible scheme of the programming interface for the isp devices. For details on the operation of the internal state machine and programming of the device please refer to the In-system programming application note.

Figure 17. Isp Programming Interface

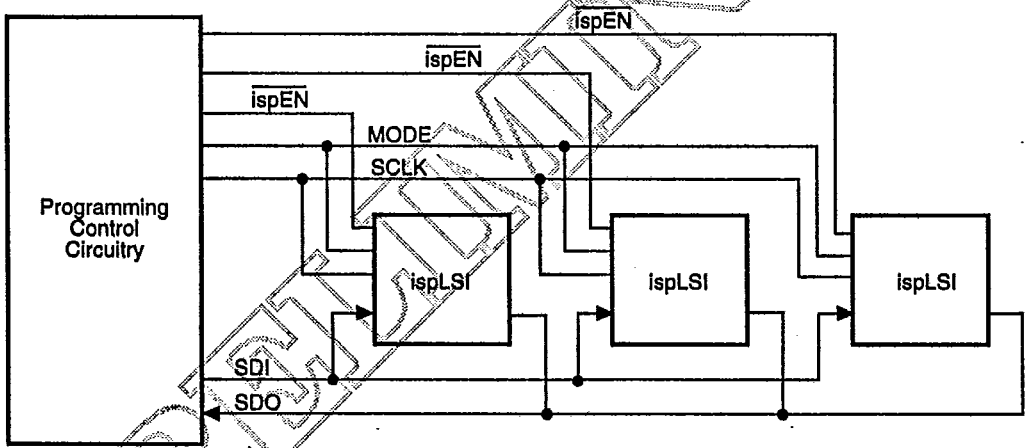
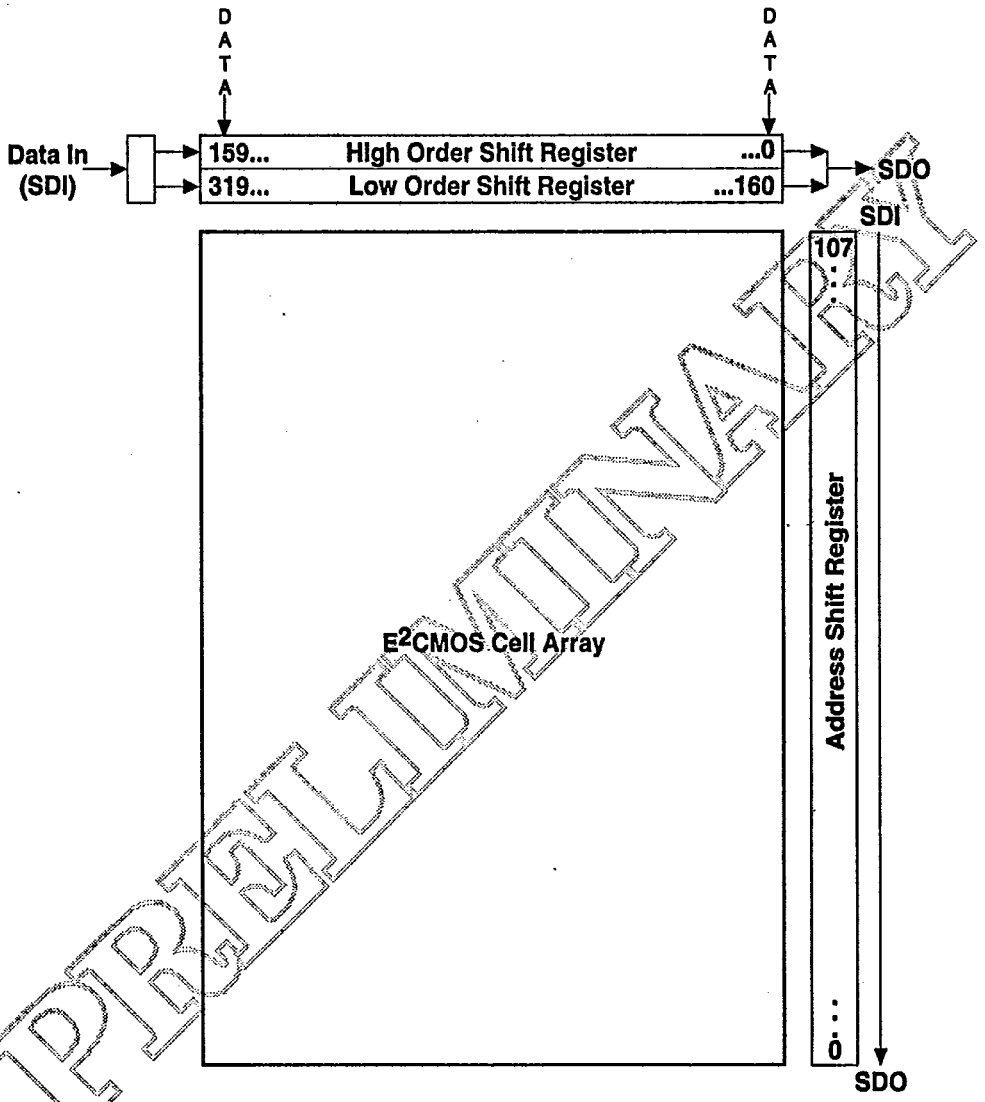


Figure 18. ispLSI Device & Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5	5.25	V
I_{CCP}	Programming Supply Current ispEN		–	50	100	mA
V_{IHP}	Input Voltage High		2.0	–	V_{CCP}	V
V_{ILP}	Input Vopltage Low		0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Volatge High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} =5 mA	0	–	0.5	V
td	Pulse Sequence Delay		1	5	10	µs
tisp	$\overline{ispEN}$ to Output 3-State		–	1	10	µs
tsu	Setup Time		.1	.5	–	µs
th	Hold Time		.1	.5	–	µs
tclk	Clock Pulse Width		0.5	1	–	µs
tpwv	Verify Pulse Width		20	30	–	µs
tpwp	Programming Pulse Width		40	–	100	ms
tbew	Bulk Erase Pulse Width		200	–	–	ms
trst	Reset Time From Valid V_{CCP}		45	–	–	µs

Figure 19. Timing Waveform for Isp Operation

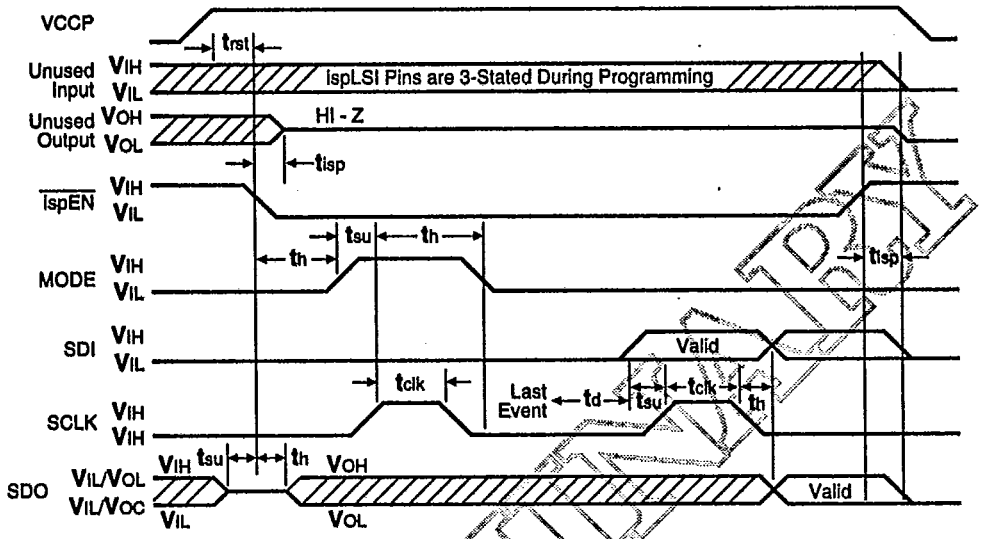
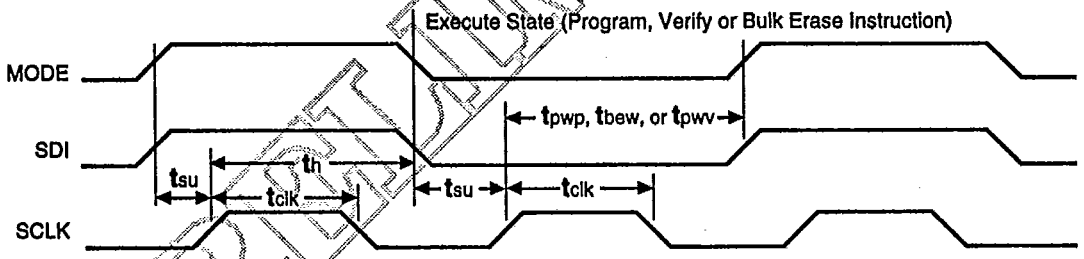
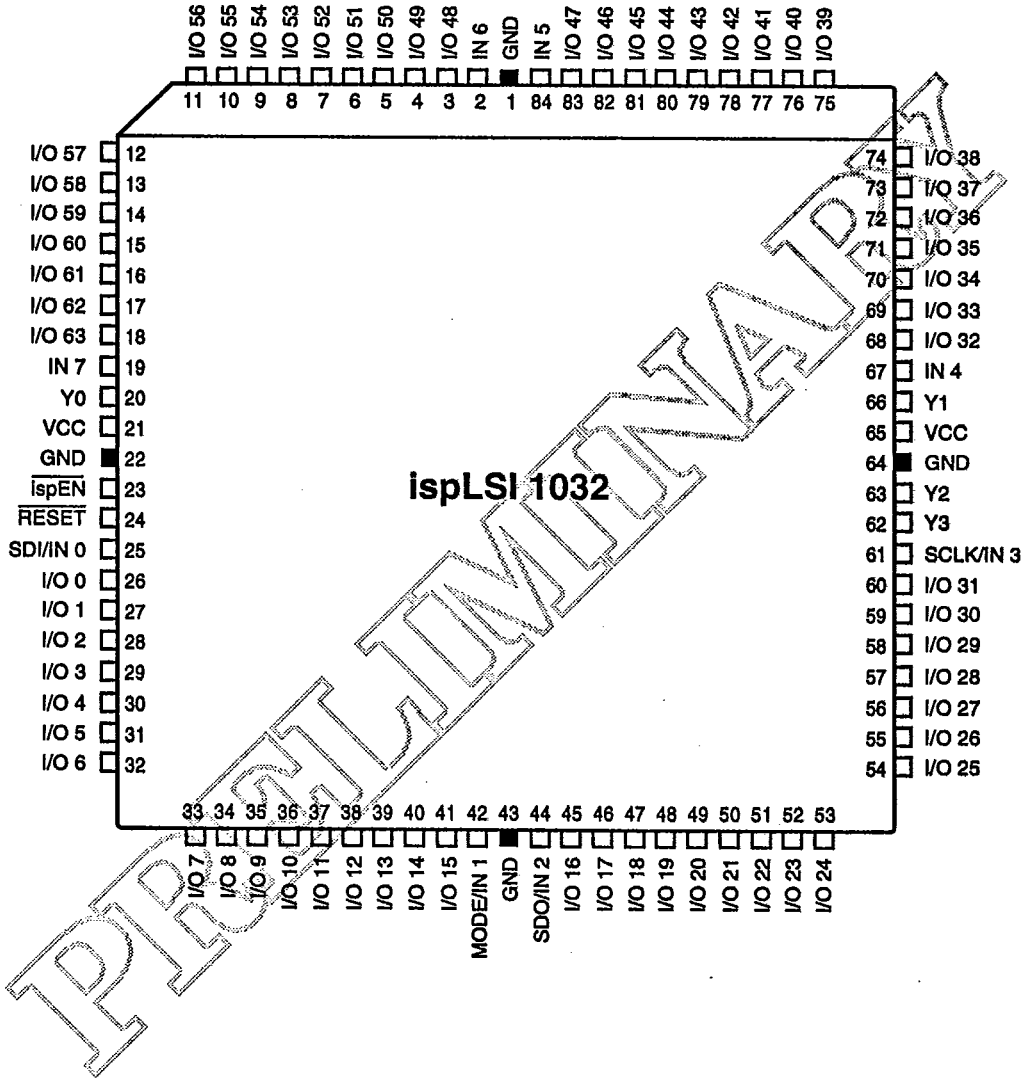


Figure 20. Program, Verify & Bulk Erase Waveform

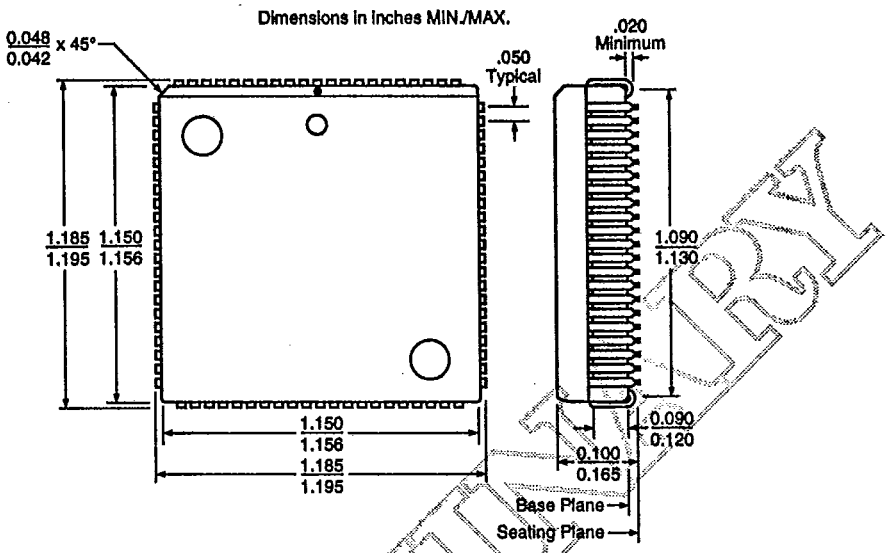


Pin Configuration

ispLSI 1032 PLCC Pinout Diagram



84-Pin PLCC



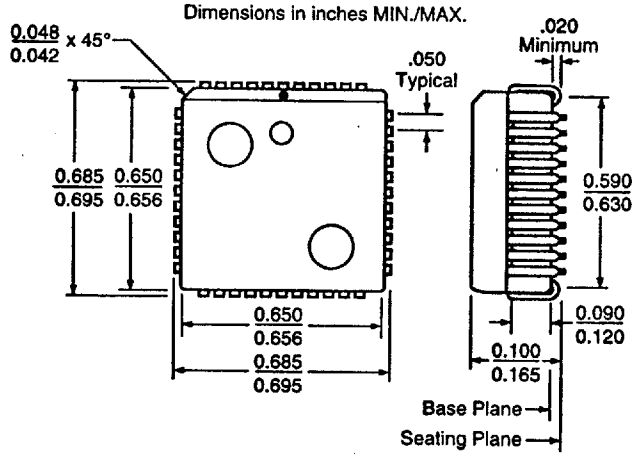
2

Package Diagrams

T-90-20

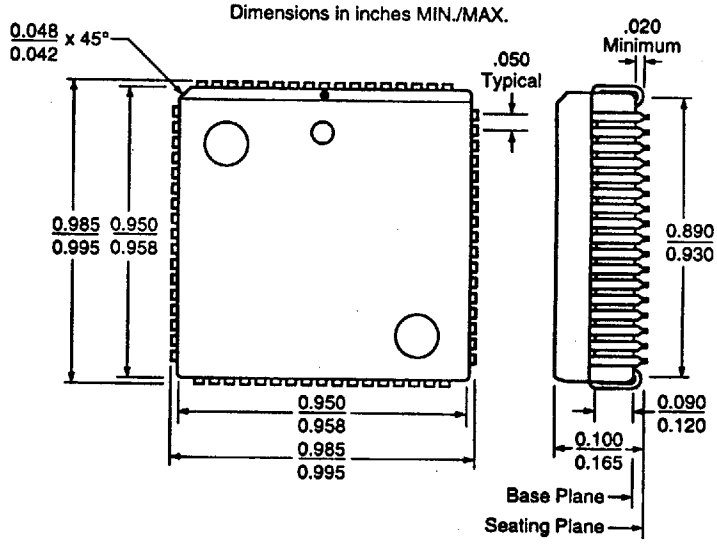
44-Pin PLCC

Dimensions in inches MIN./MAX.



68-Pin PLCC

Dimensions in inches MIN./MAX.

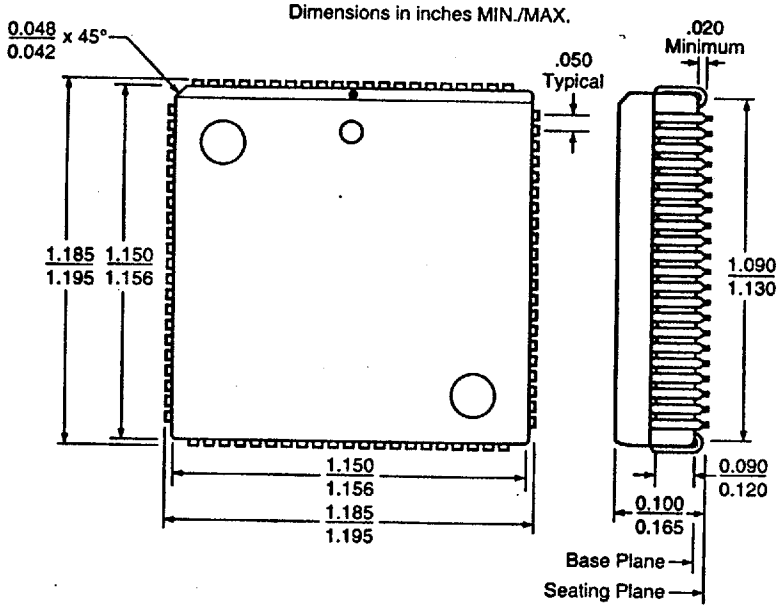


Package Diagrams

T-90-20

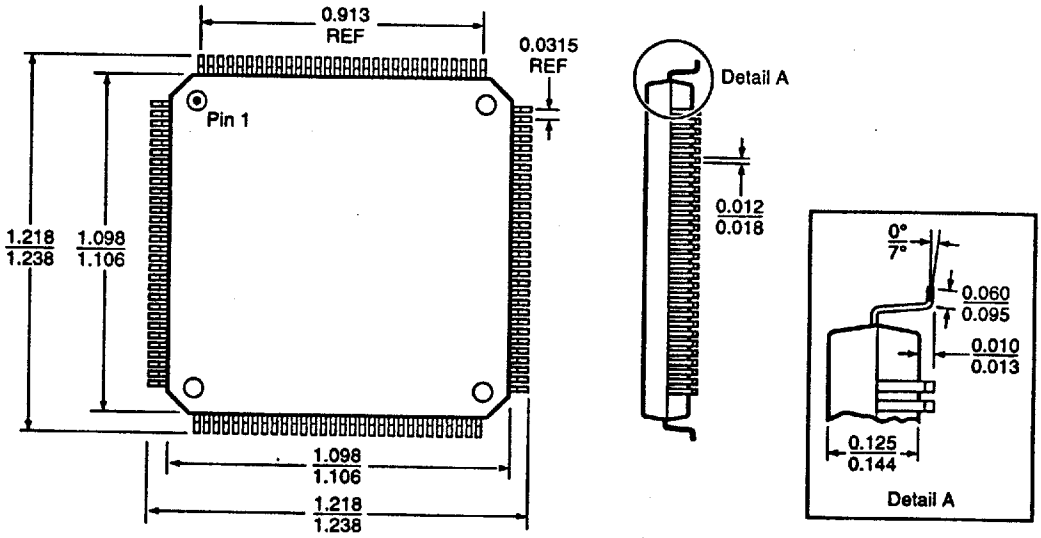
84-Pin PLCC

Dimensions in inches MIN./MAX.



120-Pin PQFP

Dimensions in inches MIN./MAX.



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