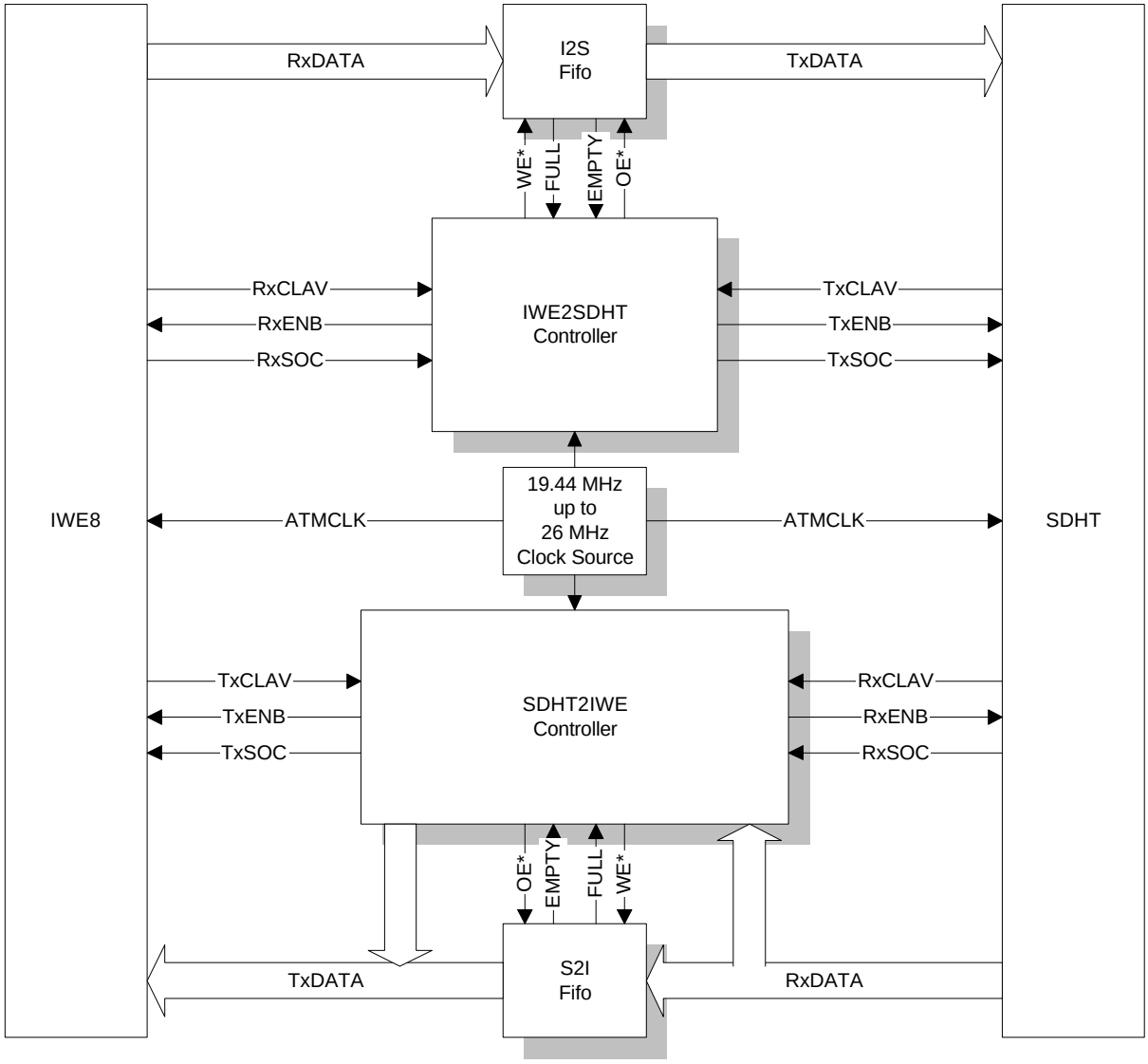
FJS 01/28/97

Block diagram and functional description of UTOPIA master to connect two or more PHY chips back-to-back



Since both PHYs operate in UTOPIA slave mode, additional logic (shadowed in the above block diagram) has to perform the master function. This comprises

- Clock supply to both PHYs,
- Operation of ENB lines,
- Fifo control,
- Generation of Port Number for IWE8 transmit direction from VPI/VCI fields.

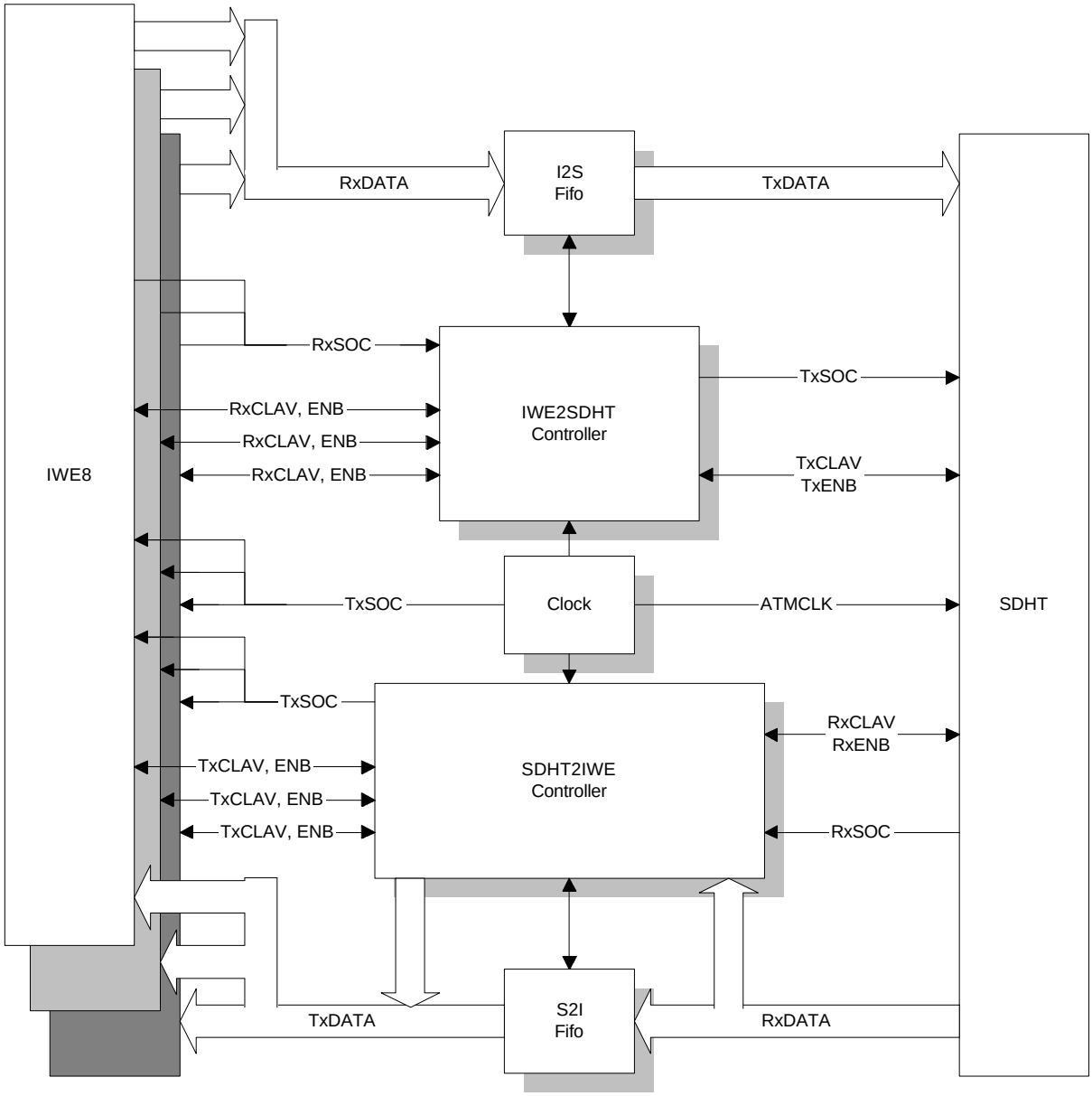
Clock:
A TTL/CMOS clock anywhere in the range of 19.44 MHz (to ensure 155.52 Mbit/s throughput) up to roughly 26 MHz is required.

Enable lines:
Main task of the Controllers shown in the block diagram is to listen to the RxCLAV line (to see if there is a cell ready to transfer) and to the TxCLAV line (to see if there is enough space to transfer the cell) and drive RxENB and TxENB accordingly. The datarates of the PHYs are decoupled by a fifo. In other words, as soon as RxCLAV is asserted, the cell can be written to the fifo, and as soon as TxCLAV is asserted, the cell can be read out again.

Fifo control:
The write enable and output enable lines of the fifos have to be driven in order to clock cells in and out. These signals are derived from ATMCLK, CLAV, ENB and SOC signals. In the direction towards the IWE8 there is a special case to be considered when generating the fifo control signals, see next paragraph.

PN generation:
The current IWE8 needs the port number (1 out of 8 E1/T1 framer interfaces) in the fifth octet (‘HEC octet’) of each cell. For this reason the SDHT2IWE Controller has to snoop the incoming RxDATA lines and read the VPI/VCI fields. The port number has to be calculated from these values and has to be put on the TxDATA lines during the fifth octet cycle in order to overwrite the HEC. This implies that fifo writing as well as fifo reading is paused during the fifth octet cycle.

Modifications that enable multiple IWEs to be connected to an SDHT:



In this case there is are two additional tasks for the control logic:

- Demultiplexing of cell stream towards several IWEs
- Arbitration of cell streams from several IWEs

Demultiplexing:
Similar to the port number generation the 'chip number' of the destination IWE has to be calculated from the VPI/VCI values. This chip number determines which CLAV/ENB pair is going to handle that cell.

Arbitration:
This is a simple round-robin polling of the RxCLAV lines of all IWEs.