

LM301A, LM201A

Non Compensated Single Operational Amplifiers

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/ μ s can be obtained.

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics

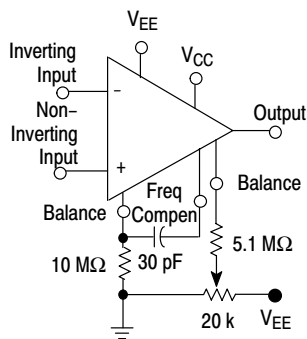
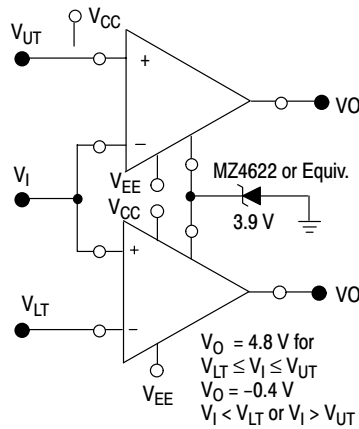


Figure 1. Standard Compensation and Offset Balancing Circuit



(Pins Not Shown Are Not Connected)

Figure 2. Double-Ended Limit Detector

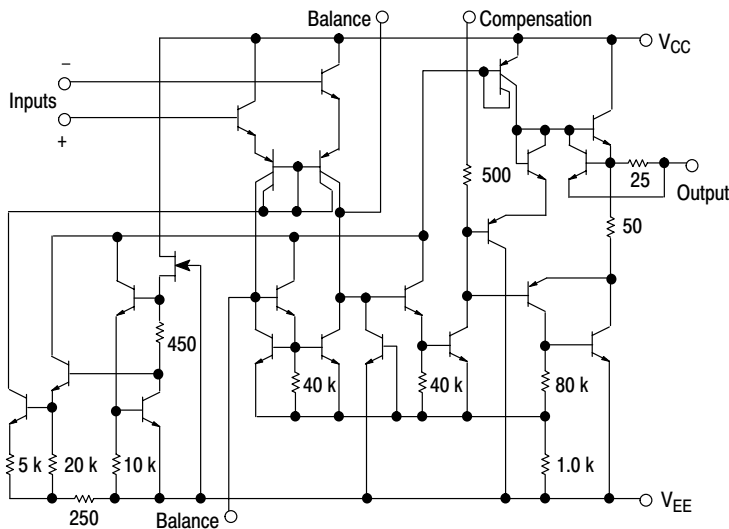


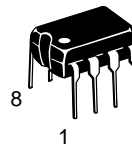
Figure 3. Representative Circuit Schematic



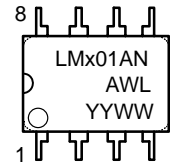
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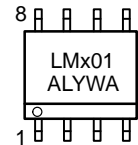
MARKING DIAGRAMS



PDIP-8
N SUFFIX
CASE 626

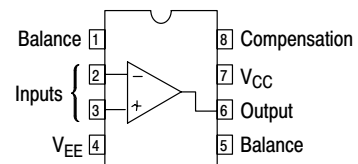


SO-8
D SUFFIX
CASE 751



x = 2 or 3
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
LM301AD	SO-8	98 Units/Rail
LM301ADR2	SO-8	2500 Tape & Reel
LM301AN	PDIP-8	50 Units/Rail
LM201AD	SO-8	98 Units/Rail
LM201ADR2	SO-8	2500 Tape & Reel
LM201AN	PDIP-8	50 Units/Rail

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MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		LM201A	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	±22	±18	Vdc
Input Differential Voltage	V_{ID}	← ±30 →		V
Input Common Mode Range (Note 1)	V_{ICR}	← ±15 →		V
Output Short Circuit Duration	t_{SC}	← Continuous →		
Power Dissipation (Package Limitation) Plastic Dual-In-Line Package Derate above $T_A = +25^\circ\text{C}$	P_D	625 5.0	625 5.0	mW mW/°C
Operating Ambient Temperature Range	T_A	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	← -65 to +150 →		°C

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristic	Symbol	LM201A			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 50 \text{ k}\Omega$)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	M Ω
Supply Current $V_{CC}/V_{EE} = \pm 20 \text{ V}$ $V_{CC}/V_{EE} = \pm 15 \text{ V}$	I_{CC}, I_{EE}	–	1.8	3.0	–	–	–	mA
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}, R_L > 2.0 \text{ k}\Omega$)	A_V	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Input Offset Voltage ($R_S \leq 50 \text{ k}\Omega$)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Avg Temperature Coefficient of Input Offset Voltage (Note 2) $T_A(\text{min}) \leq T_A \leq T_A(\text{max})$	$\Delta V_{IO}/\Delta T$	–	3.0	15	–	6.0	30	$\mu\text{V}/^\circ\text{C}$
Avg Temperature Coefficient of Input Offset Current (Note 2) $+25^\circ\text{C} \leq T_A \leq T_A(\text{max})$ $T_A(\text{min}) \leq T_A \leq 25^\circ\text{C}$	$\Delta I_{IO}/\Delta T$	–	0.01 0.02	0.1 0.2	–	0.01 0.02	0.3 0.6	nA/°C
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain ($V_{CC}/V_{EE} = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}, R_L > 2.0 \text{ k}\Omega$)	A_{VOL}	25	–	–	15	–	–	V/mV
Input Voltage Range $V_{CC}/V_{EE} = \pm 20 \text{ V}$ $V_{CC}/V_{EE} = \pm 15 \text{ V}$	V_{ICR}	–15 –	– –	+15 –	– –12	– –	– +12	V
Common Mode Rejection ($R_S \leq 50 \text{ k}\Omega$)	CMR	80	96	–	70	90	–	dB
Supply Voltage Rejection ($R_S \leq 50 \text{ k}\Omega$)	PSR	80	96	–	70	96	–	dB
Output Voltage Swing ($V_{CC}/V_{EE} = \pm 15 \text{ V}, R_L = \pm 10 \text{ k}\Omega, R_L > 2.0 \text{ k}\Omega$)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V
Supply Currents ($T_A = T_A(\text{max}), V_{CC}/V_{EE} = \pm 20 \text{ V}$)	I_{CC}, I_{EE}	–	1.2	2.5	–	–	–	mA

- For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
- Guaranteed by design.

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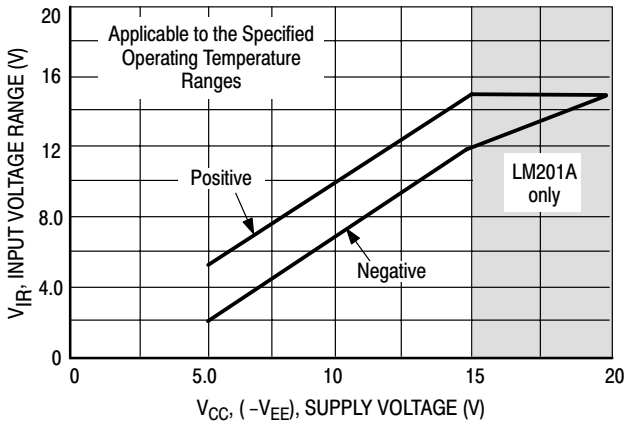


Figure 4. Minimum Input Voltage Range

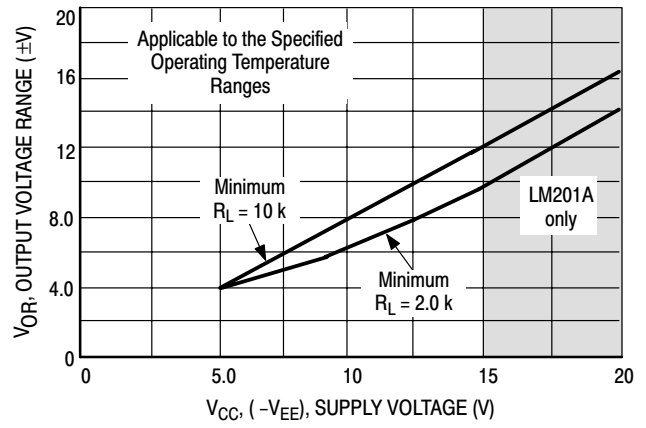


Figure 5. Minimum Output Voltage Swing

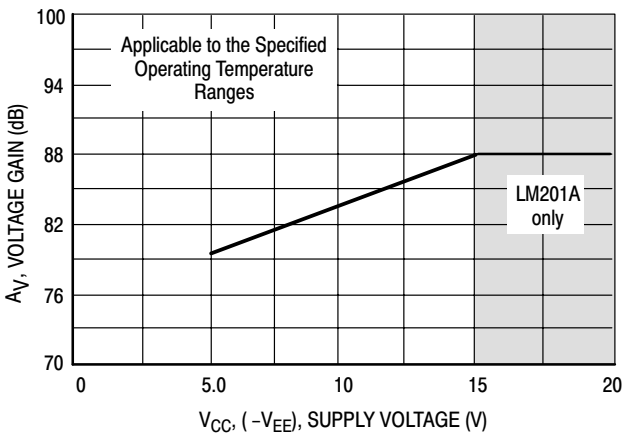


Figure 6. Minimum Voltage Gain

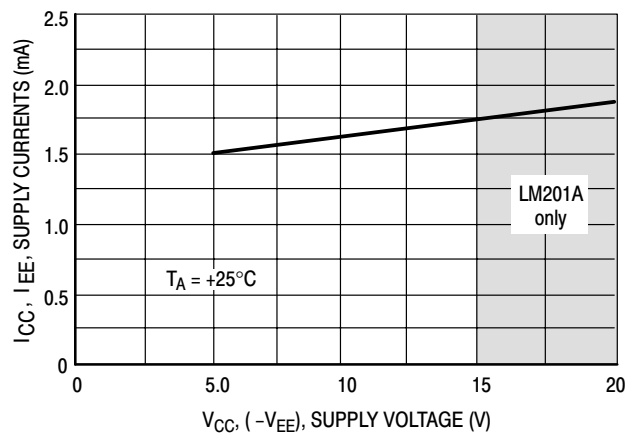


Figure 7. Typical Supply Currents

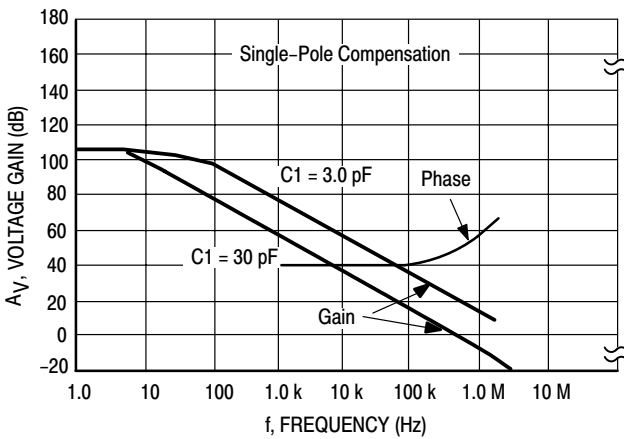


Figure 8. Open Loop Frequency Response

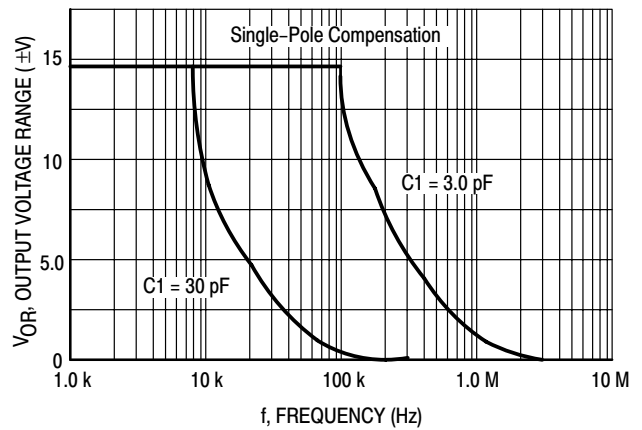


Figure 9. Large Signal Frequency Response

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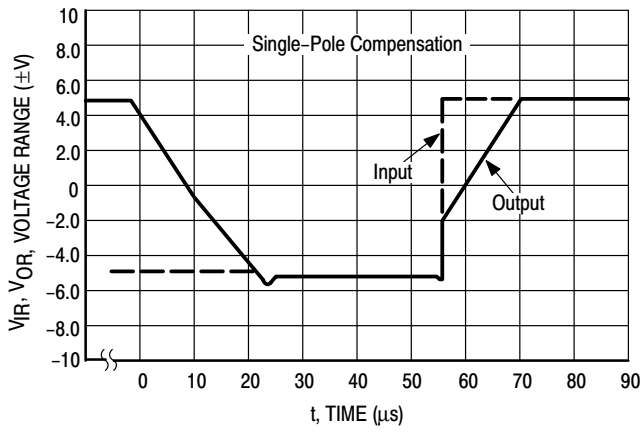


Figure 10. Voltage Follower Pulse Response

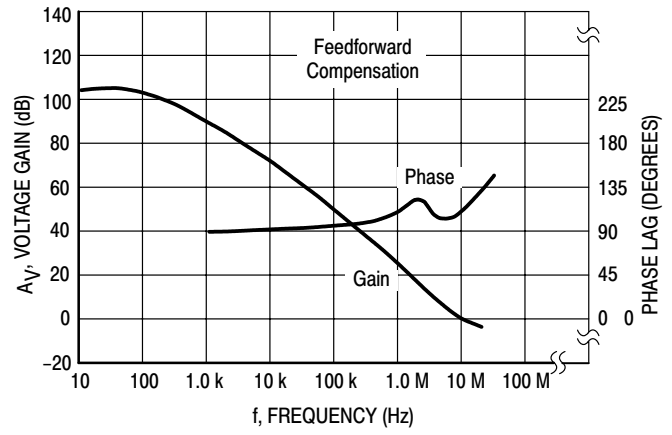


Figure 11. Open Loop Frequency Response

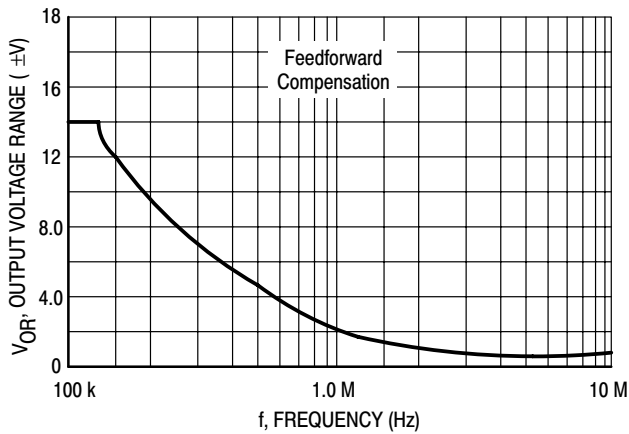


Figure 12. Large Signal Frequency Response

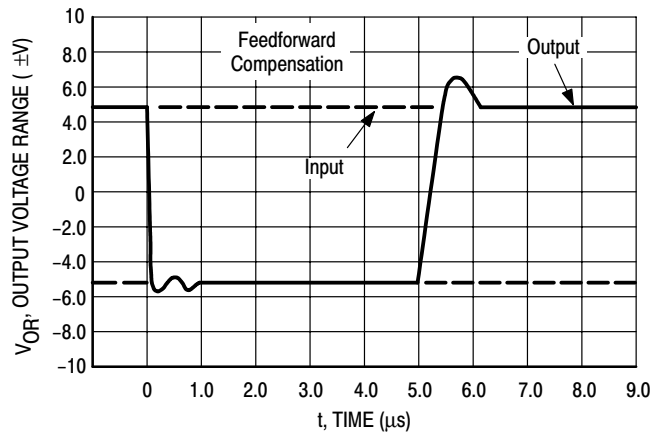


Figure 13. Inverter Pulse Response

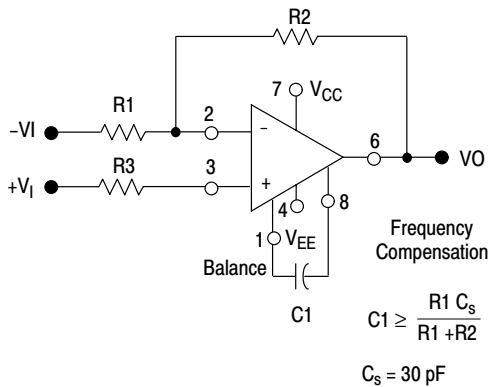


Figure 14. Single-Pole Compensation

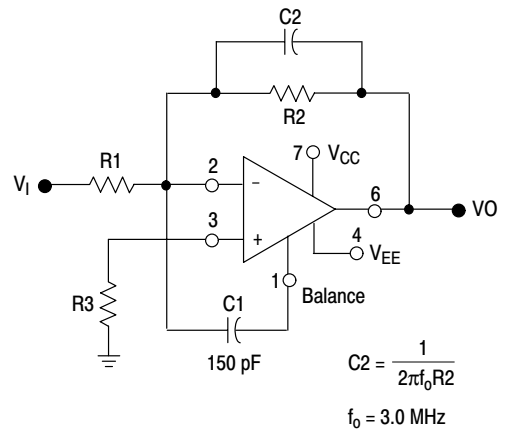
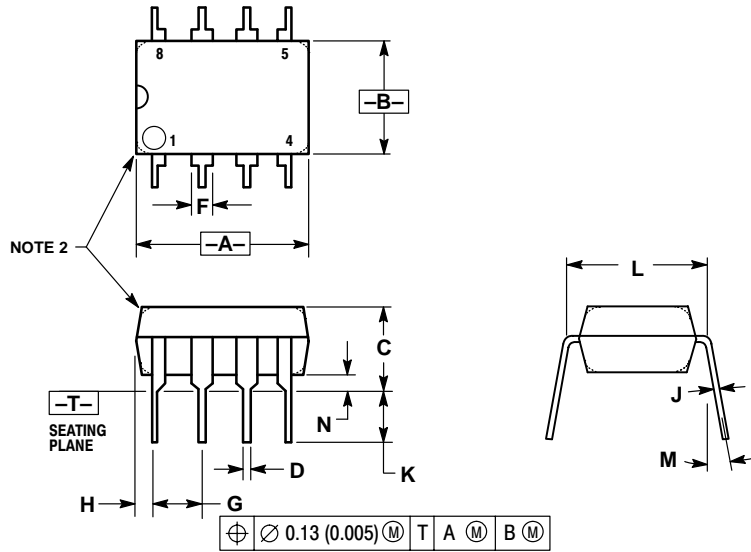


Figure 15. Feedforward Compensation

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PACKAGE DIMENSIONS

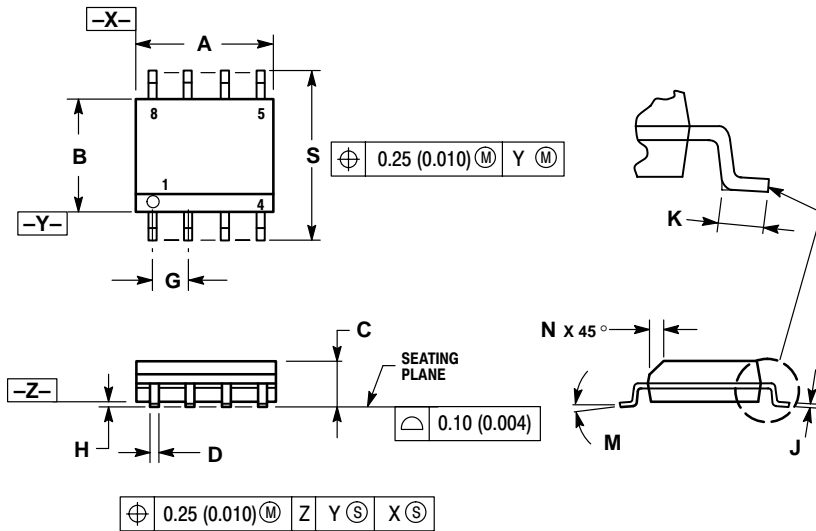
PDIP-8
N SUFFIX
CASE 626-05
ISSUE L



- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO-8
D SUFFIX
CASE 751-07
ISSUE W




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

Notes

Notes

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