GENERAL DESCRIPTION

The M901-01 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. The output clock (e.g., frequencies of 622.08, 311.04, 155.52, or 77.76MHz with the **M901-01-622.0800**) is provided from a LVPECL clock output pair. Output frequency accuracy is assured by phase-locking the VCSO to an external input reference frequency (e.g., frequencies of 19.44, 38.80, 77.76, or 155.52MHz with the **M901-01-622.0800**). The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a packaged crystal oscillator.

FEATURES

- **Output clock frequency from 62MHz to 700MHz (Consult factory for VCSO frequency availability)**
- **Low jitter 0.5ps rms, typ. (12kHz-20MHz @622.08MHz)**
- **Ideal for OC-48 (STM-16), Gigabit Ethernet clock ref**
- **Integrated SAW (surface acoustic wave) delay line**
- **XTAL or LVCMOS reference input**
- **LVPECL output**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

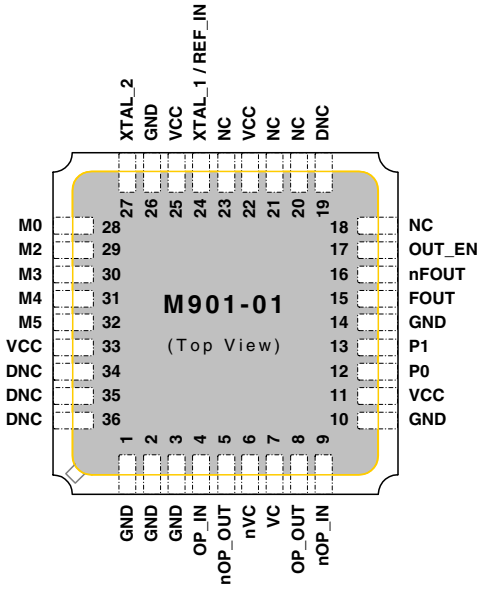


Figure 1: Pin Assignment

Example Output Frequency Configurations *

Ref Clock Freq (MHz)	VCSO Freq [1] (MHz)	Output Freq (MHz)	Application
19.44	622.08	622.08	OC-12/48 (STM-4/16)
		155.52	
25.00	625.00	156.25	10GbE

Table 1: Example Output Frequency Configurations *

Note1: Specify VCSO center frequency at time of order

BLOCK DIAGRAM

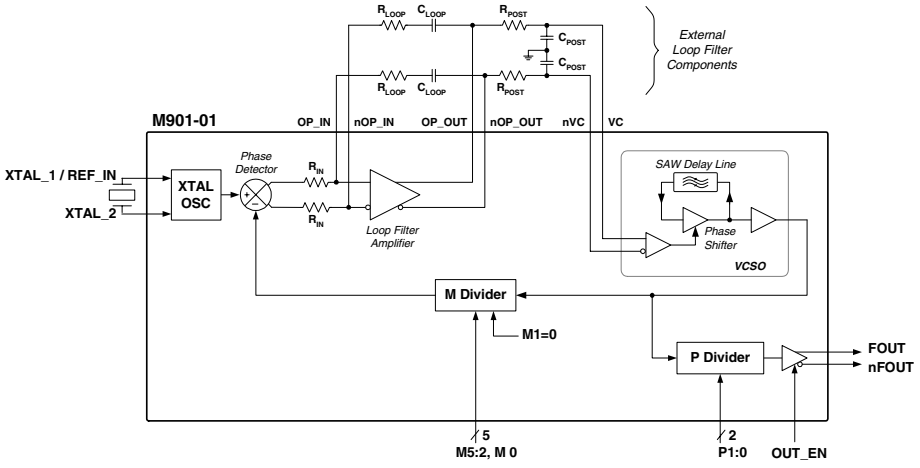


Figure 2: Block Diagram

Note *: Other frequencies available. See "Ordering Information" on pg. 8.

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4, External Loop Filter, on pg. 4.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 22, 25, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	P0 P1	Input	Internal pull-down resistor[1]	P divider (output divider) inputs P1:0. LVCMOS/LVTTL. See 4, Pin Selection of P Divider Using P1:0 Pins, on pg. 2.
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.
17	OUT_EN	Input	Internal pull-down resistor[1]	Output Enable: Logic 1 resets M and P dividers and forces FOUT to LOW and nFOUT to HIGH. Logic 0 enables the outputs. LVCMOS/LVTTL.
18, 20, 21, 23	NC			No connection.
24	XTAL_1 / REF_IN	Input		External crystal connection. Also accepts LVCMOS/LVTTL compatible clock source.
27	XTAL_2	Input		External crystal connection. Leave unconnected when driving pin 27 with external clock reference.
28 29 30 31	M0 M2 M3 M4	Input	Internal pull-down resistor[1]	M divider (feedback divider) inputs M5:2, and M0. See Table 3, Example Pin Selection of M Divider Using M5:2, M0 Pins, on pg. 2.
32	M5		Internal pull-up resistor[1]	
19, 34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note1: For typical values of internal pull-down and pull-up resistors, see DC Characteristics on pg. 6.

DEVICE CONFIGURATION TABLES

Example Pin Selection of M Divider Using M5:2, M0 Pins

M5:0 Pin Settings (Pins 32-28) M5 -M2, M0	Definition	Input Clock Freq (MHz) for Common VCSO Freqs F_{VCSO}=622.08[1]	F_{VCSO}=625.00[2]
5[3] 4 3 2 1[4] 0	Feedback Divider Value "M"		
0 0 0 1 0 0	M = 4	155.52	156.25
0 0 1 0 0 0	M = 8	77.76	
0 1 0 0 0 0	M = 16	38.80	
0 1 1 0 0 1	M = 25		25.00
1 0 0 0 0 0	M = 32	19.44	
1 1 1 1 0 1	M = 61		

Table 3: Example Pin Selection of M Divider Using M5:2, M0 Pins

Note1: F_{VCSO} = 622.08 MHz (*e.g.,* M901-01-622.0800)
Note2: F_{VCSO} = 625.00 MHz (*e.g.,* M901-01-625.0000)
Note3: M5 pin has pull-up resister; M4-M2 and M0 have pull-down.
Note4: M1 bit is always 0 (no M1 pin exists).

Pin Selection of P Divider Using P1:0 Pins

P1:0 Settings (Pin 13 and 12) P1	P0	P Divider Value	Output Frequency (MHz) Example when F_{VCSO} = 622.08[1]
0	0	1	622.08
0	1	2	311.04
1	0	4	155.52
1	1	8	77.76

Table 4: Pin Selection of P Divider Using P1:0 Pins

Note1: F_{VCSO} = 622.08MHz (e.g., M901-01-622.0800)

FUNCTIONAL DESCRIPTION

The M901-01 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock. The M901-01 combines the flexibility of a VCSO (Voltage Controlled SAW Oscillator) with the stability of a crystal oscillator.

The M901-01 uses a high-Q, narrow tuning range VCSO with a center frequency that is specified at time of device order (see Ordering Information on pg. 8). A suitable reference clock frequency, M Divider setting, and loop filter configuration must be used to assure proper operation.

Input Reference

An input clock reference is required. It should be a stable external clock source, such as a packaged crystal oscillator or distributed system clock. The clock reference is applied to the REF_IN input pin, which is internally applied to the non-inverting input of the phase detector.

See External Crystal Specifications in Application Information on pg. 4.

Internal PLL Operation

The internal PLL is comprised of a first order, type 3 frequency/phase detector, a SAW delay-line based VCO (VCSO), and a clock feedback divider.

The clock feedback divider (M Divider) divides the VCSO frequency and drives the inverting input of the phase detector, which is compared to the input reference clock. The PLL is “locked” when the phase detector inputs are aligned in frequency and phase; the phase detector output controls the VCSO frequency to achieve this, and the external loop filter provides stability to this frequency (and phase) control system. Hence, the VCSO frequency operates at “M” times the input reference frequency, thus accomplishing frequency translation. The external loop filter also acts as a low pass filter that provides attenuation of clock jitter on the reference input.

The relationship between the VCSO output frequency, the M divider, and the input reference frequency is defined as follows:

$$Fvcso = Fref\_in \times M$$

The product of M and the input frequency must be such that it falls within the “lock” range of the VCSO.

See APR in AC Characteristics on pg. 6.

P Divider and Outputs

The M901-01 provides one differential LVPECL output pair: FOUT, nFOUT. By using the P divider, the output frequency can be the VCSO center frequency (Fvcso) or 1/2, 1/4, or 1/8 Fvcso.

The P1 and P0 pins select the value for the P divider.

See Table 4, Pin Selection of P Divider Using P1:0 Pins, on pg. 2.

When the P divider is included, the complete relationship for the output frequency is defined as:

$$Fvcso = Fref\_in \times \frac{M}{P}$$

Configuration of M and P Dividers

The M and P dividers can be set by pin configuration using the input pins M0, M2 - M5, P0, and P1. The data on pins M5:2 and M0 and on pins P1:0 is passed directly to the M and P dividers.

The divider configuration of the M901-01 is reset and the outputs disabled when the input pin OUT_EN is set HIGH. MR is set LOW for divider configuration to be operational.

APPLICATION INFORMATION

This section includes information on the optional external crystal and on the external loop filter.

The subsections on the loop filter provide example component values and also briefly describe the SAW PLL simulator tool and additional application information available at www.icst.com.

External Crystal Specifications

If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should have the following general specifications:

Crystal Specifications

	Parameter	Min	Typ	Max	Unit
	Crystal Type		AT-cut quartz		
	Mode of Oscillation		Fundamental		
f_0	Frequency Range	16		40	MHz
ESR	Equivalent Series Resistance			50	Ω
	Spurious Response (non-harmonic)			-40	dBc
C_L	Load Capacitance, parallel load resonant	16		32	pF
P_0	Drive Level	0.1		1.0	mW

Table 5: Crystal Specifications

The external crystal will be applied to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.

Recommended External Crystal Configuration

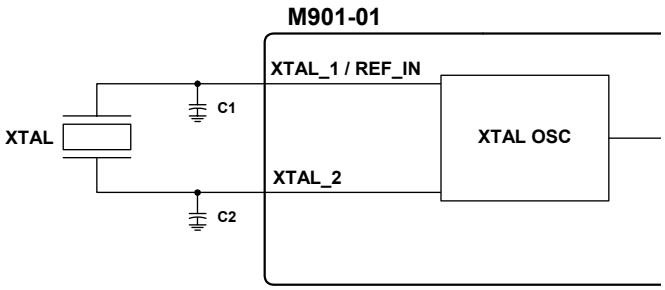


Figure 3: Recommended External Crystal Configuration

XTAL Load Capacitance Specification = 18 pF
C1 = 27 pF
C2 = 33 pF

External load capacitors C1 and C2 present a load of 15 pf to the crystal (they are seen in series by the crystal through the common ground connection). With the additional of PCB trace capacitance and M901-01 input capacitance, the total load to the crystal is about 18 pf.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M901-01 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

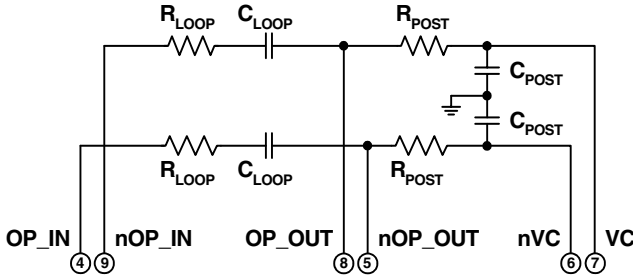


Figure 4: External Loop Filter

Example External Loop Filter Component Values

PLL Bandwidth	Damping Factor	R loop	C loop	R post	C post
400Hz	2.0	1.5kΩ	4.70µF	50kΩ	3300pF
1.2kHz	2.9	4.7kΩ	1.00µF	50kΩ	1500pF
2.5kHz	6.2	10.0kΩ	1.00µF	50kΩ	470pF
9.9kHz	3.6	39.0kΩ	0.022µF	20kΩ	470pF

Table 6: Example External Loop Filter Component Values

PLL Simulator Tool Available

A free PC software utility is available on the ICS web site. The SAW PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm for additional information.

SAW PLL Application Notes Available

The ICS web site (www.icst.com) also has application notes on:

- PCB layout guidelines (including special detailed instructions for preventing issues such as external reference crosstalk)
- Any new special device application details that may become available
- Instructions for using PLL simulator software
- Guidelines for PCB fabrication (including recommended PCB footprint, solder mask, and furnace profile)

Refer to the SAW PLL Application Notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes and any additional product information that may become available.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 7: Absolute Maximum Ratings

Note1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature					
		Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 8: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 622-675MHz,[1] LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			200		mA	
LVCMOS / LVTTL Input	V_{IH}	Input High Voltage	REF_IN, OUT_EN, P0, P1, M0, M2, M3, M4, M5	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
Inputs with Pull-down	I_{IH}	Input High Current	REF_IN, OUT_EN, P0:P1, M0, M2, M3, M4			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	M5			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			µA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Output	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [2]		0.4		0.85	V	

Table 9: DC Characteristics

Note1: For other VCSO center frequencies, contact ICS
Note2: Single-ended measurement.

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 622-675MHz,[1] LVPECL outputs terminated with 50Ω to V_{CC} - 2V

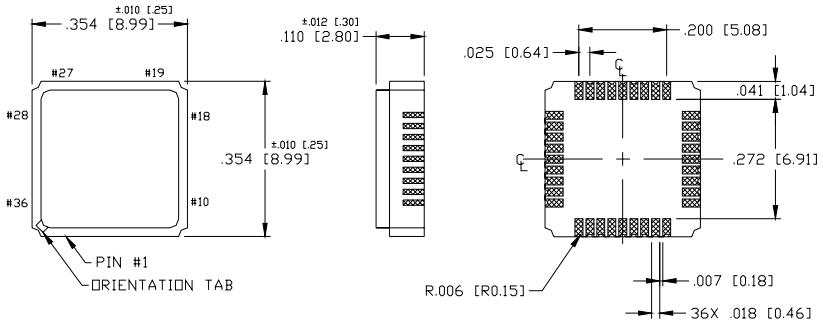
Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
F_{OUT}	Output Frequency Range		62		700	MHz	
F_{REF_IN}	Input Frequency				50	MHz	
APR	VCSO Pull-Range		±100	±150		ppm	
Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-87		dBc/Hz	
		10kHz Offset		-100		dBc/Hz	
		100kHz Offset		-123		dBc/Hz	
J(t)	Jitter (rms)			0.5	1.0	ps	12kHz to 20MHz
t_{DC}	Output Duty Cycle, High Time		40	50	60	%	
t_R	Output Rise Time	FOUT, nFOUT	200	400	550	ps	20% to 80%
t_F	Output Fall Time	FOUT, nFOUT	200	400	550	ps	20% to 80%

Table 10: AC Characteristics

Note1: For other VCSO center frequencies, contact ICS

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 5: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

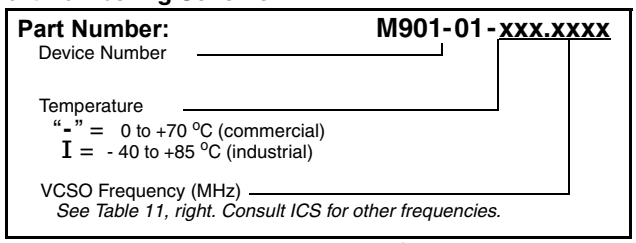


Figure 6: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*

622.0800	669.3120
625.0000	669.3266
627.3296	669.6429
644.5313	670.8386
666.5143	672.1600
669.1281	690.5692

Table 11: Standard VCSO Output Frequencies

Note *: Fout can equal Fvcso divided by: 1 or 4

Consult ICS for the availability of other PLL frequencies.

Example Part Numbers

PLL Frequency (MHz)	Temperature	Order Part Number
622.08	commercial	**M901-01- 622.0800**
	industrial	**M901-01I 622.0800**
625.00	commercial	**M901-01- 625.0000**
	industrial	**M901-01I 625.0000**
669.3266	commercial	**M901-01- 669.3266**
	industrial	**M901-01I 669.3266**
669.6429	commercial	**M901-01- 669.6429**
	industrial	**M901-01I 669.6429**

Table 12: Example Part Numbers