

EVALUATION KIT  
AVAILABLE**MAXIM**

# 10-Bit, 40Msps, +3.0V, Low-Power ADC with Internal Reference

**MAX1444**

## General Description

The MAX1444 10-bit, +3V analog-to-digital converter (ADC) features a pipelined 10-stage ADC architecture with fully differential wideband track-and-hold (T/H) input and digital error correction incorporating a fully differential signal path. This ADC is optimized for low-power, high dynamic performance applications in imaging and digital communications. The MAX1444 operates from a single +2.7V to +3.6V supply, consuming only 57mW while delivering a 59.5dB signal-to-noise ratio (SNR) at a 20MHz input frequency. The fully differential input stage has a 400MHz -3dB bandwidth and may be operated with single-ended inputs. In addition to low operating power, the MAX1444 features a 5µA power-down mode for idle periods.

An internal +2.048V precision bandgap reference is used to set the ADC full-scale range. A flexible reference structure allows the user to supply a buffered, direct, or externally derived reference for applications requiring increased accuracy or a different input voltage range.

Higher speed, pin-compatible versions of the MAX1444 are also available. Please refer to the MAX1446 data sheet (60Msps) and the MAX1448 data sheet (80Msps).

The MAX1444 has parallel, offset binary, CMOS-compatible three-state outputs that can be operated from +1.7V to +3.6V to allow flexible interfacing. The device is available in a 5x5mm 32-pin TQFP package and is specified over the extended industrial (-40°C to +85°C) temperature range.

## Applications

- Ultrasound Imaging
- CCD Imaging
- Baseband and IF Digitization
- Digital Set-Top Boxes
- Video Digitizing Applications

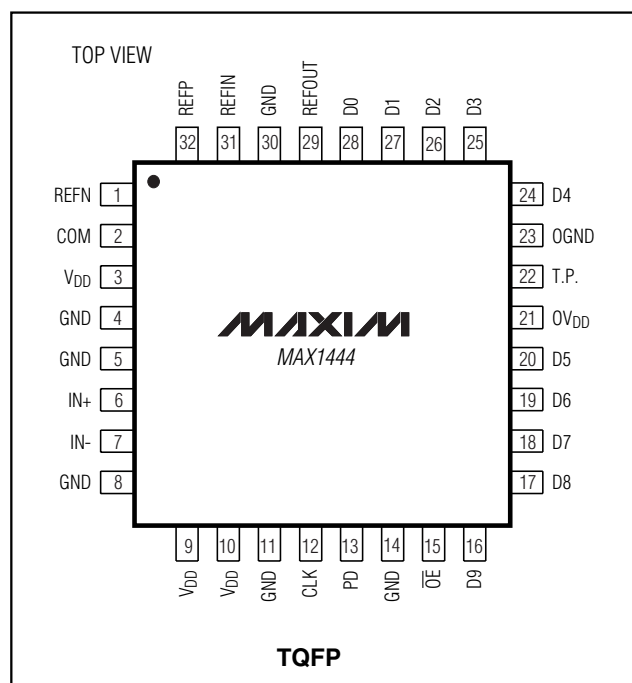
## Features

- ◆ Single +3.0V Operation
- ◆ Excellent Dynamic Performance
  - 59.5dB SNR at  $f_{IN} = 20\text{MHz}$
  - 74dBc SFDR at  $f_{IN} = 20\text{MHz}$
- ◆ Low Power
  - 19mA (Normal Operation)
  - 5µA (Shutdown Mode)
- ◆ Fully Differential Analog Input
- ◆ Wide 2Vp-p Differential Input Voltage Range
- ◆ 400MHz -3dB Input Bandwidth
- ◆ On-Chip +2.048V Precision Bandgap Reference
- ◆ CMOS-Compatible Three-State Outputs
- ◆ 32-Pin TQFP Package
- ◆ Evaluation Kit Available

## Ordering Information

| PART       | TEMP. RANGE    | PIN-PACKAGE |
|------------|----------------|-------------|
| MAX1444EHJ | -40°C to +85°C | 32 TQFP     |

## Pin Configuration



Functional Diagram appears at end of data sheet.

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## ABSOLUTE MAXIMUM RATINGS

|                                                 |                                    |
|-------------------------------------------------|------------------------------------|
| V <sub>DD</sub> , OV <sub>DD</sub> to GND ..... | -0.3V to +3.6V                     |
| OGND to GND .....                               | -0.3V to +0.3V                     |
| IN+, IN- to GND .....                           | -0.3V to V <sub>DD</sub>           |
| REFIN, REFOUT, REFP, REFN, and COM to GND ..... | -0.3V to (V <sub>DD</sub> + 0.3V)  |
| OE, PD, CLK to GND .....                        | -0.3V to (V <sub>DD</sub> + 0.3V)  |
| D9–D0 to GND .....                              | -0.3V to (OV <sub>DD</sub> + 0.3V) |

|                                                       |                 |
|-------------------------------------------------------|-----------------|
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                 |
| 32-Pin TQFP (derate 11.1mW/°C above +70°C) .....      | 889mW           |
| Operating Temperature Range .....                     | -40°C to +85°C  |
| Storage Temperature Range .....                       | -60°C to +150°C |
| Lead Temperature (soldering, 10s) .....               | +300°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +3.0V, OV<sub>DD</sub> = +2.7V; 0.1μF and 1.0μF capacitors from REFP, REFN, and COM to GND; V<sub>REFIN</sub> = +2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V<sub>IN</sub> = 2V<sub>p-p</sub> (differential w.r.t. COM), C<sub>L</sub> = 10pF at digital outputs, f<sub>CLK</sub> = 40MHz (50% duty cycle), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

| PARAMETER                                                                 | SYMBOL            | CONDITIONS                                             | MIN  | TYP                        | MAX  | UNITS  |
|---------------------------------------------------------------------------|-------------------|--------------------------------------------------------|------|----------------------------|------|--------|
| <b>DC ACCURACY</b>                                                        |                   |                                                        |      |                            |      |        |
| Resolution                                                                |                   |                                                        | 10   |                            |      | bits   |
| Integral Nonlinearity                                                     | INL               | f <sub>IN</sub> = 7.51MHz                              |      | ±0.6                       | ±1.9 | LSB    |
| Differential Nonlinearity                                                 | DNL               | f <sub>IN</sub> = 7.51MHz, no missing codes guaranteed |      | ±0.4                       | ±1.0 | LSB    |
| Offset Error                                                              |                   |                                                        |      | <±0.1                      | ±1.7 | % FS   |
| Gain Error                                                                |                   |                                                        |      | 0                          | ±2   | % FS   |
| <b>ANALOG INPUT</b>                                                       |                   |                                                        |      |                            |      |        |
| Input Differential Range                                                  | V <sub>DIFF</sub> | Differential or single-ended inputs                    |      | ±1.0                       |      | V      |
| Common-Mode Voltage Range                                                 | V <sub>COM</sub>  |                                                        |      | V <sub>DD</sub> /2<br>±0.5 |      | V      |
| Input Resistance                                                          | R <sub>IN</sub>   | Switched capacitor load                                |      | 50                         |      | kΩ     |
| Input Capacitance                                                         | C <sub>IN</sub>   |                                                        |      | 5                          |      | pF     |
| <b>CONVERSION RATE</b>                                                    |                   |                                                        |      |                            |      |        |
| Maximum Clock Frequency                                                   | f <sub>CLK</sub>  |                                                        | 40   |                            |      | MHz    |
| Data Latency                                                              |                   |                                                        |      | 5.5                        |      | cycles |
| <b>DYNAMIC CHARACTERISTICS</b> (f <sub>CLK</sub> = 40MHz, 4096-point FFT) |                   |                                                        |      |                            |      |        |
| Signal-To-Noise Ratio                                                     | SNR               | f <sub>IN</sub> = 7.51MHz                              | 57.5 | 59.5                       |      | dB     |
|                                                                           |                   | f <sub>IN</sub> = 19.91MHz                             | 57   | 59.5                       |      |        |
|                                                                           |                   | f <sub>IN</sub> = 39.9MHz (Note 1)                     |      | 58.5                       |      |        |
| Signal-To-Noise And Distortion (Up to 5th harmonic)                       | SINAD             | f <sub>IN</sub> = 7.51MHz                              | 57   | 59.4                       |      | dB     |
|                                                                           |                   | f <sub>IN</sub> = 19.91MHz                             | 56.7 | 59                         |      |        |
|                                                                           |                   | f <sub>IN</sub> = 39.9MHz (Note 1)                     |      | 58.3                       |      |        |
| Spurious-Free Dynamic Range                                               | SFDR              | f <sub>IN</sub> = 7.51MHz                              | 67   | 75                         |      | dBc    |
|                                                                           |                   | f <sub>IN</sub> = 19.91MHz                             | 66   | 74                         |      |        |
|                                                                           |                   | f <sub>IN</sub> = 39.9 MHz (Note 1)                    |      | 72.5                       |      |        |

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ ; 0.1 $\mu F$  and 1.0 $\mu F$  capacitors from REFP, REFN, and COM to GND;  $V_{REFIN} = +2.048V$ , REFOUT connected to REFIN through a 10k $\Omega$  resistor,  $V_{IN} = 2V_{p-p}$  (differential w.r.t. COM),  $C_L = 10pF$  at digital outputs,  $f_{CLK} = 40MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER                                                   | SYMBOL           | CONDITIONS                                                             | MIN  | TYP                  | MAX  | UNITS           |
|-------------------------------------------------------------|------------------|------------------------------------------------------------------------|------|----------------------|------|-----------------|
| Third-Harmonic Distortion                                   | HD3              | $f_{IN} = 7.51MHz$                                                     |      | -75                  |      | dBc             |
|                                                             |                  | $f_{IN} = 19.91MHz$                                                    |      | -74                  |      |                 |
|                                                             |                  | $f_{IN} = 39.9MHz$ (Note 1)                                            |      | -72.5                |      |                 |
| Two-Tone Intermodulation Distortion                         | IMD              | $f_1 = 11.5MHz$ at -6.5dBFS<br>$f_2 = 13.5MHz$ at -6.5dBFS<br>(Note 2) |      | -76                  |      | dBc             |
| Third-Order Intermodulation Distortion                      | IM3              | $f_1 = 11.5MHz$ at -6.5dBFS<br>$f_2 = 13.5MHz$ at -6.5dBFS<br>(Note 2) |      | -76                  |      | dBc             |
| Total Harmonic Distortion<br>(First 5 Harmonics)            | THD              | $f_{IN} = 7.51MHz$                                                     |      | -73.8                | -65  | dBc             |
|                                                             |                  | $f_{IN} = 19.91MHz$                                                    |      | -72.2                | -65  |                 |
|                                                             |                  | $f_{IN} = 39.9MHz$ (Note 1)                                            |      | -70                  |      |                 |
| Small-Signal Bandwidth                                      |                  | Input at -20dBFS, differential inputs                                  |      | 500                  |      | MHz             |
| Full-Power Bandwidth                                        | FPBW             | Input at -0.5dBFS, differential inputs                                 |      | 400                  |      | MHz             |
| Aperture Delay                                              | $t_{AD}$         |                                                                        |      | 1                    |      | ns              |
| Aperture Jitter                                             | $t_{AJ}$         |                                                                        |      | 2                    |      | psRMS           |
| Overdrive Recovery Time                                     |                  | For $1.5 \times$ full-scale input                                      |      | 2                    |      | ns              |
| Differential Gain                                           |                  |                                                                        |      | $\pm 1$              |      | %               |
| Differential Phase                                          |                  |                                                                        |      | $\pm 0.25$           |      | degree          |
| Output Noise                                                |                  | $IN+ = IN- = COM$                                                      |      | 0.2                  |      | LSBRMS          |
| <b>INTERNAL REFERENCE</b>                                   |                  |                                                                        |      |                      |      |                 |
| Reference Output Voltage                                    | REFOUT           |                                                                        |      | $2.048 \pm 1\%$      |      | V               |
| Reference Temperature Coefficient                           | $TC_{REF}$       |                                                                        |      | 60                   |      | ppm/ $^\circ C$ |
| Load Regulation                                             |                  |                                                                        |      | 1.25                 |      | mV/mA           |
| <b>EXTERNAL REFERENCE</b>                                   |                  |                                                                        |      |                      |      |                 |
| Positive Reference                                          | REFP             | $V_{REFIN} = +2.048V$                                                  |      | 2.012                |      | V               |
| Negative Reference                                          | REFN             | $V_{REFIN} = +2.048V$                                                  |      | 0.988                |      | V               |
| Differential Reference Voltage                              | $\Delta V_{REF}$ | $V_{REFP} - V_{REFN}$ , $V_{REFIN} = +2.048V$                          | 0.98 | 1.024                | 1.07 | V               |
| REFIN Resistance                                            | $R_{REFIN}$      |                                                                        |      | >50                  |      | M $\Omega$      |
| <b>DIGITAL INPUTS (CLK, PD, <math>\overline{OE}</math>)</b> |                  |                                                                        |      |                      |      |                 |
| Input High Threshold                                        | $V_{IH}$         | CLK                                                                    |      | $0.8 \times V_{DD}$  |      | V               |
|                                                             |                  | PD, $\overline{OE}$                                                    |      | $0.8 \times OV_{DD}$ |      |                 |
| Input Low Threshold                                         | $V_{IL}$         | CLK                                                                    |      | $0.2 \times V_{DD}$  |      | V               |
|                                                             |                  | PD, $\overline{OE}$                                                    |      | $0.2 \times OV_{DD}$ |      |                 |

# 10-Bit, 40MSPS, +3.0V, Low-Power ADC with Internal Reference

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ ; 0.1 $\mu F$  and 1.0 $\mu F$  capacitors from REFP, REFN, and COM to GND;  $V_{REFIN} = +2.048V$ , REFOUT connected to REFIN through a 10k $\Omega$  resistor,  $V_{IN} = 2V_{p-p}$  (differential w.r.t. COM),  $C_L = 10pF$  at digital outputs,  $f_{CLK} = 40MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER                              | SYMBOL               | CONDITIONS                                                    | MIN                       | TYP | MAX | UNITS |
|----------------------------------------|----------------------|---------------------------------------------------------------|---------------------------|-----|-----|-------|
| Input Hysteresis                       | V <sub>HYST</sub>    |                                                               | 0.1                       |     |     | V     |
| Input Leakage                          | I <sub>IH</sub>      | V <sub>IH</sub> = V <sub>DD</sub> = OV <sub>DD</sub>          | ±5                        |     |     | μA    |
|                                        | I <sub>IL</sub>      | V <sub>IL</sub> = 0                                           | ±5                        |     |     |       |
| Input Capacitance                      | C <sub>IN</sub>      |                                                               | 5                         |     |     | pF    |
| DIGITAL OUTPUTS (D9–D0)                |                      |                                                               |                           |     |     |       |
| Output Voltage Low                     | V <sub>OL</sub>      | I <sub>SINK</sub> = 200μA                                     | 0.2                       |     |     | V     |
| Output Voltage High                    | V <sub>OH</sub>      | I <sub>SOURCE</sub> = 200μA                                   | OV <sub>DD</sub><br>- 0.2 |     |     | V     |
| Three-State Leakage Current            | I <sub>LEAK</sub>    | $\overline{OE}$ = OV <sub>DD</sub>                            | ±10                       |     |     | μA    |
| Three-State Output Capacitance         | C <sub>OUT</sub>     | $\overline{OE}$ = OV <sub>DD</sub>                            | 5                         |     |     | pF    |
| POWER REQUIREMENTS                     |                      |                                                               |                           |     |     |       |
| Analog Supply Voltage                  | V <sub>DD</sub>      |                                                               | 2.7                       | 3.0 | 3.6 | V     |
| Output Supply Voltage                  | OV <sub>DD</sub>     |                                                               | 1.7                       | 3.0 | 3.6 | V     |
| Analog Supply Current                  | I <sub>VDD</sub>     | Operating, f <sub>IN</sub> = 19.91MHz at -0.5dBFS             | 19                        |     | 25  | mA    |
|                                        |                      | Shutdown, clock idle, PD = $\overline{OE}$ = OV <sub>DD</sub> | 4                         |     | 15  | μA    |
| Output Supply Current                  | I <sub>OVDD</sub>    | Operating, f <sub>IN</sub> = 19.91MHz at -0.5dBFS             | 4.5                       |     |     | mA    |
|                                        |                      | Shutdown, clock idle, PD = $\overline{OE}$ = OV <sub>DD</sub> | 1                         |     | 10  | μA    |
| Power Supply Rejection                 | PSRR                 | Offset                                                        | ±0.1                      |     |     | mV/V  |
|                                        |                      | Gain                                                          | ±0.1                      |     |     | %/V   |
| TIMING CHARACTERISTICS                 |                      |                                                               |                           |     |     |       |
| CLK Rise to Output Data Valid          | t <sub>DO</sub>      | Figure 6, (Note 3)                                            | 5                         |     | 8   | ns    |
| $\overline{OE}$ Fall to Output Enable  | t <sub>ENABLE</sub>  | Figure 5                                                      | 10                        |     |     | ns    |
| $\overline{OE}$ Rise to Output Disable | t <sub>DISABLE</sub> | Figure 5                                                      | 15                        |     |     | ns    |
| CLK Pulse Width High                   | t <sub>CH</sub>      | Figure 6, clock period 25ns                                   | 12.5 ±3.8                 |     |     | ns    |
| CLK Pulse Width Low                    | t <sub>CL</sub>      | Figure 6, clock period 25ns                                   | 12.5 ±3.8                 |     |     | ns    |
| Wake-up Time                           | t <sub>WAKE</sub>    | (Note 4)                                                      | 1.7                       |     |     | μs    |

**Note 1:** SNR, SINAD, THD, SFDR, and HD3 are based on an analog input voltage of -0.5dBFS referenced to a +1.024V full-scale input voltage range.

**Note 2:** Intermodulation distortion is the total power of the intermodulation products relative to the individual carrier. This number is 6dB better if referenced to the two-tone envelope.

**Note 3:** Digital outputs settle to  $V_{IH}$  /  $V_{IL}$ .

**Note 4:** REFIN is driven externally. REFP, COM, and REFN are left floating while powered down.

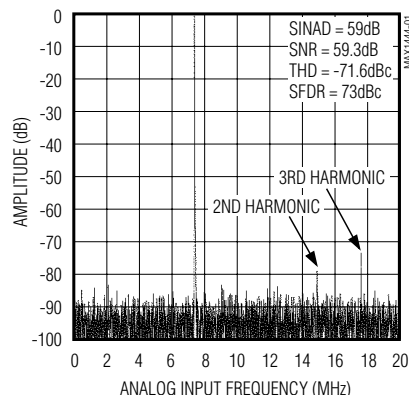
# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

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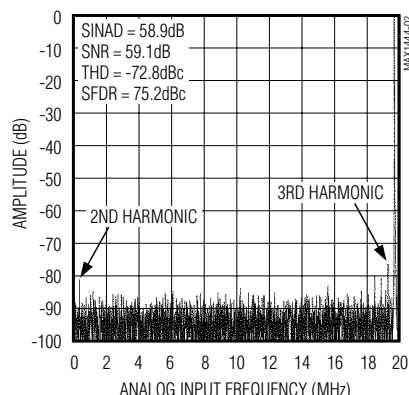
## Typical Operating Characteristics

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ , internal reference, differential input at  $-0.5dB$  FS,  $f_{CLK} = 40MHz$ ,  $C_L \approx 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

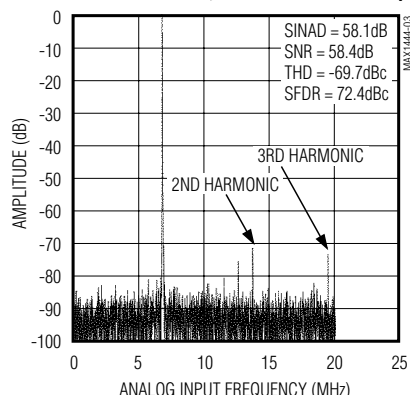
**FFT PLOT ( $f_{IN} = 7.51MHz$ ,  
8192-POINT FFT, DIFFERENTIAL INPUT)**



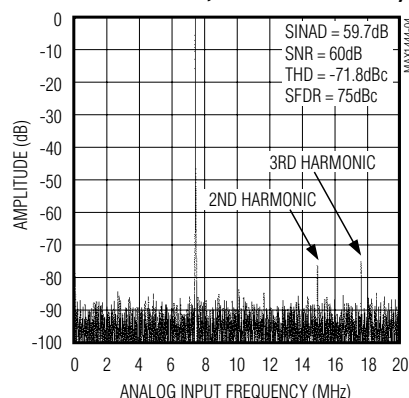
**FFT PLOT ( $f_{IN} = 19.91MHz$ ,  
8192-POINT FFT, DIFFERENTIAL INPUT)**



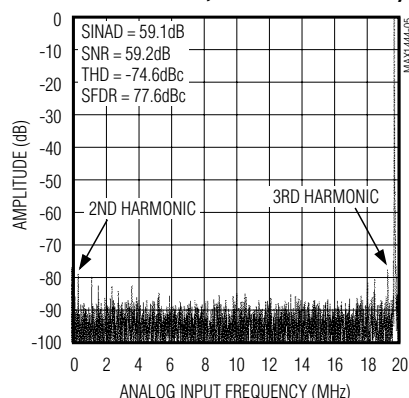
**FFT PLOT ( $f_{IN} = 47MHz$ ,  
8192-POINT FFT, DIFFERENTIAL INPUT)**



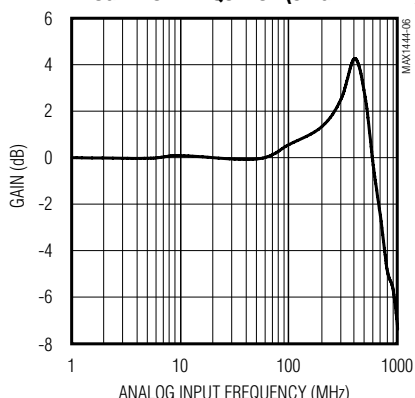
**FFT PLOT ( $f_{IN} = 7.51MHz$ ,  
8192-POINT FFT, SINGLE-ENDED INPUT)**



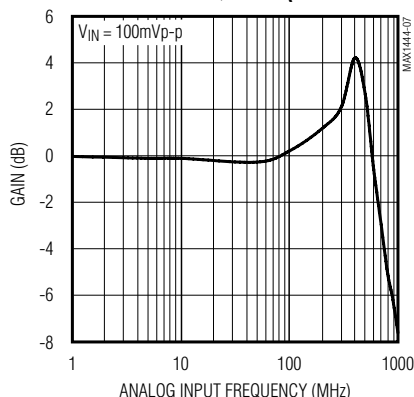
**FFT PLOT ( $f_{IN} = 19.91MHz$ ,  
8192-POINT FFT, SINGLE-ENDED INPUT)**



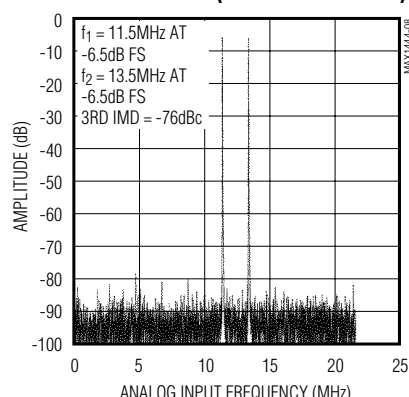
**FULL-POWER INPUT BANDWIDTH vs.  
ANALOG INPUT FREQUENCY (SINGLE-ENDED)**



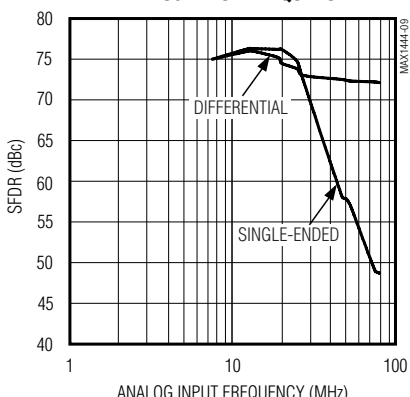
**SMALL-SIGNAL INPUT BANDWIDTH vs.  
ANALOG INPUT FREQUENCY (SINGLE-ENDED)**



**TWO-TONE INTERMODULATION  
8192-POINT IMD (DIFFERENTIAL INPUT)**



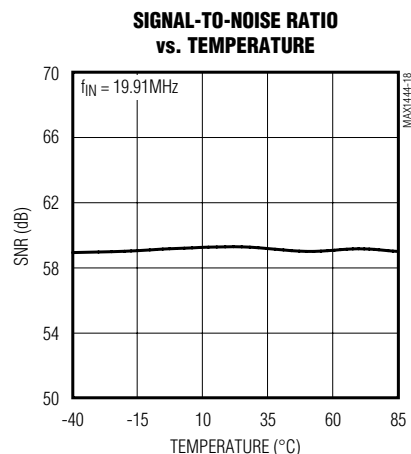
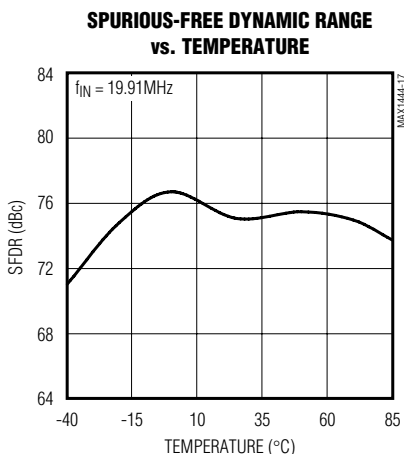
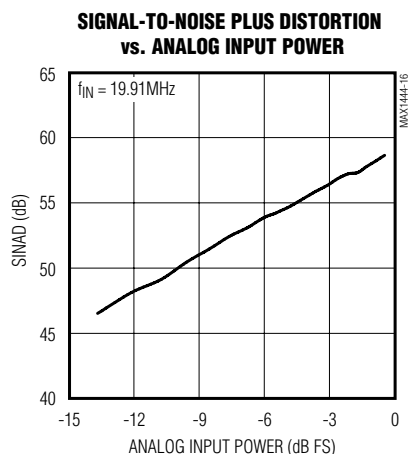
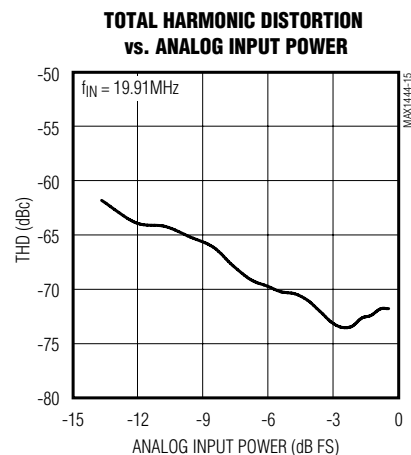
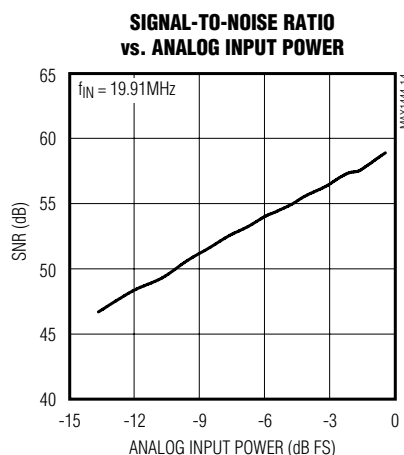
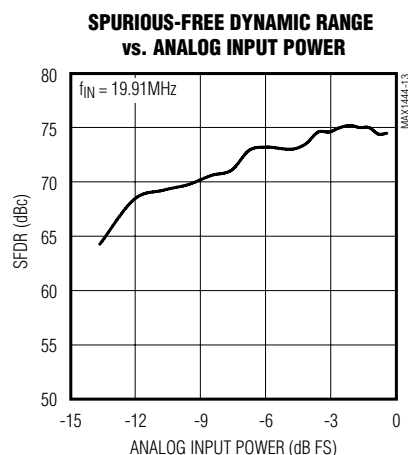
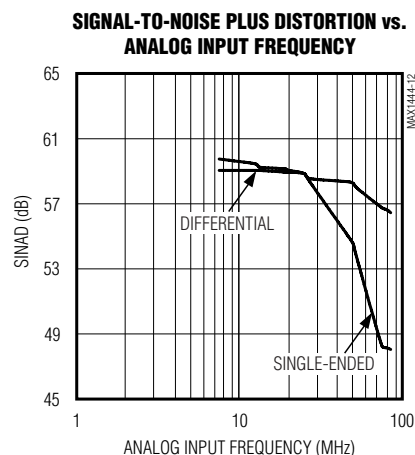
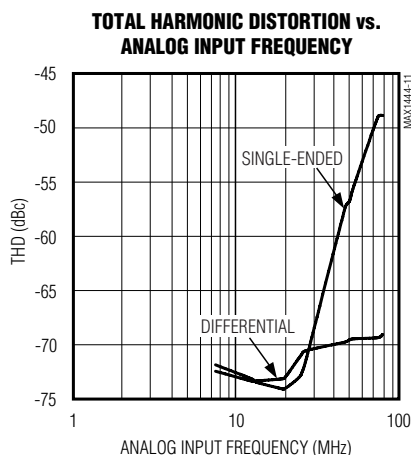
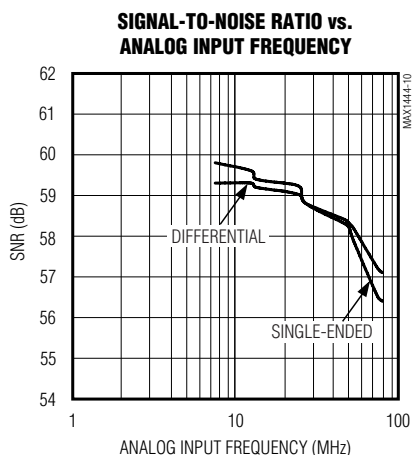
**SPURIOUS-FREE DYNAMIC RANGE vs.  
ANALOG INPUT FREQUENCY**



# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

## Typical Operating Characteristics (continued)

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ , internal reference, differential input at  $-0.5dB$  FS,  $f_{CLK} = 40MHz$ ,  $C_L \approx 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



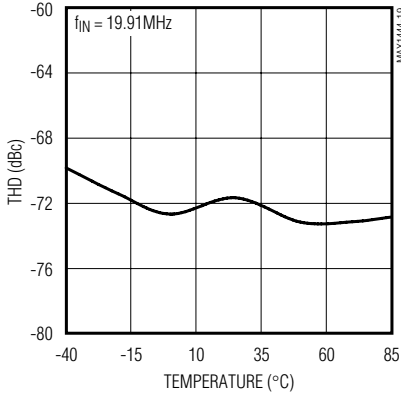
# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

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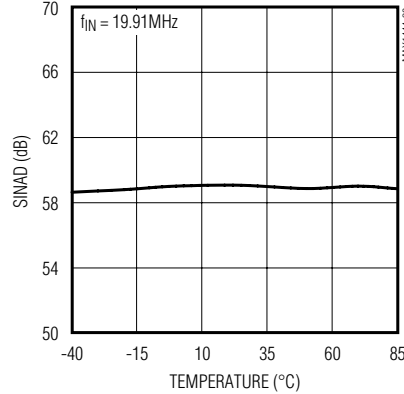
## Typical Operating Characteristics (continued)

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ , internal reference, differential input at -0.5dB FS,  $f_{CLK} = 40MHz$ ,  $C_L \approx 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

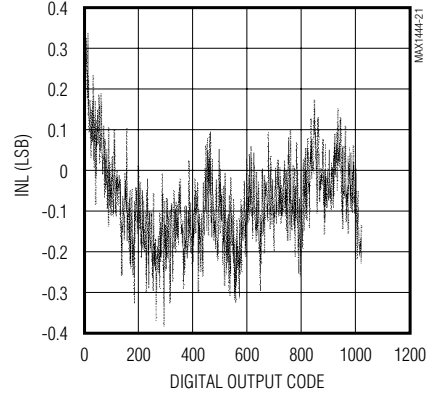
**TOTAL HARMONIC DISTORTION vs. TEMPERATURE**



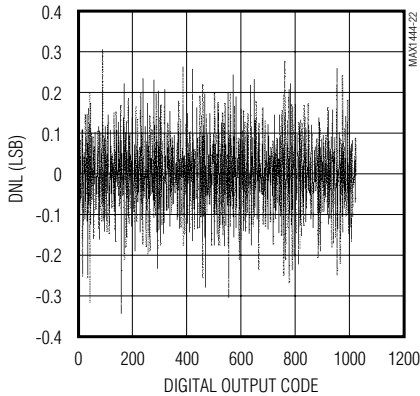
**SIGNAL-TO-NOISE PLUS DISTORTION vs. TEMPERATURE**



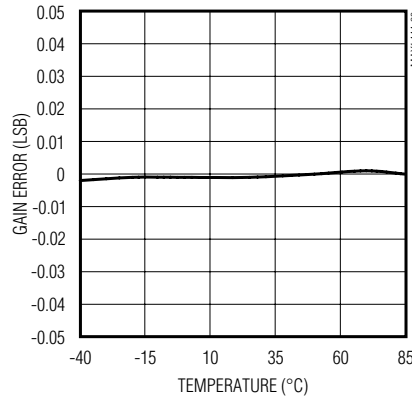
**INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (BEST STRAIGHT LINE)**



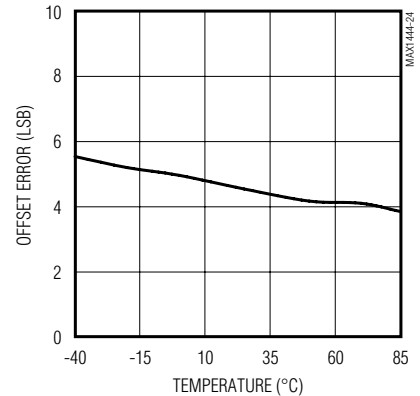
**DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE**



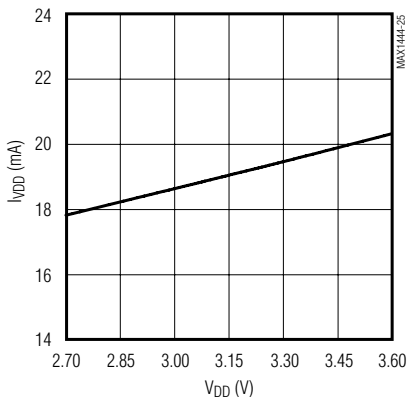
**GAIN ERROR vs. TEMPERATURE, EXTERNAL REFERENCE ( $V_{REFIN} = +2.048V$ )**



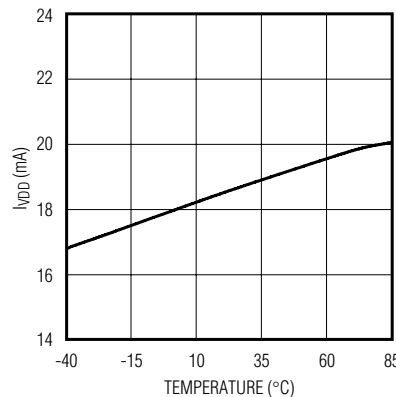
**OFFSET ERROR vs. TEMPERATURE, EXTERNAL REFERENCE ( $V_{REFIN} = +2.048V$ )**



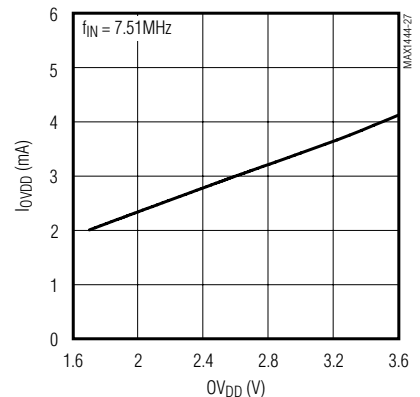
**ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE**



**ANALOG SUPPLY CURRENT vs. TEMPERATURE**



**DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE**

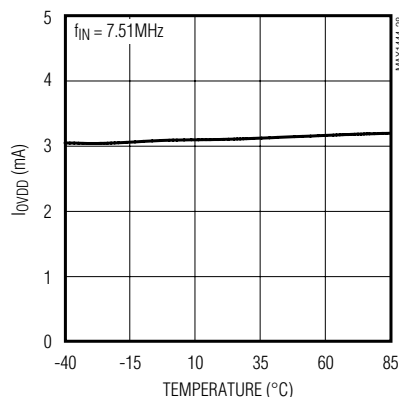


# 10-Bit, 40MSPS, +3.0V, Low-Power ADC with Internal Reference

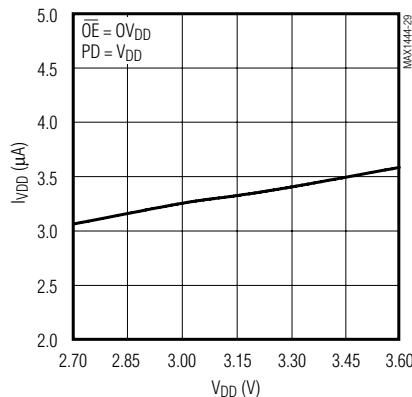
## Typical Operating Characteristics (continued)

( $V_{DD} = +3.0V$ ,  $OV_{DD} = +2.7V$ , internal reference, differential input at -0.5dB FS,  $f_{CLK} = 40MHz$ ,  $C_L \approx 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

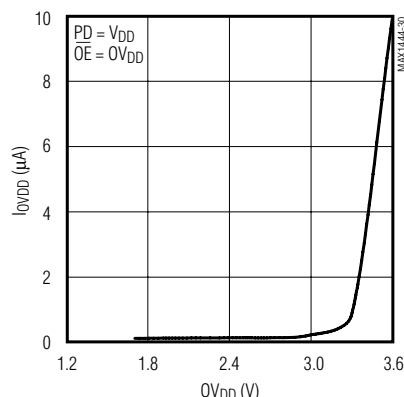
**DIGITAL SUPPLY CURRENT  
vs. TEMPERATURE**



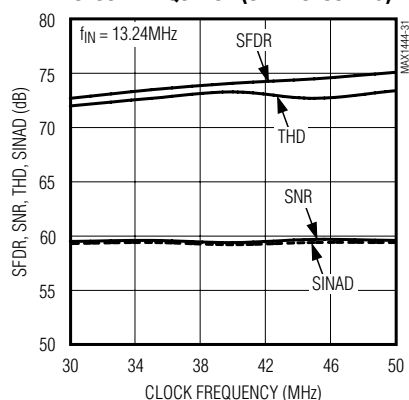
**ANALOG POWER-DOWN CURRENT  
vs. ANALOG POWER SUPPLY**



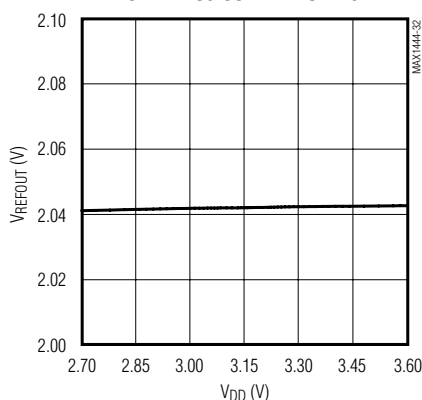
**DIGITAL POWER-DOWN CURRENT  
vs. DIGITAL POWER SUPPLY**



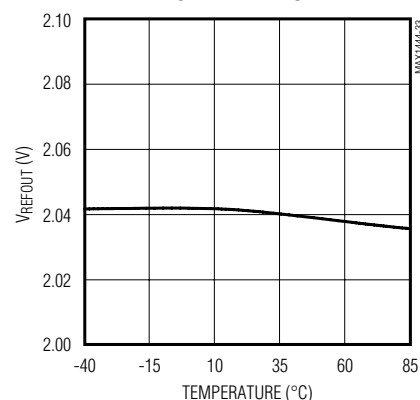
**SFDR, SNR, THD, SINAD vs.  
CLOCK FREQUENCY (OVER-CLOCKING)**



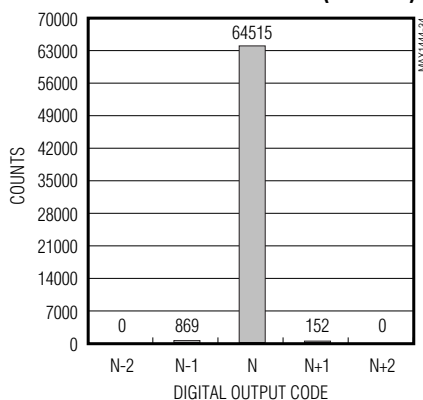
**INTERNAL REFERENCE VOLTAGE  
vs. ANALOG SUPPLY VOLTAGE**



**INTERNAL REFERENCE VOLTAGE  
vs. TEMPERATURE**



**OUTPUT NOISE HISTOGRAM (DC INPUT)**





# 10-Bit, 40Msps, +3.0V, Low-Power ADC with Internal Reference

## Pin Description

MAX1444

| PIN                 | NAME                   | FUNCTION                                                                                                                         |
|---------------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| 1                   | REFN                   | Lower Reference. Conversion range is $\pm(V_{REFP} - V_{REFN})$ . Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.             |
| 2                   | COM                    | Common-Mode Voltage Output. Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.                                                   |
| 3, 9, 10            | $V_{DD}$               | Analog Supply Voltage. Bypass to GND with a capacitor combination of $2.2\mu\text{F}$ in parallel with $0.1\mu\text{F}$ .        |
| 4, 5, 8, 11, 14, 30 | GND                    | Analog Ground                                                                                                                    |
| 6                   | IN+                    | Positive Analog Input. For single-ended operation, connect signal source to IN+.                                                 |
| 7                   | IN-                    | Negative Analog Input. For single-ended operation, connect IN- to COM.                                                           |
| 12                  | CLK                    | Conversion Clock Input                                                                                                           |
| 13                  | PD                     | Power Down Input. High: Power-down mode. Low: Normal operation.                                                                  |
| 15                  | $\overline{\text{OE}}$ | Output Enable Input. High: Digital outputs disabled. Low: Digital outputs enabled.                                               |
| 16–20               | D9–D5                  | Three-State Digital Outputs D9–D5. D9 is the MSB.                                                                                |
| 21                  | $\text{OV}_{DD}$       | Output Driver Supply Voltage. Bypass to GND with a capacitor combination of $2.2\mu\text{F}$ in parallel with $0.1\mu\text{F}$ . |
| 22                  | T.P.                   | Test Point. <b>Do not connect.</b>                                                                                               |
| 23                  | OGND                   | Output Driver Ground                                                                                                             |
| 24–28               | D4–D0                  | Three-State Digital Outputs D4–D0. D0 is the LSB.                                                                                |
| 29                  | REFOUT                 | Internal Reference Voltage Output. May be connected to REFIN through a resistor or a resistor-divider.                           |
| 31                  | REFIN                  | Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$ . Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.               |
| 32                  | REFP                   | Upper Reference. Conversion range is $\pm(V_{REFP} - V_{REFN})$ . Bypass to GND with a $> 0.1\mu\text{F}$ capacitor.             |

# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

## Detailed Description

The MAX1444 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half-clock cycle. Counting the delay through the output latch, the clock-cycle latency is 5.5.

A 1.5-bit (2-comparator) flash ADC converts the held input voltage into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage where the process is repeated until the signal has been processed by all 10 stages. Each stage provides a 1-bit resolution. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes.

## Input Track-and-Hold Circuit

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuit in both track and hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuit samples the input signal onto the two capacitors (C2a and C2b). Switches S2a and S2b set the common mode for the amplifier input. The resulting differential

voltage is held on C2a and C2b. Switches S4a, S4b, S5a, S5b, S1, S2a, and S2b are then opened before S3a, S3b, and S4c are closed, connecting capacitors C1a and C1b to the amplifier output. This charges C1a and C1b to the same values originally held on C2a and C2b. This value is then presented to the first-stage quantizer and isolates the pipeline from the fast-changing input. The wide-input-bandwidth T/H amplifier allows the MAX1444 to track and sample/hold analog inputs of high frequencies beyond Nyquist. The analog inputs (IN+ and IN-) can be driven either differentially or single-ended. It is recommended to match the impedance of IN+ and IN- and set the common-mode voltage to midsupply ( $V_{DD}/2$ ) for optimum performance.

## Analog Input and Reference Configuration

The MAX1444 full-scale range is determined by the internally generated voltage difference between REFP ( $V_{DD}/2 + V_{REFIN}/4$ ) and REFN ( $V_{DD}/2 - V_{REFIN}/4$ ). The ADC's full-scale range is user-adjustable through the REF pin, which provides a high input impedance for this purpose. REFOUT, REFP, COM ( $V_{DD}/2$ ), and REFN are internally buffered, low-impedance outputs.

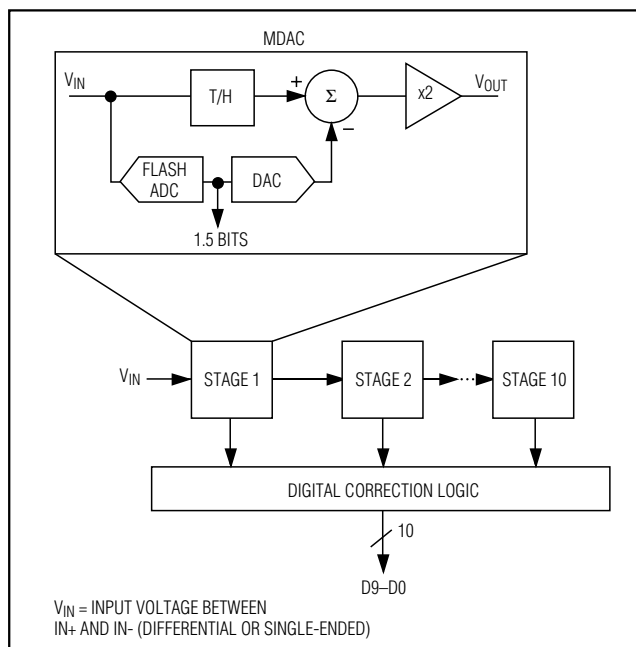


Figure 1. Pipelined Architecture—Stage Blocks

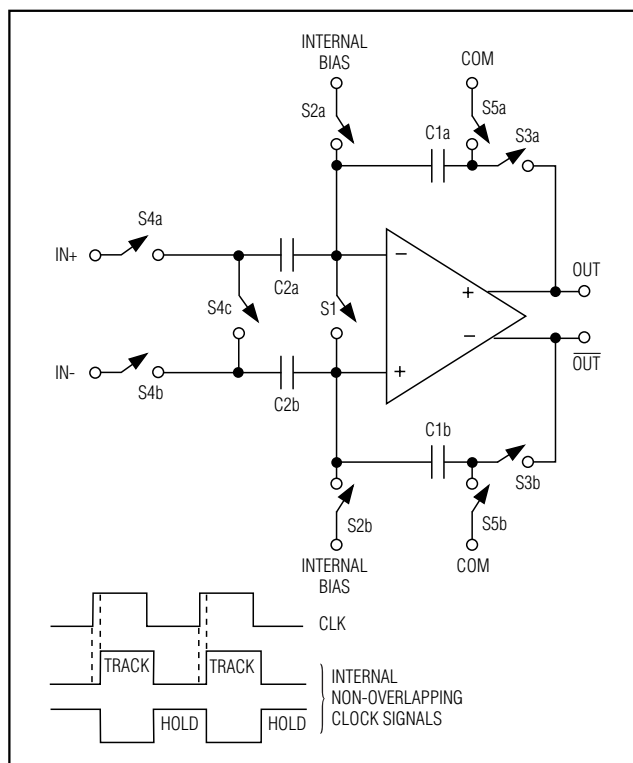


Figure 2. Internal T/H Circuit

# 10-Bit, 40Msps, +3.0V, Low-Power ADC with Internal Reference

The MAX1444 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, the internal reference output (REFOUT) can be tied to the REFIN pin through a resistor (e.g., 10k $\Omega$ ) or resistor-divider if an application requires a reduced full-scale range. For stability purposes, it is recommended to bypass REFIN with a >10nF capacitor to GND.

In buffered external reference mode, the reference voltage levels can be adjusted externally by applying a stable and accurate voltage at REFIN. In this mode, REFOUT may be left open or connected to REFIN through a >10k $\Omega$  resistor.

In unbuffered external reference mode, REFIN is connected to GND, thereby deactivating the on-chip buffers of REFP, COM, and REFN. With their buffers shut down, these pins become high impedance and can be driven by external reference sources.

## Clock Input (CLK)

The MAX1444 CLK input accepts CMOS-compatible clock signals. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). In particular, sampling occurs on the falling edge of the clock signal, mandating this edge to provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the ADC as follows:

$$\text{SNR} = 20 \log (1 / 2\pi f_{\text{IN}} t_{\text{AJ}})$$

where  $f_{\text{IN}}$  represents the analog input frequency, and  $t_{\text{AJ}}$  is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be considered as an analog input and routed away from any analog input or other digital signal lines.

The MAX1444 clock input operates with a voltage threshold set to  $V_{\text{DD}}/2$ . Clock inputs with a duty cycle other than 50% must meet the specifications for high and low periods as stated in the *Electrical Characteristics*. See Figures 3a, 3b, 4a, and 4b for the relationship between spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), total harmonic distortion (THD), or signal-to-noise plus distortion (SINAD) versus duty cycle.

## Output Enable ( $\overline{\text{OE}}$ ), Power Down (PD), and Output Data (D0–D9)

All data outputs, D0 (LSB) through D9 (MSB), are TTL/CMOS-logic compatible. There is a 5.5 clock-cycle latency between any particular sample and its valid output data. The output coding is straight offset binary (Table 1). With  $\overline{\text{OE}}$  and PD (power down) high, the digital output enters a high-impedance state. If  $\overline{\text{OE}}$  is held low with PD high, the outputs are latched at the last value prior to the power down.

The capacitive load on the digital outputs D0–D9 should be kept as low as possible (<15pF) to avoid large digital currents that could feed back into the analog portion of the MAX1444, thus degrading its dynamic performance. The use of buffers on the ADC's digital outputs can further isolate the digital outputs from heavy capacitive loads.

Figure 5 displays the timing relationship between output enable and data output valid as well as power-down/wake-up and data output valid.

**Table 1. MAX1444 Output Code for Differential Inputs**

| DIFFERENTIAL INPUT VOLTAGE*      | DIFFERENTIAL INPUT         | STRAIGHT OFFSET BINARY |
|----------------------------------|----------------------------|------------------------|
| $V_{\text{REF}} \times 511/512$  | +Full Scale -1LSB          | 11 1111 1111           |
| $V_{\text{REF}} \times 510/512$  | +Full Scale -2LSB          | 11 1111 1110           |
| $V_{\text{REF}} \times 1/512$    | +1LSB                      | 10 0000 0001           |
| 0                                | Bipolar Zero               | 10 0000 0000           |
| $-V_{\text{REF}} \times 1/512$   | -1LSB                      | 01 1111 1111           |
| $-V_{\text{REF}} \times 511/512$ | Negative Full Scale + 1LSB | 00 0000 0001           |
| $-V_{\text{REF}} \times 512/512$ | Negative Full Scale        | 00 0000 0000           |

\* $V_{\text{REF}} = V_{\text{REFP}} - V_{\text{REFN}}$

# 10-Bit, 40MSPS, +3.0V, Low-Power ADC with Internal Reference

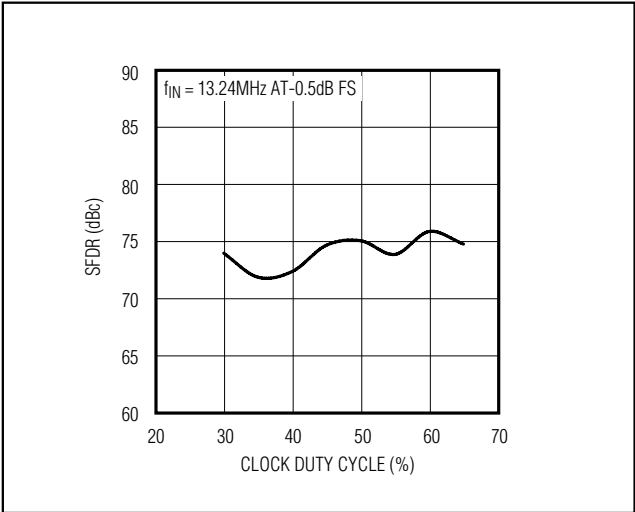


Figure 3a. Spurious-Free Dynamic Range vs. Clock Duty Cycle (Differential Input)

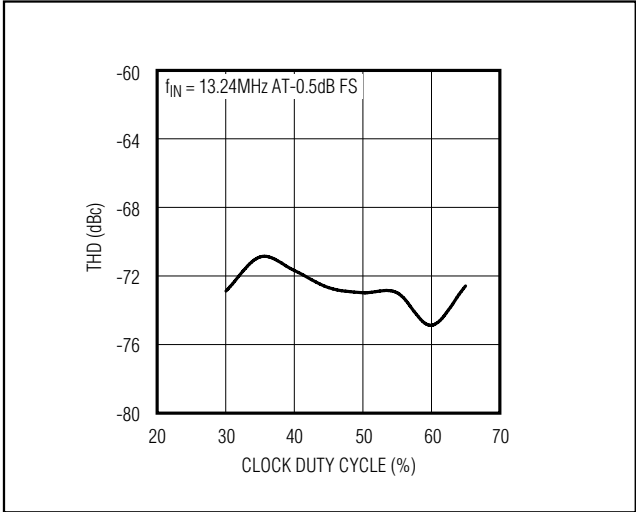


Figure 4a. Total Harmonic Distortion vs. Clock Duty Cycle (Differential Input)

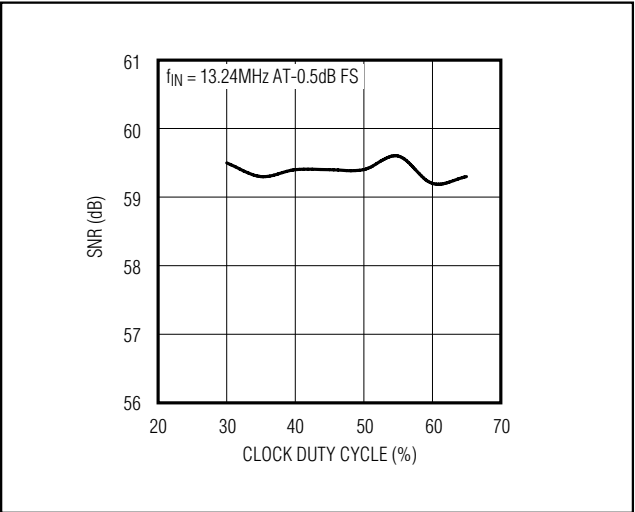


Figure 3b. Signal-to-Noise Ratio vs. Clock Duty Cycle (Differential Input)

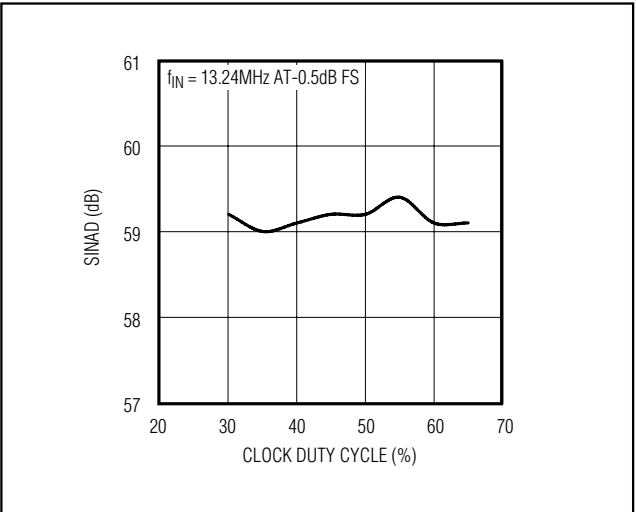


Figure 4b. Signal-to-Noise Plus Distortion vs. Clock Duty Cycle (Differential Input)

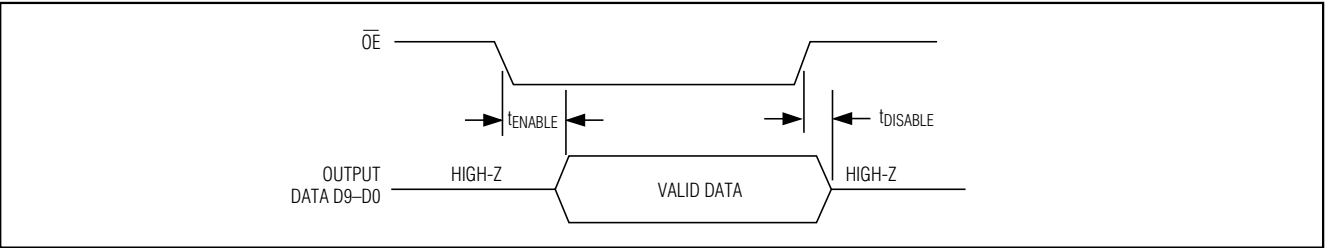


Figure 5. Output Enable Timing

# 10-Bit, 40MSPS, +3.0V, Low-Power ADC with Internal Reference

## System Timing Requirements

Figure 6 shows the relationship between the clock input, analog input, and data output. The MAX1444 samples at the falling edge of the input clock. Output data is valid on the rising edge of the input clock. The output data has an internal latency of 5.5 clock cycles. The output data has an internal latency of 5.5 clock cycles. Figure 6 also shows the relationship between the input clock parameters and the valid output data.

## Applications Information

Figure 7 shows a typical application circuit containing a single-ended to differential converter. The internal reference provides a  $V_{DD}/2$  output voltage for level shifting purposes. The input is buffered and then split to a voltage follower and inverter. A lowpass filter follows the op amps to suppress some of the wideband noise associated with high-speed op amps. The user may select the  $R_{ISO}$  and  $C_{IN}$  values to optimize the filter performance to suit a particular application. For the application in Figure 7, an  $R_{ISO}$  of  $50\Omega$  is placed before the capacitive load to prevent ringing and oscillation. The 22pF  $C_{IN}$  capacitor acts as a small bypassing capacitor.

## Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution for converting a single-ended source signal to a fully differential signal, required by the MAX1444 for optimum performance. Connecting the transformer's center tap to COM provides a  $V_{DD}/2$  DC level shift to the input. Although a 1:1 transformer is shown, a step-

up transformer may be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, may also improve the overall distortion.

In general, the MAX1444 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for very high input frequencies. In differential input mode, even-order harmonics are lower since both inputs ( $IN+$ ,  $IN-$ ) are balanced, and each of the inputs only requires half the signal swing compared to single-ended mode.

## Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application. The MAX4108 op amp provides high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

## Grounding, Bypassing, and Board Layout

The MAX1444 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass  $V_{DD}$ , REFP, REFN, and COM with two parallel 0.1 $\mu$ F ceramic capacitors and a 2.2 $\mu$ F bipolar capacitor to GND. Follow the same rules to bypass the digital supply ( $OV_{DD}$ ) to OGND. Multilayer boards with separated ground and power planes pro-

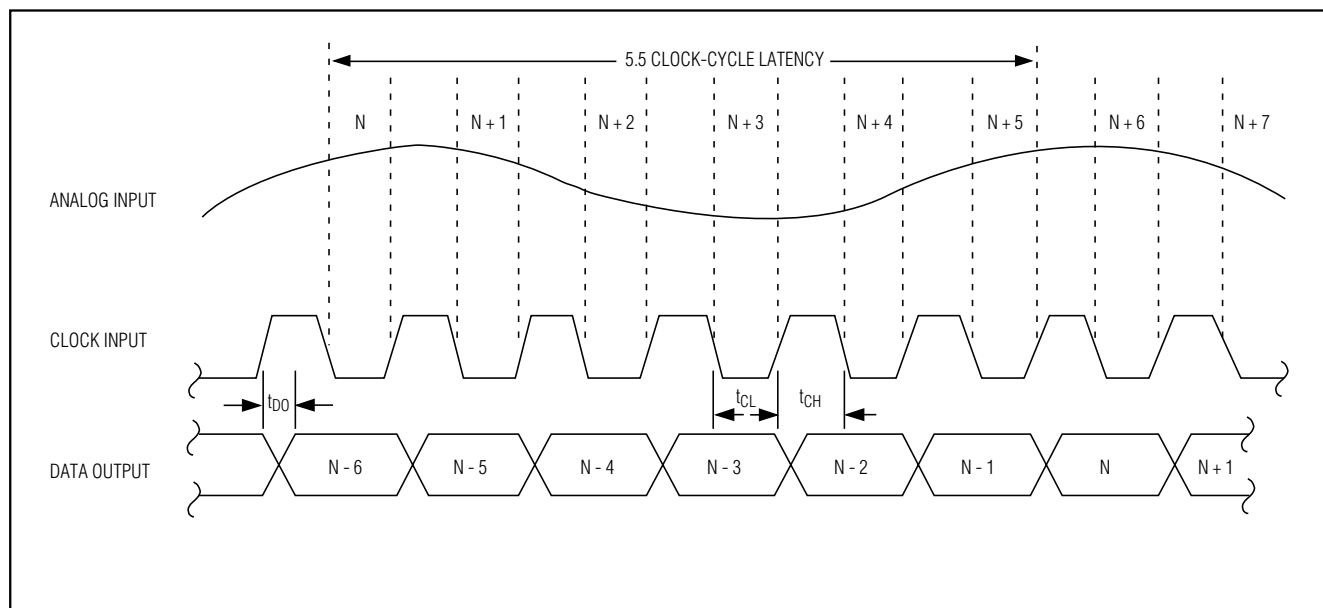


Figure 6. System and Output Timing Diagram

# 10-Bit, 40MSPS, +3.0V, Low-Power ADC with Internal Reference

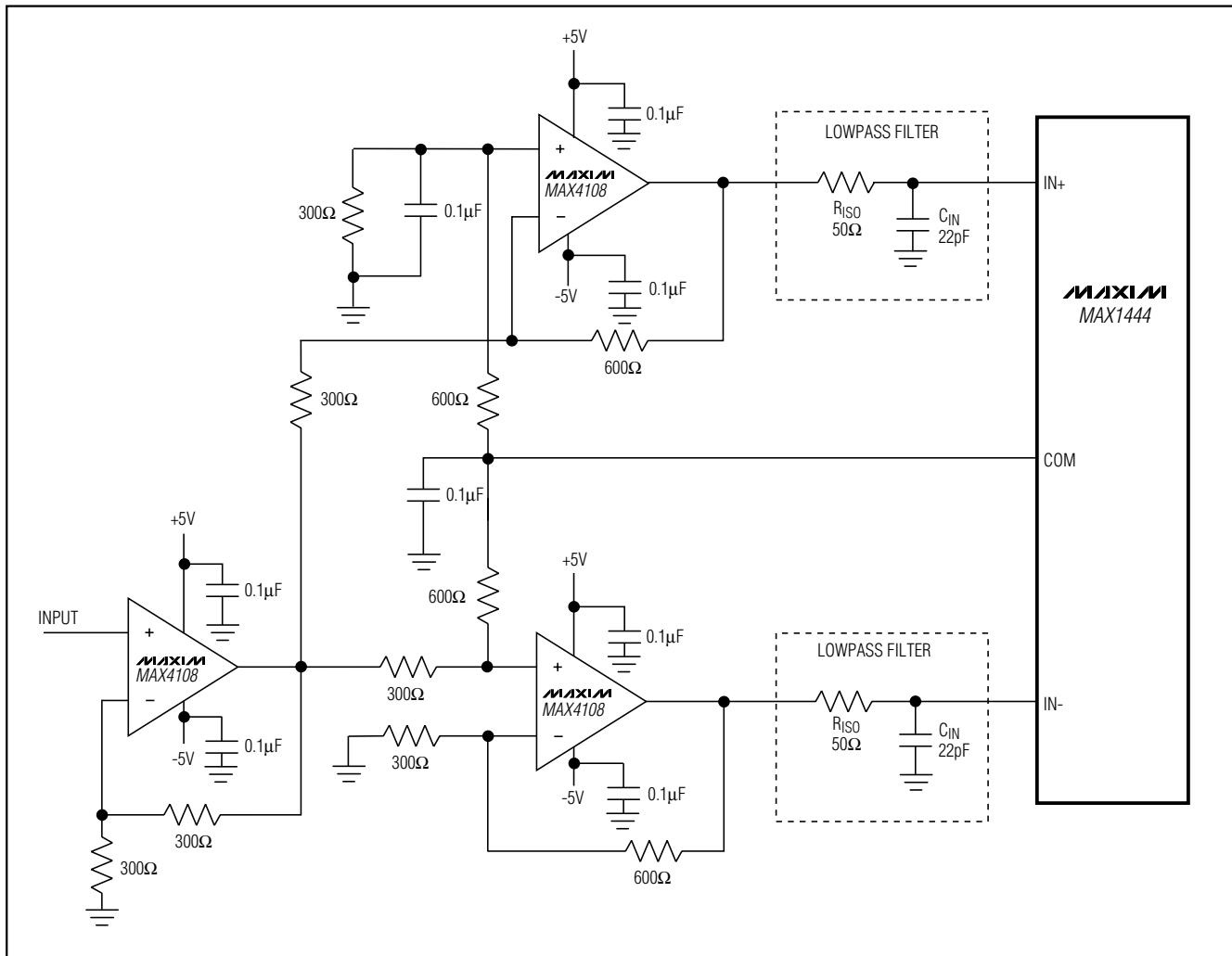


Figure 7. Typical Application Circuit for Single-Ended to Differential Conversion

duce the highest level of signal integrity. Consider using a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package.

The two ground planes should be joined at a single point so that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally at a point along the gap between the two ground planes that produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all

ground pins could share the same ground plane if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from sensitive analog traces. Keep all signal lines short and free of 90° turns.

# 10-Bit, 40Mbps, +3.0V, Low-Power ADC with Internal Reference

MAX1444

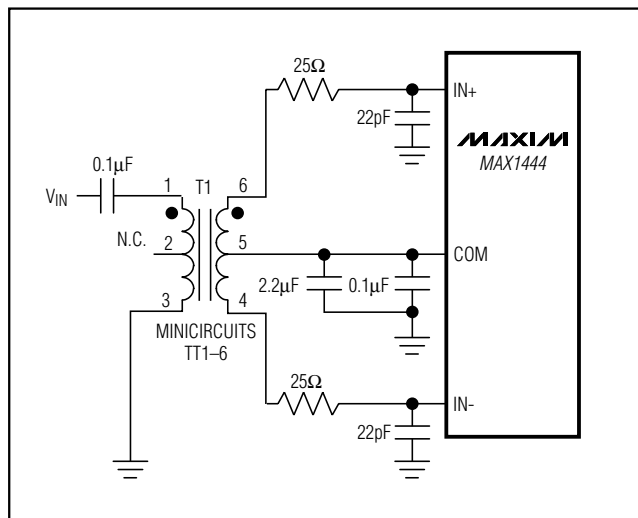


Figure 8. Using a Transformer for AC Coupling

## Static Parameter Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. The MAX1444's static linearity parameters are measured using the best straight-line fit method.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

## Dynamic Parameter Definitions

### Aperture Jitter

Figure 10 depicts the aperture jitter ( $t_{AJ}$ ), which is the sample-to-sample variation in the aperture delay.

### Aperture Delay

Aperture delay ( $t_{AD}$ ) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 10).

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum A/D noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

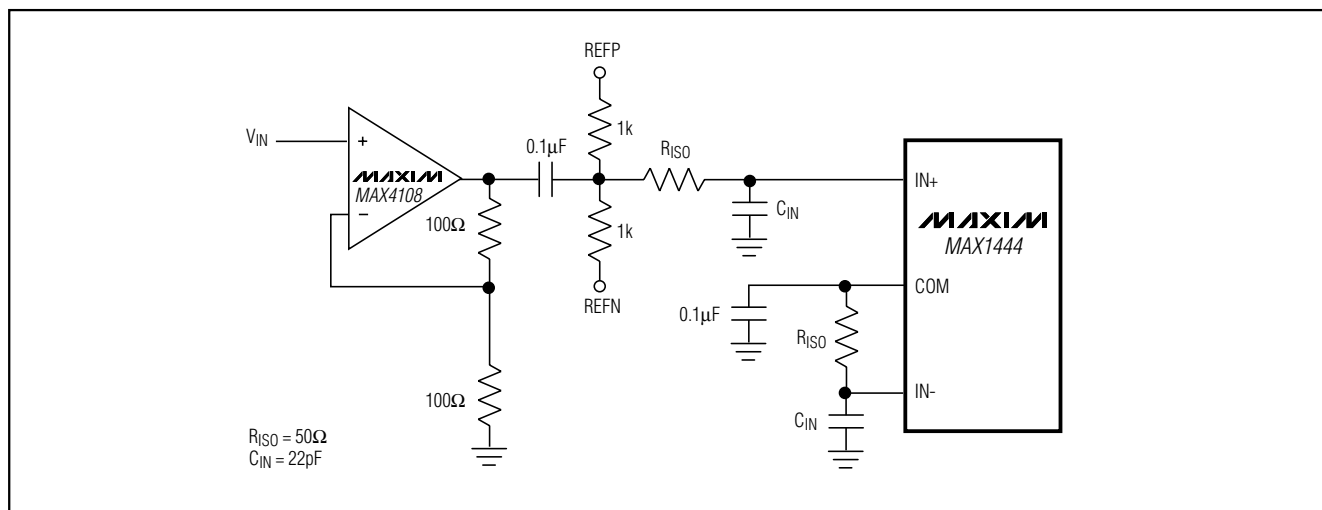


Figure 9. Single-Ended AC-Coupled Input

# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

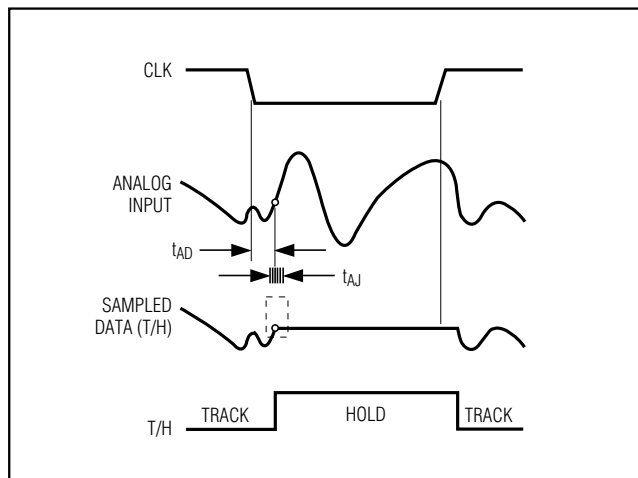


Figure 10. T/H Aperture Timing

## Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

## Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is computed from:

$$\text{ENOB} = (\text{SINAD} - 1.76\text{dB}) / 6.02\text{dB}$$

$$\text{THD} = 20 \times \log \left( \sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2} / V_1 \right)$$

## Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

where  $V_1$  is the fundamental amplitude, and  $V_2$  through  $V_5$  are the amplitudes of the 2nd- through 5th-order harmonics.

## Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

## Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale, and their envelope is at -0.5dB full scale.

## Chip Information

TRANSISTOR COUNT: 5684

PROCESS: CMOS



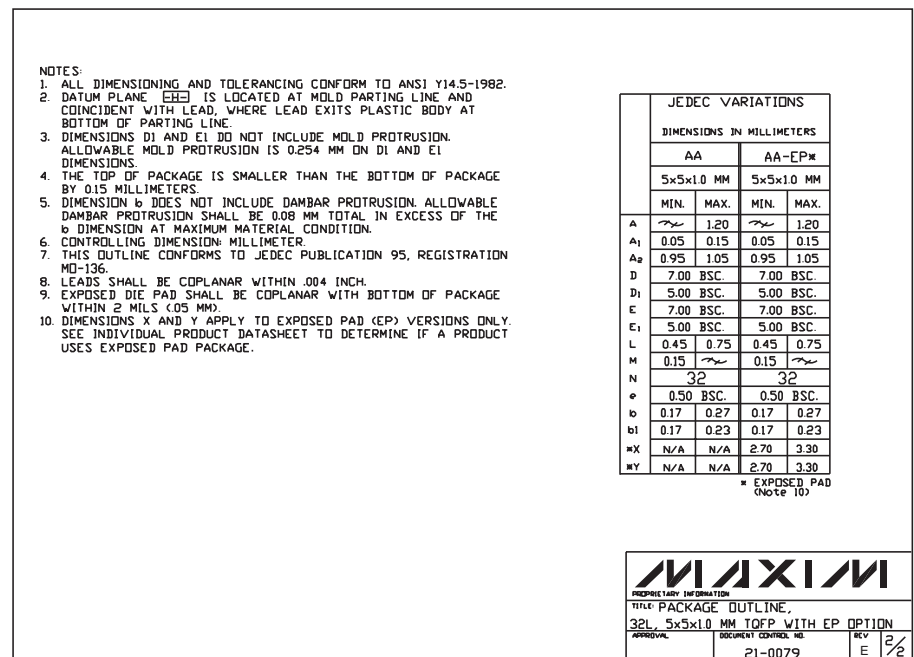
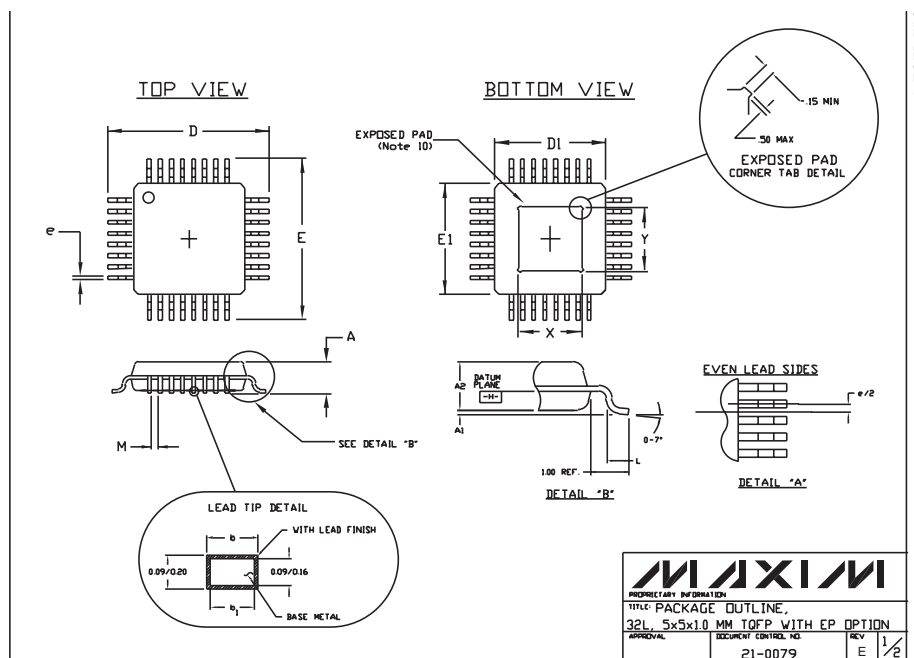
# MAX1444

The block diagram of the MAX1444 shows the following internal components and connections:

- CONTROL**: Receives CLK and manages the T/H, PIPELINE ADC, and OUTPUT DRIVERS.
- T/H (Track-and-Hold)**: Receives IN+ and IN- signals and outputs to the PIPELINE ADC.
- PIPELINE ADC**: Receives signals from the T/H and the REF SYSTEM + BIAS, and outputs to the DEC.
- DEC (Decoder)**: Receives signals from the PIPELINE ADC and outputs to the OUTPUT DRIVERS.
- OUTPUT DRIVERS**: Receives signals from the DEC and outputs D9-D0. It is also connected to OE.
- REF SYSTEM + BIAS**: Receives PD and provides a reference signal to the PIPELINE ADC. It is connected to REFOUT, REFIN, REFP, COM, and REFN.
- Power Connections**: VDD, GND, OVDD, and OGND are shown on the right side of the block.

# 10-Bit, 40Mps, +3.0V, Low-Power ADC with Internal Reference

## Package Information



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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