19-2694; Rev 0; 12/02

MAXIM

MAX3740 Evaluation Kit

Evaluates: MAX3740

General Description

The MAX3740 evaluation kit (EV kit) is an assembled demonstration board that provides complete optical and electrical evaluation of the MAX3740 VCSEL driver.

The EV kit has an electrical section and an optical section. The output of the electrical evaluation section is interfaced to an SMA connector, which can be connected to a 50Ω terminated oscilloscope. The optical section of the evaluation board is populated with a DS1858 digital potentiometer and allows evaluation of the MAX3740 in an SFP layout. With slight modifications, a common-cathode VCSEL also can be evaluated using the electrical side of the EV kit.

Features

- ♦ **Fully Assembled and Tested**
- ♦ **Single +3.3V Power-Supply Operation**
- ♦ **Allows Optical and Electrical Evaluation**
- ♦ **Allows Evaluation with DS1858 in SFP Layout**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX3740EVKIT	-40°C to +85°C	24 QFN

Electrical Evaluation Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C5, C9, C13, C15, C16, C17	8	0.1µF ±10% ceramic capacitors (0402)
C3	1	0.047µF ±10% ceramic capacitor (0402)
C4, C6, C7, C8, C11, C12	6	0.01µF ±10% ceramic capacitors (0402)
C10	1	Open
C14	1	10µF ±10% ceramic capacitor (0805)
C18	1	10µF ±10% tantalum capacitor, case B
D1	1	VCSEL laser and photodiode*
D2	1	LED, red T1 package
L1, L2, L3	3	600Ω ferrite beads (0603) Murata BLM18HD102SN1
L4	1	1µH inductor (1008CS) Coilcraft 1008CS-102XKBC
R1, R2	2	10kΩ potentiometers
R3	1	350Ω resistor (0402)
R4	1	2.49kΩ resistor (0402)
R5, R12	2	499Ω resistors (0402)
R6, R13	2	10kΩ resistors (0402)
R7	1	0Ω resistor (0402)*
R8	1	4.7kΩ resistor (0402)
R9, R11	2	49.9Ω resistors (0402)
R10, R26, R27, R34, R35, R36	6	Open
R14	1	20kΩ potentiometer
R15	1	50kΩ potentiometer
R16	1	500kΩ potentiometer
Q1, Q2	2	NPN transistors (SOT23) Zetex FMMT491A
Q3	1	MOSFET (SOT23) Zetex BS170F
JU1–JU8, JU10	9	2-pin headers, 0.1in centers
J1–J7	7	SMA connectors, round contacts
TP1–TP11, TP20, TP21	13	Test points
U1	1	MAX3740ETG (24 QFN)
U2	1	MAX495ESA (8 SO)
None	9	Shunts
None	1	MAX3740 EV board
None	1	MAX3740 data sheet

**These components are not supplied but can be populated if the user wants to test the VCSEL with the electrical side of the EV kit.*

Optical Evaluation Component List

DESIGNATION	QTY	DESCRIPTION
C19	1	0.01µF ±10% ceramic capacitor (0402)
C20, C25, C27	3	0.1µF ±10% ceramic capacitors (0402)
C21	1	10µF ±10% tantalum capacitor, case B
C22	1	0.047µF ±10% ceramic capacitor (0402)
C23, C26, C28, C29	4	0.01µF ±10% ceramic capacitors (0201)
C30	1	Open
J9, J10	2	SMA connectors, round contacts
JU9	1	2-pin header, 0.1in center
L5	1	1µH inductor (1008CS) Coilcraft 1008CS-102XKBC
L6	1	600Ω ferrite bead (0603) Murata BLM18HD102SN1
R17, R18, R28	3	4.7kΩ resistors (0603)
R21, R22, R23, R33	4	Open
R24	1	350Ω resistor (0201)
R25	1	1.7kΩ resistor (0201)
R29, R30	2	0Ω resistors (0201)
R31	1	49.9Ω resistor (0402)
R32	1	20kΩ resistor (0402)
TP13–TP19, TP22, TP23	9	Test points
U3	1	MAX3740ETG (24-pin QFN)
U4	1	DS1858 (16-pin BGA, 1.5mm pitch)

Component Suppliers

SUPPLIER	PHONE	FAX
AVX	803-946-0690	803-626-3123
Coilcraft	847-639-6400	847-639-1469
Murata	814-237-1431	814-238-0490
Zetex	516-543-7100	516-864-7630

Quick Start

Electrical Evaluation

In the electrical configuration, an automatic power-control (APC) test circuit is included to emulate a semiconductor laser with a monitor photodiode. Monitor diode current is provided by transistor Q1, which is controlled by an operational amplifier (U2). The APC test circuit, consisting of U2 and Q1, applies the simulated monitor diode current to the MD pin of the MAX3740. To ensure proper operation in the electrical configuration, set up the evaluation board as follows:

1) Place shunts on JU4–JU8 and JU10 (see the *Adjustment and Control Descriptions* section for details).
2) Remove shunts JU1 and JU2.
3) To enable the outputs, connect TX_DISABLE to GND by placing a shunt on JU3.

   Note: When performing the following resistance checks, autoranging DMMs may forward bias the on-chip ESD protection and cause inaccurate measurements. To avoid this problem, manually set the DMM to a high range.
4) Adjust R15, the $R_{BIASSET}$ potentiometer, for 1.7kΩ resistance between TP4 (BIASSET) and ground.
5) Adjust R1, the R_{PWRSET} potentiometer, for 10kΩ resistance between TP2 (REF) and pin 1 (MD) of JU2.
6) Adjust R14, the $R_{PEAKSET}$ potentiometer, for 20kΩ resistance between TP10 (PEAKSET) and ground to disable peaking.
7) Adjust R16, the RTC potentiometer, for 0Ω resistance between TP7 (TC1) and TP8 (TC2) to disable temperature compensation.
8) Adjust R2, the R_{MODSET} potentiometer, for 10kΩ resistance between TP9 (MODSET) and ground.
9) Apply a differential input signal (250mV$_{P-P}$ to 2200mV$_{P-P}$) between SMA connectors J5 and J7 (IN+ and IN-).
10) Attach a high-speed oscilloscope with a 50Ω input to SMA connector J6 (OUT).
11) Connect a +3.3V supply between TP20 (VCC) and TP21 (GND). Adjust the power supply until the voltage between TP11 and ground is +3.3V.
12) Adjust R1 (R_{PWRSET}) until the desired laser bias current is achieved.

$$I_{BIAS} = \frac{V_{PIN1\_JU5}}{49.9\Omega}$$

13) The MD and BIAS currents can be monitored at TP1 (V_{PWRMON}) and TP3 ($V_{BIASMON}$) using the equations below:

$$I_{MD} = \frac{V_{PWRMON}}{2 \times R_{PWRSET}}$$

$$I_{BIAS} = \frac{9 \times V_{BIASMON}}{350\Omega}$$

Note: If the voltage at TP1 exceeds V_{PMTH} (0.8V typ) or TP3 exceeds V_{BMTH} (0.8V typ), the FAULT signal is asserted and latched.

14) Adjust R2 until the desired laser modulation current is achieved.

$$I_{MOD} = \frac{\text{Signal Amplitude (V)}}{50\Omega}$$

15) Adjust R14 ($R_{PEAKSET}$) until the desired amount of peaking is achieved.

Optical Evaluation with Mechanical Potentiometers

For optical evaluation of the MAX3740, configure the evaluation kit as follows:

1) Place shunts on JU2, JU6, JU7, JU8, and JU10 (see the *Adjustment and Control Descriptions* section).
2) Remove components L2 and C9. Remove the shunts from JU1, JU4, and JU5.
3) Install a 0Ω resistor at R7 to connect the anode of the VCSEL to the output.
4) To enable the outputs, connect TX_DISABLE to GND by placing a shunt on JU3.
5) Connect a common-cathode VCSEL as shown in Figure 1. Keep leads short to reduce reflection.

   Note: When performing the following resistance checks, autoranging DMMs may forward bias the on-chip ESD protection and cause inaccurate measurements. To avoid this problem, manually set the DMM to a high range.
6) Adjust R15, the $R_{BIASSET}$ potentiometer, for 1.7kΩ resistance between TP4 (BIASSET) and ground.
7) Adjust R1, the R_{PWRSET} potentiometer, for 10kΩ resistance between TP2 (REF) and pin 1 (MD) of JU2.
8) Adjust R14, the $R_{PEAKSET}$ potentiometer, for 20kΩ resistance between TP10 (PEAKSET) and ground to disable peaking.
9) Adjust R16, the R_{TC} potentiometer, for 0Ω resistance between TP7 (TC1) and TP8 (TC2), to disable temperature compensation.
10) Adjust R2, the R_{MODSET} potentiometer, for 10kΩ resistance between TP9 (MODSET) and ground.
11) Apply a differential input signal (250mV_{P-P} to 2200mV_{P-P}) between SMA connectors J5 and J7 (IN+ and IN-).
12) Attach the VCSEL fiber connector to an optical/electrical converter.
13) Connect a +3.3V supply between TP20 (VCC) and TP21 (GND). Adjust the power supply until the voltage between TP11 and ground is +3.3V.
14) Adjust R1 (R_{PWRSET}) until desired average optical power is achieved.
15) The MD and BIAS currents can be monitored at TP1 (V_{PWRMON}) and TP3 ($V_{BIASMON}$) using the following equations:

$$I_{MD} = \frac{V_{PWRMON}}{2 \times R_{PWRSET}}$$

$$I_{BIAS} = \frac{9 \times V_{BIASMON}}{350\Omega}$$

Note: If the voltage at TP1 exceeds V_{PMTH} (0.8V typ) or TP3 exceeds V_{BMTH} (0.8V typ), the FAULT signal is asserted and latched.

16) Adjust R2 (R_{MODSET}) until the desired optical amplitude is achieved. Optical amplitude can be observed on an oscilloscope connected to an optical/electrical converter. VCSEL overshoot and ringing can be improved by appropriate selection of R10 and C10, as described in the *Design Procedure* section of the MAX3740 data sheet.
17) To improve the falling edge of a VCSEL, adjust R14 ($R_{PEAKSET}$).

Optical Evaluation Using the DS1858 Digital Potentiometer with Monitors

The MAX3740 optical evaluation side is similar to an SFP transmitter. In this configuration, R_{MODSET} and R_{PWRSET} are provided by the DS1858 digital potentiometer. The DS1858 also monitors the PWRMON and BIASMON outputs of the MAX3740. Control for the DS1858 is provided through a two-wire interface at TP14 (MOD-DEF2) and TP15 (MOD-DEF1). For control of the digital potentiometer, refer to the DS1858 data sheet.

1) To enable the outputs, connect TX_DISABLE to GND by placing a shunt on JU9.
2) Connect a common-cathode VCSEL as shown in Figure 2. Keep the leads short to reduce reflection.
3) Apply a differential input signal (250mV$_{P-P}$ to 2200mV$_{P-P}$) between SMA connectors J9 and J10 (IN+ and IN-).
4) Attach the VCSEL fiber connector to an optical/electrical converter.
5) Connect a +3.3V supply between TP22 (VCCT) and TP23 (GND). Adjust the power supply until the voltage between TP13 and ground is +3.3V.
6) Adjust the R_{PWRSET} resistor using the DS1858 until desired average optical power is achieved. Refer to the DS1858 data sheet for control instructions.
7) The MD and BIAS currents can be monitored through the DS1858 (refer to DS1858 data sheet), or at TP16 (V_{PWRMON}) and TP17 ($V_{BIASMON}$) using the following equations:

$$I_{MD} = \frac{V_{PWRMON}}{2 \times R_{PWRSET}}$$

$$I_{BIAS} = \frac{9 \times V_{BIASMON}}{350\Omega}$$

Note: If the voltage at TP16 exceeds V_{PMTH} (0.8V typ) or TP17 exceeds V_{BMTH} (0.8V typ), the FAULT signal is asserted and latched.

8) Adjust the R_{MODSET} resistor using the DS1858 until the desired optical amplitude is achieved. Optical amplitude can be observed on an oscilloscope connected to an optical/electrical converter. Refer to the DS1858 data sheet for control instructions.
9) If needed, change the value of $R_{PEAKSET}$ (R32) to improve the falling edge of the VCSEL.

Adjustment and Control Descriptions (see Quick Start)

COMPONENT	NAME	FUNCTION
D2	Fault Indicator	The LED is illuminated when a fault condition has occurred (refer to the *Detailed Description* section of the MAX3740 data sheet).
JU1	COMP	Enables/disables the APC circuit. Remove the shunt to enable the APC circuit.
JU2	PHOTODIODE	Installing a shunt connects the photodiode of the VCSEL to the MD pin. Used when a VCSEL is installed.
JU3, JU9	TX_DISABLE	Enable/disable the output currents. Install a shunt to enable output currents.
JU4	IPD	Determines the gain of the photodiode emulator. When JU4 is open, the gain is 0.02A/A. When JU4 is shunted, the gain is 0.12A/A.
JU5	APCOPEN	Installing a shunt connects the electrical output of the part to the emulation circuit.
JU6	FAULT	Installing a shunt enables the external fault-indicator circuit.
JU7	SQUELCH	Installing a shunt enables the squelch function.
JU8	POWER	Installing a shunt enables power to the part.
JU10	VCCEXT	Installing a shunt provides power to the emulation and fault-indicator circuits.
R1	R_{PWRSET}	Adjusts transmit optical power to be maintained by the APC loop.
R2	R_{MODSET}	Adjusts the laser modulation current.
R14	$R_{PEAKSET}$	Adjusts the peaking for the falling edge of the VCSEL.
R15	$R_{BIASSET}$	In a closed-loop configuration, adjusts the maximum bias current available to the APC. In an open-loop configuration, adjusts the bias level of the output.
R16	R_{TC}	Adjusts the temperature compensation of the modulation current.
TP14	MOD-DEF2	Part of the two-wire interface for the DS1858. Refer to the DS1858 data sheet.
TP15	MOD-DEF1	Part of the two-wire interface for the DS1858. Refer to the DS1858 data sheet.

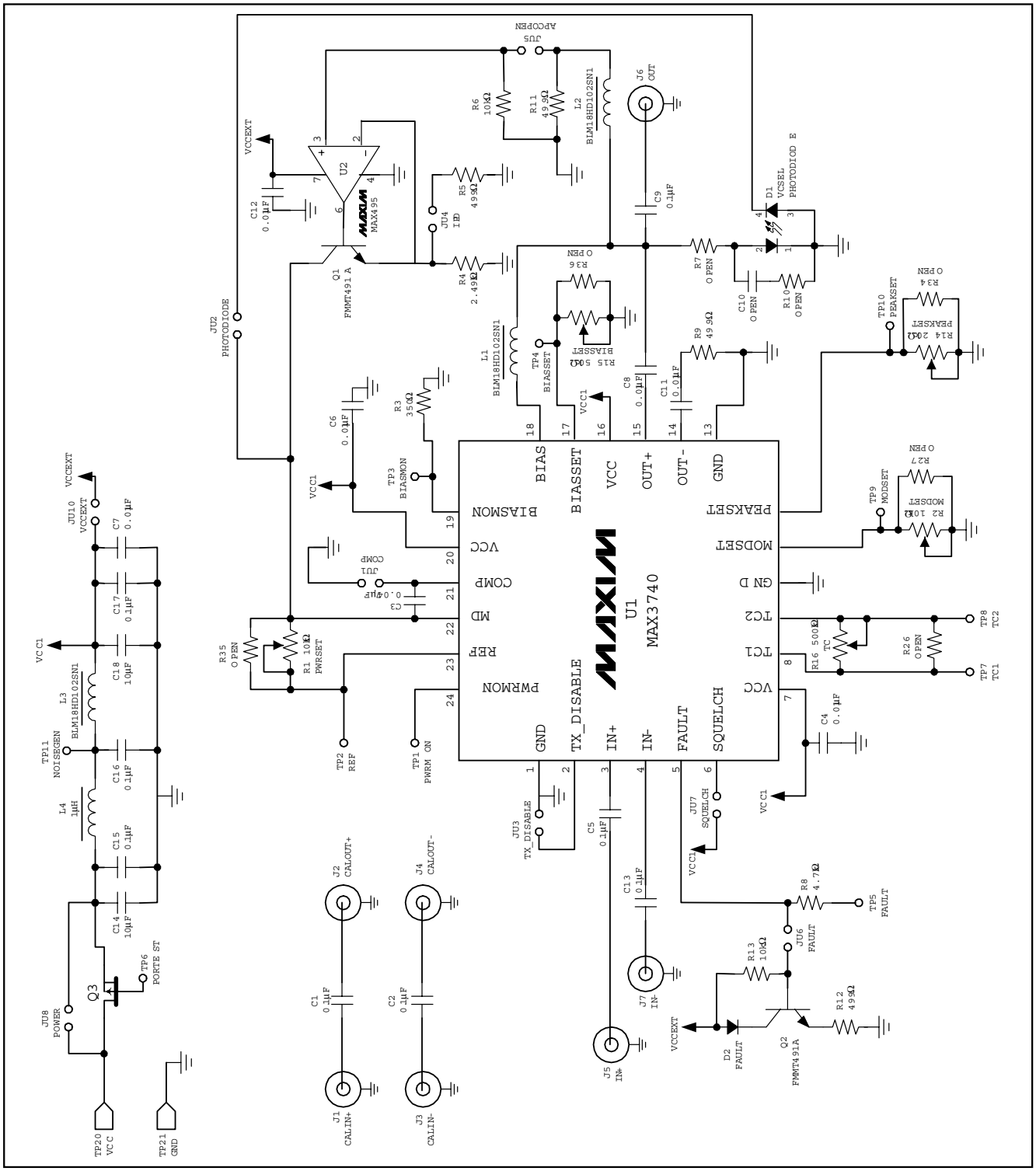

Figure 1. MAX3740 EV Kit Electrical Schematic

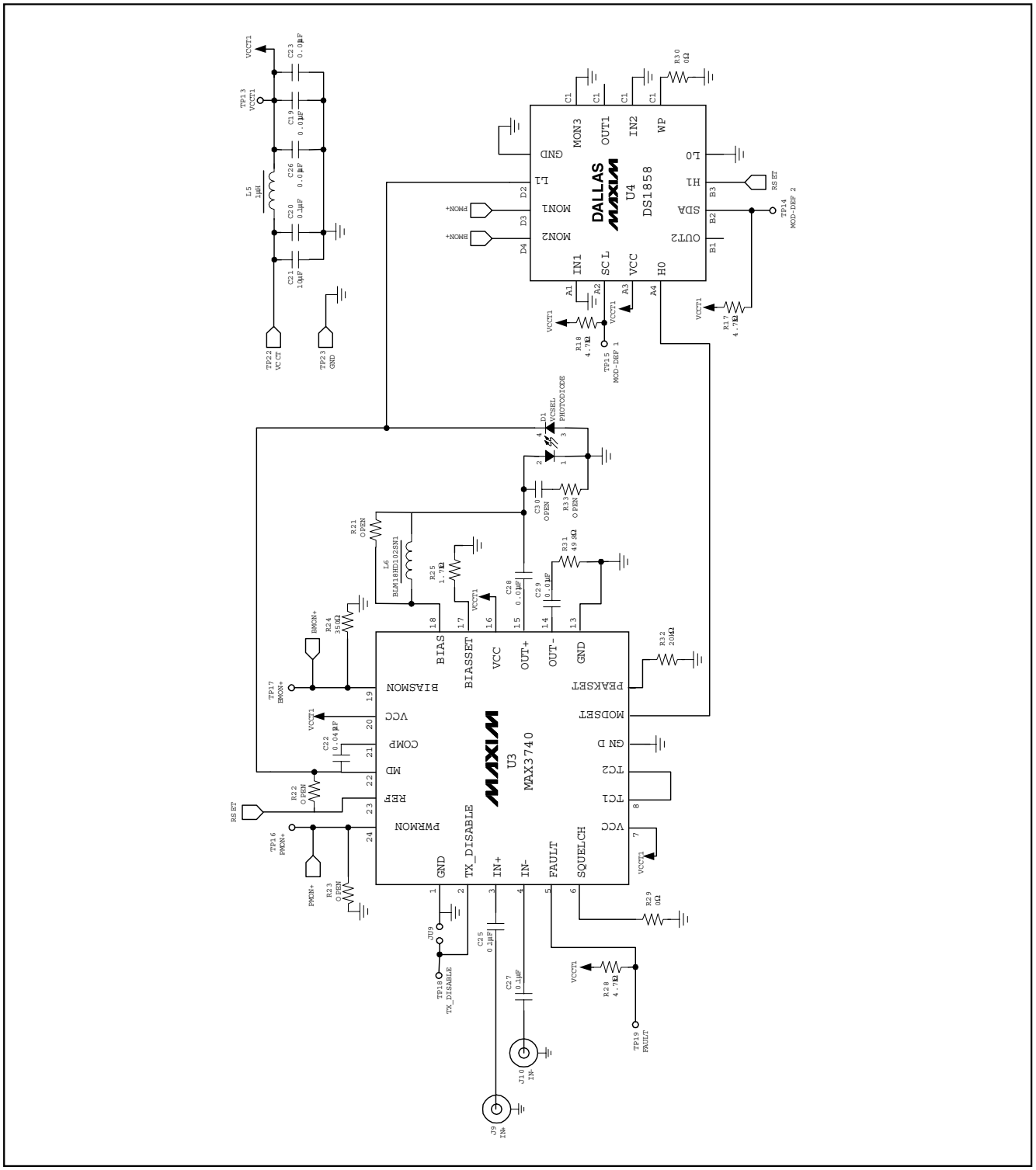

Figure 2. MAX3740 EV Kit Optical Schematic with DS1858

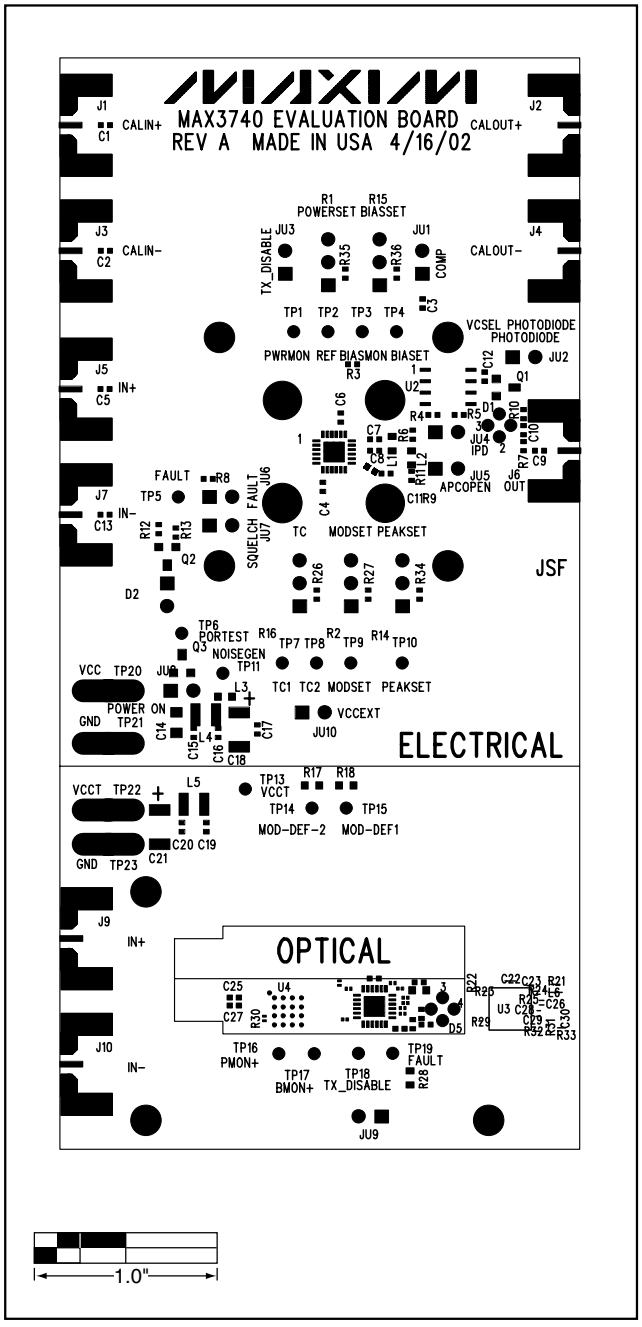

Figure 3. MAX3740 EV Kit Component Placement Guide—Component Side

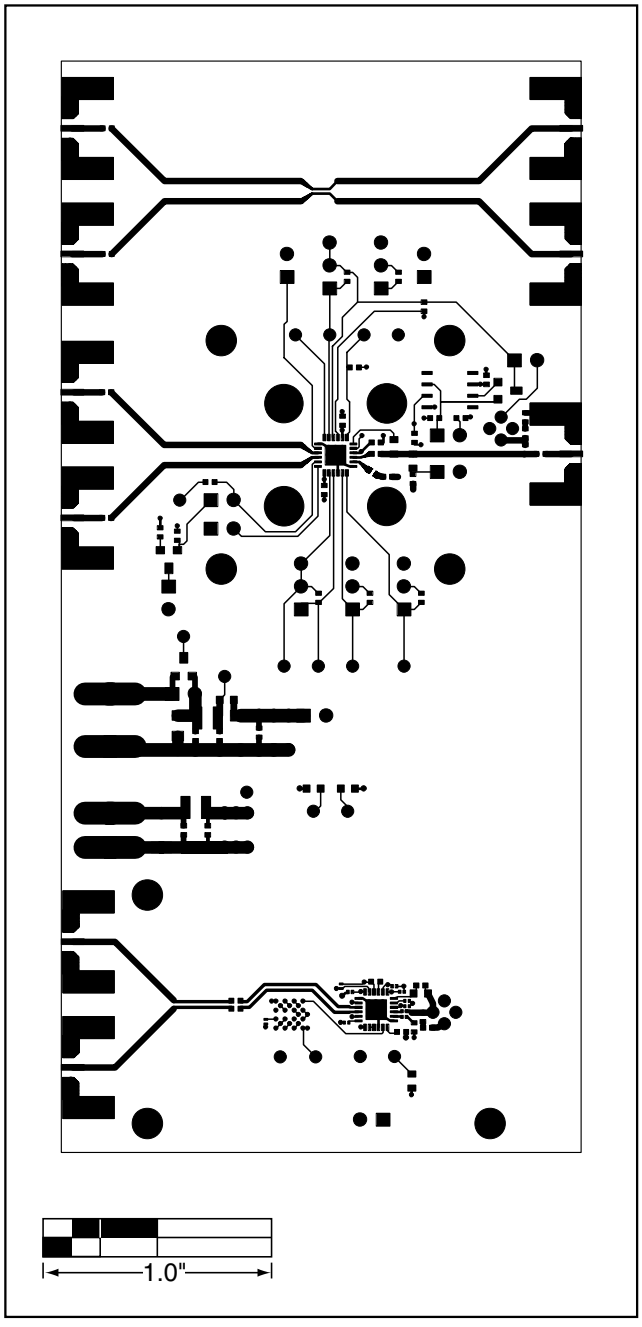

Figure 4. MAX3740 EV Kit PC Board Layout—Component Side

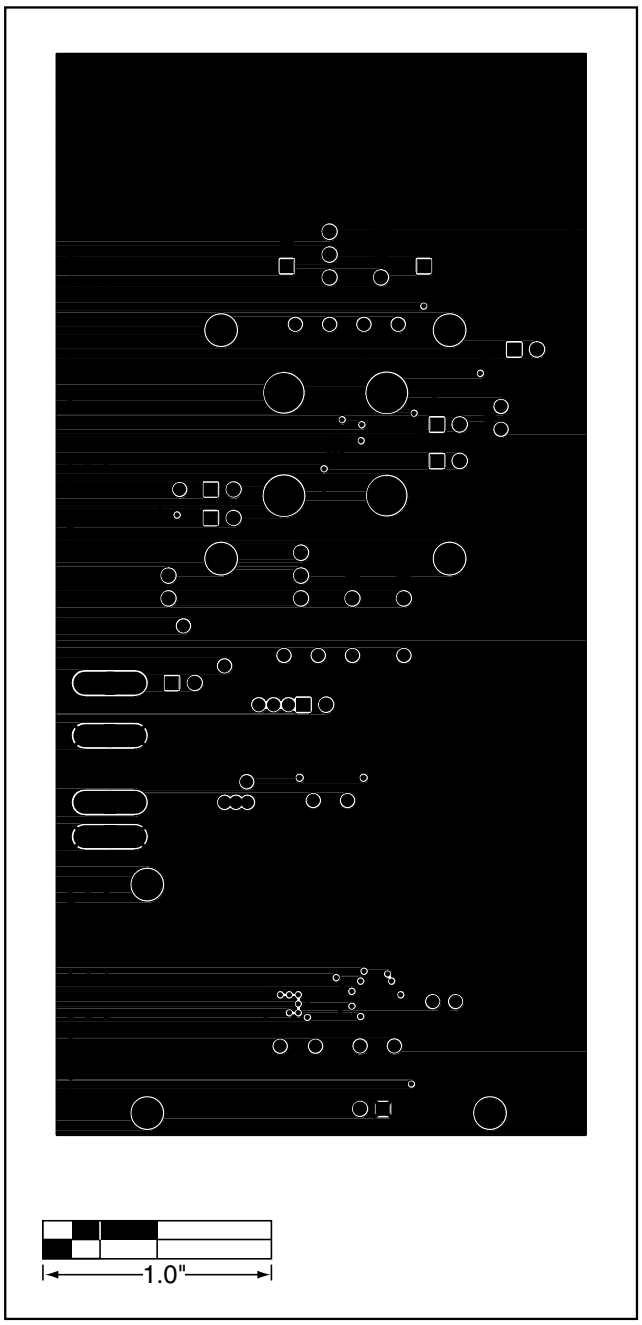

Figure 5. MAX3740 EV Kit PC Board Layout—Ground Plane

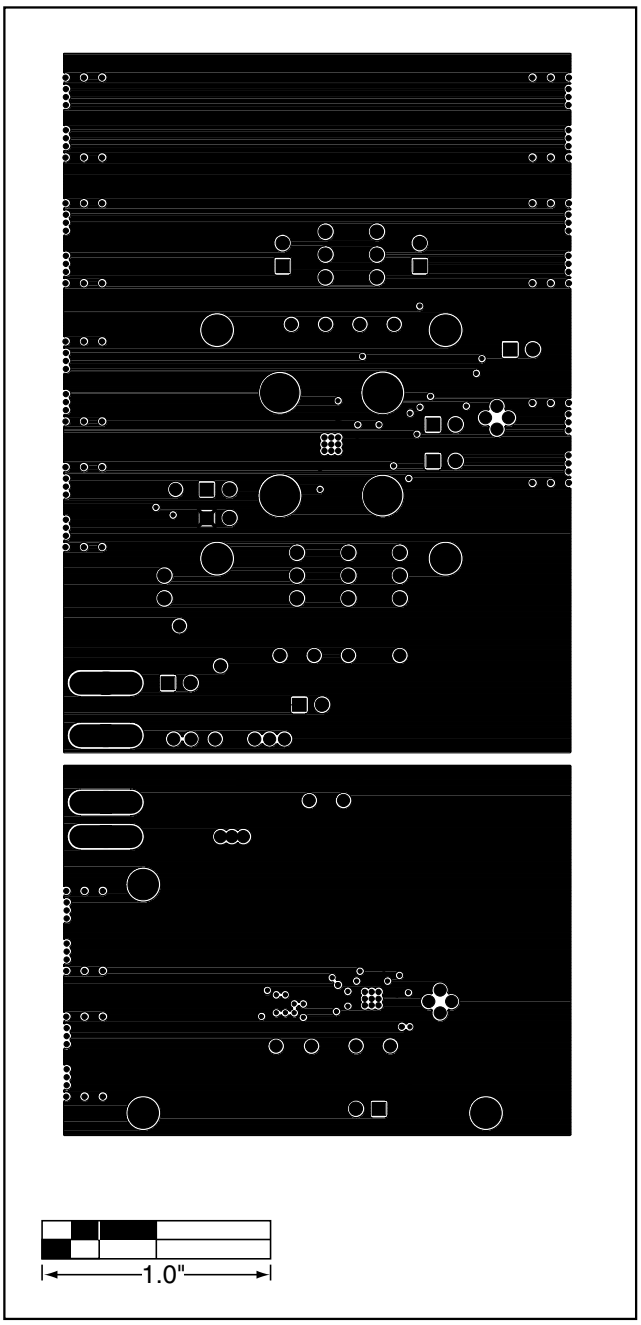

Figure 6. MAX3740 EV Kit PC Board Layout—Power Plane

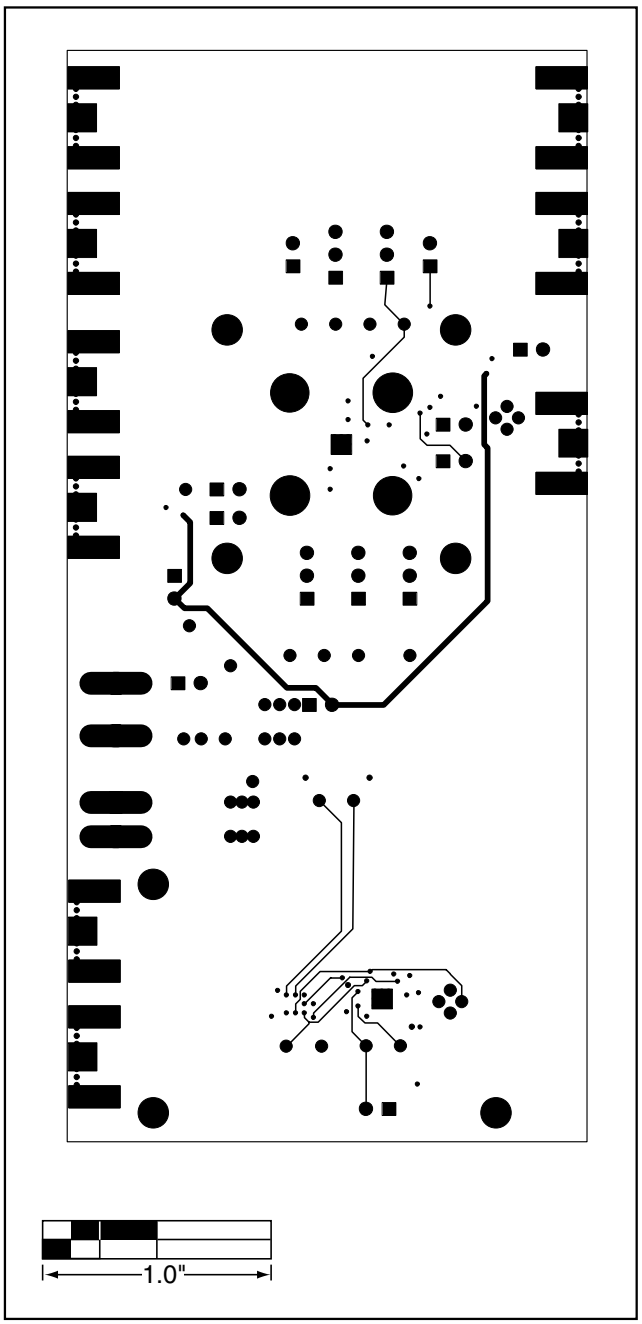

Figure 7. MAX3740 EV Kit PC Board Layout—Solder Side