19-2577; Rev 0; 9/02

MAXIM

Low-Power, Compact 2.5Gbps/2.7Gbps Clock-Recovery and Data-Retiming IC

General Description

The MAX3873A is a compact, low-power 2.488Gbps/2.67Gbps clock-recovery and data-retiming IC for SDH/SONET applications. The phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input. The input data is then retimed by this recovered clock, providing a clean data output. The MAX3873A meets all SDH/SONET jitter specifications, does not require an external reference clock to aid in frequency acquisition, and provides excellent tolerance to both deterministic and sinusoidal jitter. The MAX3873A provides a PLL loss-of-lock ($\overline{LOL}$) output to indicate whether the CDR is in lock. The recovered data and clock outputs are CML with on-chip 50Ω back terminations on each line. The clock output can be powered down if not used.

The MAX3873A is implemented in Maxim's second-generation SiGe process and consumes only 260mW at 3.3V supply (output clock disabled, low output swing). The device is available in a 4mm x 4mm 20-pin QFN exposed-pad package and operates from -40°C to +85°C.

Applications

Switch Matrix Backplanes

SDH/SONET Receivers and Regenerators

Add/Drop Multiplexers

Digital Cross-Connects

SDH/SONET Test Equipment

DWDM Transmission Systems

Typical Application Circuit appears at end of data sheet.

Features

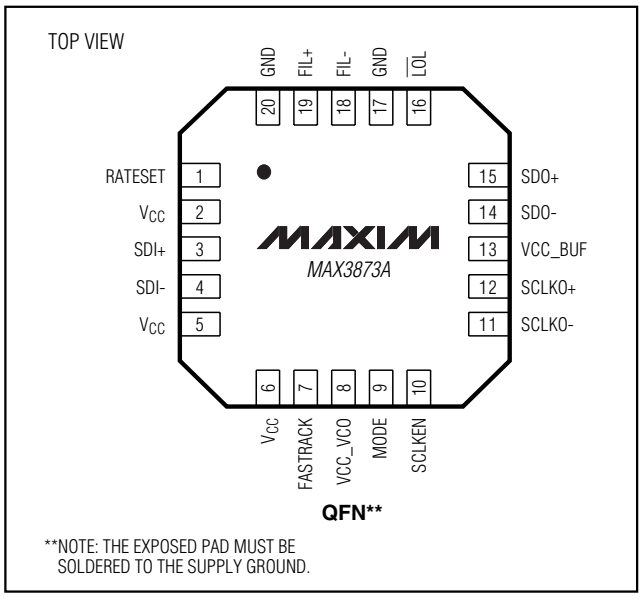
- **Fully Integrated Clock Recovery and Data Retiming**
- **Power Dissipation: 260mW with +3.3V Supply**
- **Clock Jitter Generation: 5mUI$_{RMS}$**
- **Exceeds ANSI, ITU, and Bellcore SDH/SONET Jitter Specifications**
- **Differential Input Range: 50mV$_{P-P}$ to 1.6V$_{P-P}$**
- **Single +3.3V Power Supply**
- **PLL Fast Track (FASTRACK) Mode Available**
- **Clock Output Can Be Disabled**
- **Input Data Rate: 2.488Gbps or 2.67Gbps**
- **Selectable Output Amplitude**
- **Tolerates 2000 Consecutive Identical Digits**
- **Loss-of-Lock Indicator**
- **Differential CML Data and Clock Outputs**
- **Operating Temperature Range: -40°C to +85°C**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3873AEGP	-40°C to +85°C	20 QFN-EP* (4mm × 4mm)

**EP = exposed pad.*

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +5.0V
Voltage at SDI± ..... (V_{CC} - 1.0V) to (V_{CC} + 0.5V)
CML Output Current at SDO±, SCLKO± 22mA
Voltage at $\overline{LOL}$, FASTRACK, FIL±, SCLKEN
MODE, RATESET.....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
20-Lead QFN (derate 20.0mW/°C above +85°C).....1300mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-50°C to +150°C
Processing Temperature.....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, T_A = -40°C to +85°C. Typical values are at 2.488Gbps, V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 2)	I_{CC}	MODE = GND, SCLKEN = low		79	99	mA
		MODE = OPEN, SCLKEN = high		112	142	
CML INPUT SPECIFICATIONS (SDI+, SDI-)						
Differential Input Voltage	V_{ID}	Figure 1	50		1600	mV_{P-P}
Single-Ended Input Voltage	V_{IS}	Figure 1	V_{CC} - 0.8		V_{CC} + 0.4	V
Input Common-Mode Voltage		DC-coupled, Figure 1	V_{CC} - V_{ID}/4			V
Input Termination to V_{CC}	R_{IN}		40	50	60	Ω
CML OUTPUT SPECIFICATIONS (SDO+, SDO-, SCLKO+, SCLKO-)						
Differential Output Swing (Note 3)		MODE = open	640	800	1000	mV_{P-P}
		MODE = V_{CC}	400	600	800	
		MODE = GND	200	400	600	
Differential Output Resistance	R_O		80	100	120	Ω
Output Common-Mode Voltage (Note 3)		MODE = Open		V_{CC} - 0.17		V
		MODE = V_{CC}		V_{CC} - 0.13		
		MODE = GND		V_{CC} - 0.08		
TTL INPUT/OUTPUT SPECIFICATIONS (FASTRACK, LOL, SCLKEN, MODE, RATESET)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current			-30		+30	µA
Output High Voltage	V_{OH}	I_{OH} = sourcing 40µA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = sinking 2mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, C_F = 0.022µF, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, 2.488Gbps, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Input Data Rate		RATESET = low			2.488		Gbps
		RATESET = high			2.67		
Clock-to-Q Delay	t_{CLK-Q}	Figure 2 (Note 5)		-70		+70	ps
Jitter Peaking	J_P	f ≤ 2MHz				0.1	dB
Jitter Transfer Bandwidth	J_{BW}	RATESET = Low				2.0	MHz
Sinusoidal Jitter Tolerance		(Notes 6, 8)	f = 70kHz, 0.4UI deterministic jitter on input data		6.9		UI_{P-P}
			f = 100kHz, 0.4UI deterministic jitter on input data	2.12	4.5		
			f = 1MHz, 0.4UI deterministic jitter on input data	0.33	0.6		
			f = 10MHz, 0.4UI deterministic jitter on input data	0.15	0.3		
		(Notes 6, 9)	f = 70kHz, 0.4UI deterministic jitter on input data		6.9		
			f = 100kHz, 0.4UI deterministic jitter on input data	2.12	4.5		
			f = 1MHz, 0.4UI deterministic jitter on input data	0.33	0.6		
			f = 10MHz, 0.37UI deterministic jitter on input data	0.15	0.3		
Jitter Generation	J_{GEN}	(Notes 7, 8)			5	6.8	mUI_{RMS}
					45	62	mUI_{P-P}
		(Notes 7, 9)			6	7.65	mUI_{RMS}
					40	86	mUI_{P-P}
Clock Output Edge Speed		20% to 80%			60	110	ps
Data Output Edge Speed		20% to 80%			60	110	ps
Tolerated Consecutive Identical Digits					2000		bits
SDI± Input Return Loss (-20log(|S_{11}|))		100kHz to 2.5GHz			17		dB
		2.5GHz to 4.0GHz			14		
Frequency Acquisition Time		Figure 4			1		ms
$\overline{LOL}$ Assert Time		Figure 4			1.6		µs

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, C_F = 0.022µF, T_A = -40°C to +85°C. Typical values are at V_{CC} = 3.3V, 2.488Gbps, T_A = +25°C, unless otherwise noted.) (Note 4)

Note 1: At T_A = -40°C, DC characteristics are guaranteed by design and characterization.
Note 2: CML outputs open.
Note 3: R_L = 50Ω to V_{CC}.
Note 4: AC characteristics are guaranteed by design and characterization.
Note 5: Relative to the falling edge of SCLKO+. See Figure 2.
Note 6: Measured with 2^{23} - 1 PRBS.
Note 7: Jitter BW = 12kHz to 20MHz.
Note 8: RATESET = low.
Note 9: RATESET = high.

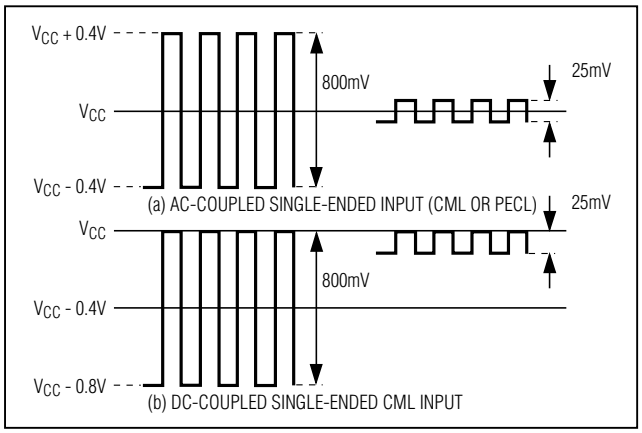


Figure 1. Definition of Input Voltage Swing

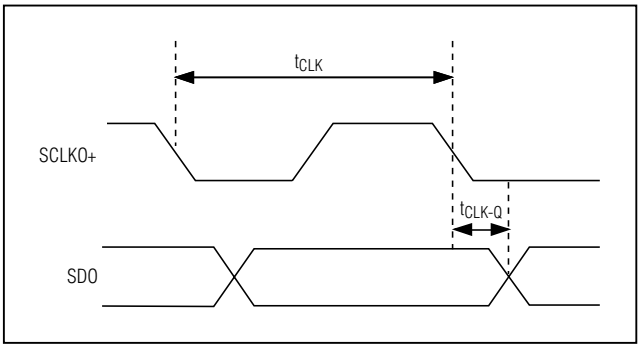


Figure 2. Definition of Clock-to-Q Delay

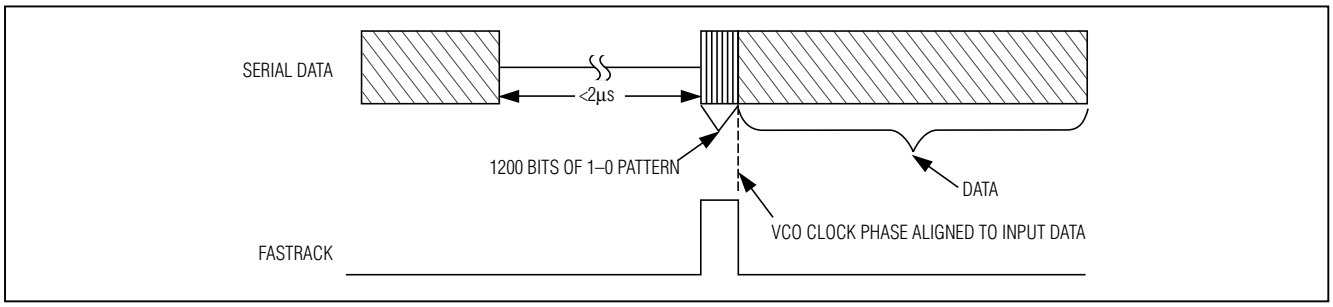


Figure 3. Definition of Phase Acquisition Time

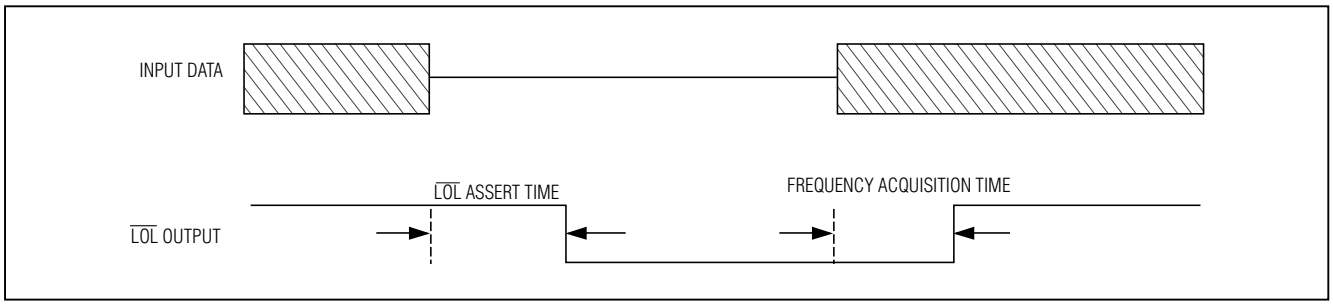


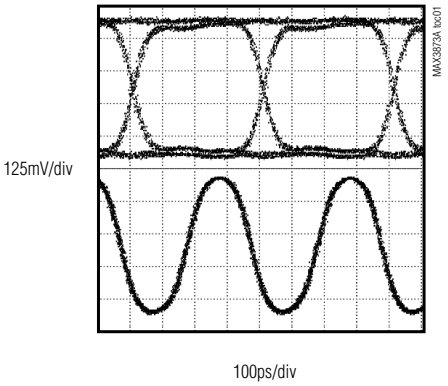
Figure 4. Definition of $\overline{LOL}$ Assert Time and Frequency Acquisition Time

Low-Power, Compact 2.5Gbps or 2.7Gbps Clock-Recovery and Data-Retiming IC

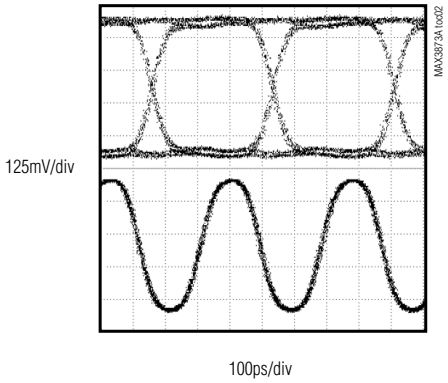
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

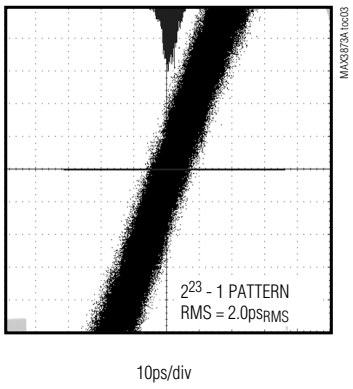
RECOVERED CLOCK AND DATA (2.488Gbps, 2^{23} - 1 PATTERN, V_{IN} = 50mV_{P-P})



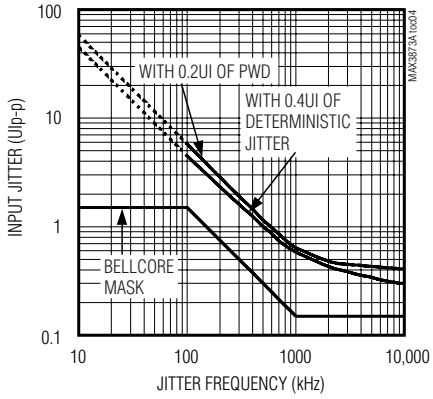
RECOVERED CLOCK AND DATA (2.67Gbps, 2^{23} - 1 PATTERN, V_{IN} = 50mV_{P-P})



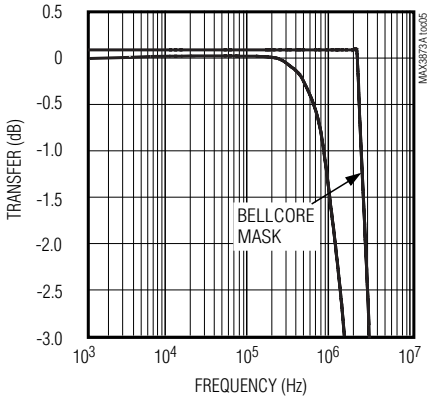
RECOVERED CLOCK JITTER (2.488Gbps)



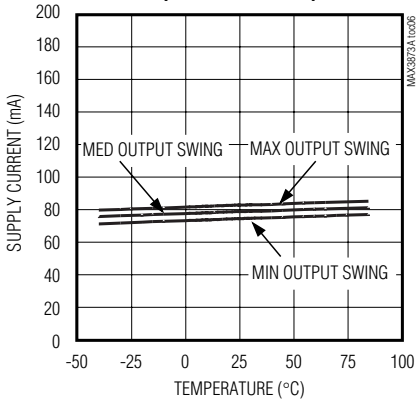
JITTER TOLERANCE (2.488Gbps, 2^{23} - 1 PATTERN, V_{IN} = 50mV_{P-P})



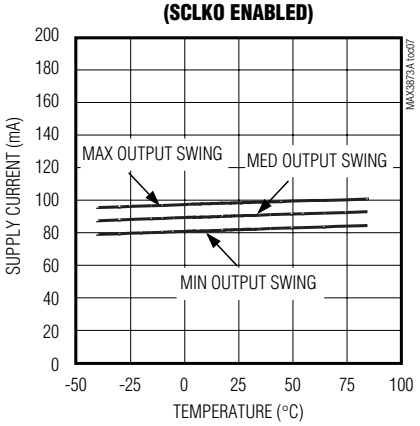
JITTER TRANSFER



SUPPLY CURRENT vs. TEMPERATURE (SCLKO DISABLED)



SUPPLY CURRENT vs. TEMPERATURE (SCLKO ENABLED)



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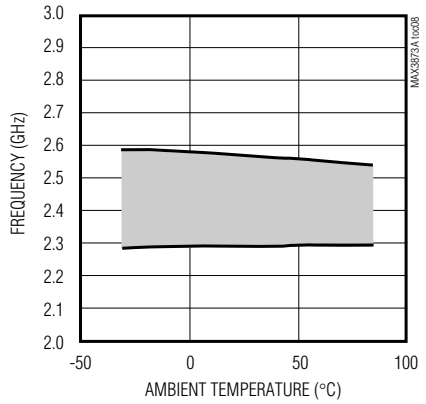
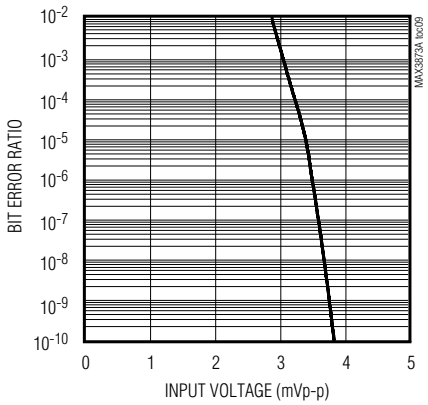
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

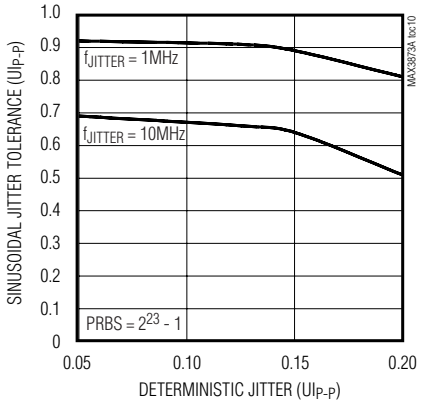
PULLIN RANGE (RATESET = 0)



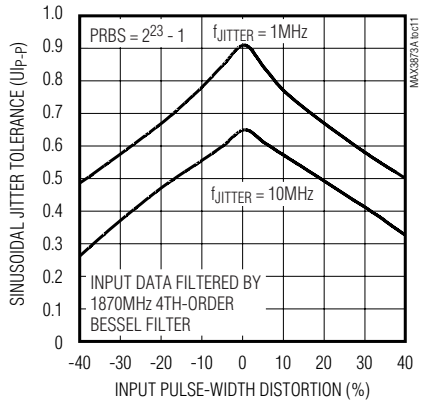
BIT-ERROR RATIO vs. INPUT AMPLITUDE



JITTER TOLERANCE vs. INPUT DETERMINISTIC JITTER



JITTER TOLERANCE vs. PULSE-WIDTH DISTORTION



Pin Description

PIN	NAME	FUNCTION
1	RATESET	Input Rate Select. Connect to TTL low for 2.488Gbps data and to TTL high for 2.67Gbps data.
2, 5, 6	V_{CC}	3.3V Supply Voltage
3	SDI+	Positive Serial Data Input
4	SDI-	Negative Serial Data Input
7	FASTRACK	PLL Fast Track Control, TTL Input. When FASTRACK is TTL high, the PLL is switched to a fast-track mode for fast phase acquisition. When FASTRACK is TTL low, the PLL operates normally.
8	VCC_VCO	3.3V VCO Supply Voltage
9	MODE	Output Amplitude Mode Select. MODE = open sets the CML output amplitude to high; MODE = high sets the output amplitude to medium; MODE = low sets the output amplitude to low.

Pin Description (continued)

PIN	NAME	FUNCTION
10	SCLKEN	Clock Output Enable, TTL Input. When SCLKEN = open or SCLKEN = high, the clock outputs (SCLKO±) are enabled. When SCLKEN = low, the clock outputs are disabled and SCLKO± = V_{CC}.
11	SCLKO-	Negative Clock Output, CML. This output can be disabled by setting SCLKEN to low.
12	SCLKO+	Positive Clock Output, CML. This output can be disabled by setting SCLKEN to low.
13	VCC_BUF	3.3V CML Output Buffer Supply Voltage
14	SDO-	Negative Data Output, CML
15	SDO+	Positive Data Output, CML
16	$\overline{LOL}$	Loss-of-Lock Output, TTL (Active Low). The $\overline{LOL}$ output indicates a PLL lock failure.
17, 20	GND	Supply Ground
18	FIL-	Negative PLL Loop Filter Connection. Connect a 0.022µF capacitor between FIL+ and FIL-.
19	FIL+	Positive PLL Loop Filter Connection. Connect a 0.022µF capacitor between FIL+ and FIL-.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper electrical and thermal operation.

Detailed Description

The MAX3873A consists of a fully integrated phase-locked loop (PLL), input amplifier, and CML output buffers (Figure 5). The PLL consists of a phase/frequency detector, a loop filter, and a voltage-controlled oscillator (VCO).

This device is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques.

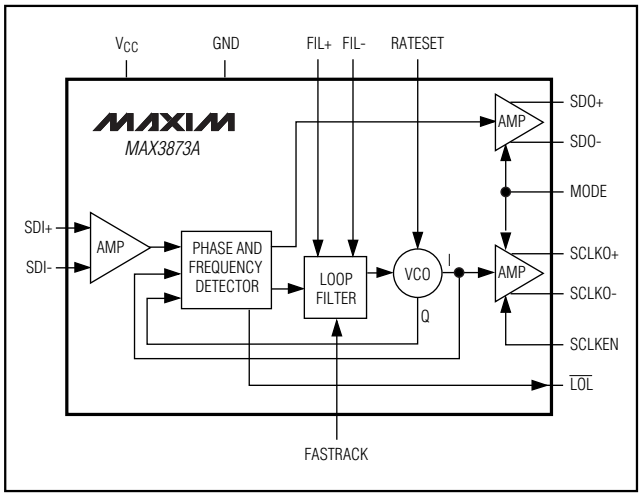


Figure 5. Functional Diagram

Input Amplifier

The input amplifier provides internal 50Ω line terminations and can accept a differential input amplitude from 50mV$_{P-P}$ to 1600mV$_{P-P}$. The structure of the input amplifier is shown in Figure 9.

Phase Detector

The phase detector incorporated in the MAX3873A produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming.

Frequency Detector

The digital frequency detector (FD) aids frequency acquisition during startup conditions. The frequency difference between the received data and the VCO clock is derived by sampling the VCO outputs on each edge of the data input signal. The FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state.

Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. An external capacitor, C_F, is required to set the PLL damping ratio. See the *Design Procedure* section for guidelines on selecting this capacitor.

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The loop filter output controls the on-chip LC VCO running at either 2.488GHz or 2.67GHz. The VCO provides low phase noise and is trimmed to the correct frequency. Clock jitter generation is typically $2ps_{RMS}$ within a jitter band of 12kHz to 20MHz.

Loss-of-Lock Monitor

A loss-of-lock ($\overline{LOL}$) monitor is incorporated in the MAX3873A to indicate either a loss of frequency lock or the absence of incoming data. Under loss-of-lock conditions, $\overline{LOL}$ may momentarily assert high due to noise.

Design Procedure

Setting the Loop Filter

The MAX3873A is designed for both regenerator and receiver applications. Its fully integrated PLL is a classic second-order feedback system, with a loop bandwidth (J_{BW}) below 2.0MHz. The external capacitor, C_F, can be adjusted to set the loop damping. Figures 6 and 7 show the open-loop and closed-loop transfer functions. The PLL zero frequency, f_Z, is a function of external capacitor C_F and can be approximated according to:

$$f_Z = \frac{1}{2\pi\,(3000\Omega)\,C_F}$$

with C_F expressed in F.

For an overdamped system, the jitter peaking (J_P) of a second-order system can be approximated by:

$$J_P = 20\log\left(1 + \frac{f_Z}{J_{BW}}\right)$$

For example, using C_F = 2000pF results in jitter peaking of 0.2dB. Reducing C_F below 500pF might result in PLL instability. The recommended value is C_F = 0.022µF to guarantee a maximum jitter peaking of less than 0.1dB. C_F must be a low TC, high-quality capacitor of type X7R or better.

FASTRACK Mode

The MAX3873A has a PLL fast-track (FASTRACK) mode to decrease locking time in switched data applications. In applications where the input data is switched from one source to another, there is a brief period in which there is no valid data input to the MAX3873A. In the absence of input data, the PLL phase slowly drifts from the ideal position. By enabling FASTRACK during reacquisition, the time required to regain phase alignment is reduced. This is accomplished by increasing the loop bandwidth by approximately 50%.

The bandwidth of the MAX3873A is also linearly dependent upon the transition density of the input data. By using a preamble of 1200 bits of a 1–0 pattern during switching, the loop bandwidth is increased by a factor of approximately 2 (Figure 3). Thus, by using a 1–0 pattern preamble and enabling FASTRACK, the PLL bandwidth is increased by a factor of approximately 3, resulting in the fastest possible reacquisition of phase lock.

FASTRACK increases the rate at which the MAX3873A acquires the proper phase, assuming that the VCO is already running at the proper frequency. On startup conditions, however, the VCO frequency is significantly different from the input data, and the time required to lock to the incoming data is increased to approximately 1.0ms.

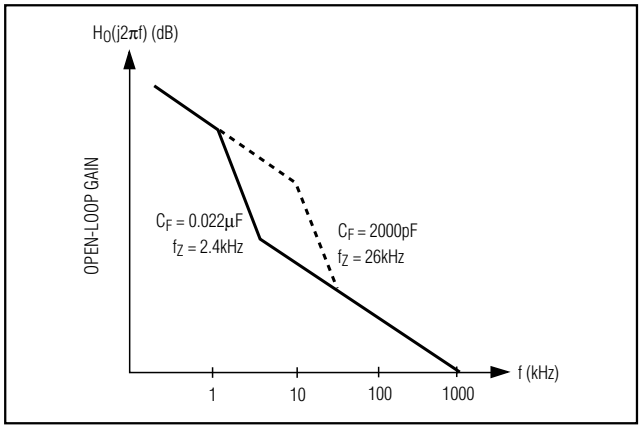

Figure 6. Open-Loop Transfer Function

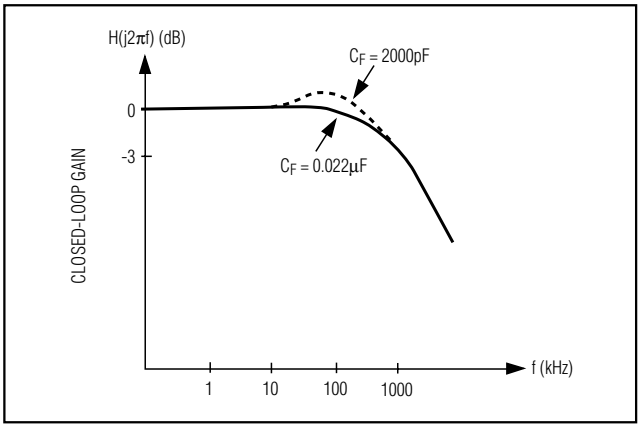

Figure 7. Closed-Loop Transfer Function

Sinusoidal Jitter Tolerance and Input Deterministic Jitter Trade-Offs

The MAX3873A has excellent jitter tolerance. Adding DJ to the input will close the eye opening and result in reduced sinusoidal jitter tolerance. It typically can tolerate more than $0.3UI_{P-P}$ of 10MHz jitter when measured with a 2^{23} - 1 PRBS data stream with 0.4UI of deterministic jitter (DJ). This gives a total high-frequency jitter tolerance of 0.7UI. Refer to the Jitter Tolerance vs. Pulse-Width Distortion and Jitter Tolerance vs. Deterministic Jitter graphs in the *Typical Operating Characteristics* section.

Input and Output Terminations

The MAX3873A's digital CML outputs (SDO+, SDO-, SCLKO+, SCLKO-) have selectable output amplitude controlled by the MODE input. If the SCLKO outputs are not used, they can be disabled (see the Supply Current vs. Temperature graph in the *Typical Operating Characteristics* section).

The structure of the high-speed digital outputs is shown in Figure 8. The MODE input sets the current in the current source, thereby controlling the output swing. The SCLKEN input sets the current in the SCLKO current source to 0mA, disabling the output.

The structure of the CML inputs (SDI±) is shown in Figure 9. Unless the CML input is DC-coupled to a CML output, use AC-coupling with the CML inputs to avoid upsetting the common-mode voltage.

Applications Information

Consecutive Identical Digits (CID)

The MAX3873A has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER of less than 10^{-10}. The CID tolerance is tested using a 2^{13} - 1 PRBS, substituting a long run of zeros to simulate the worst case. A CID tolerance of 2000 bits is typical.

Exposed-Pad Package

The exposed-pad (EP), 20-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3873A and must be soldered to the circuit board for proper thermal and electrical performance.

Layout

Circuit board layout and design can significantly affect the MAX3873A's performance. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data and clock signals. Place power-supply decoupling as close to the V_{CC} pins as possible. Isolate the input from the output signals to reduce feedthrough.

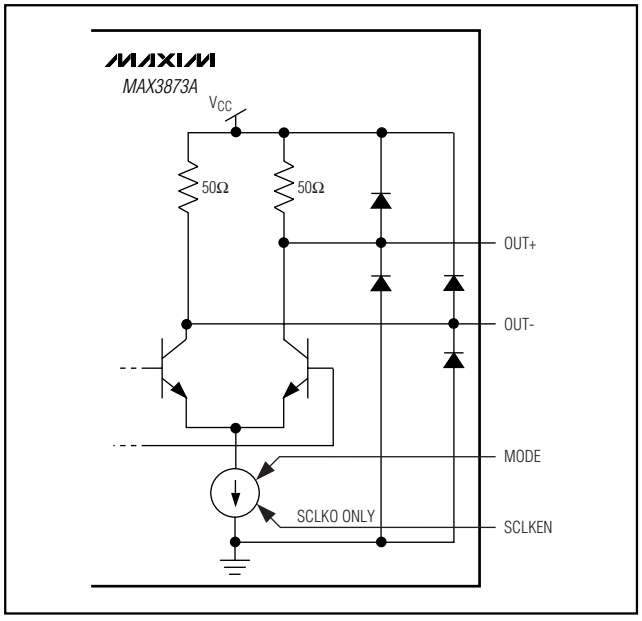

Figure 8. CML Output Model

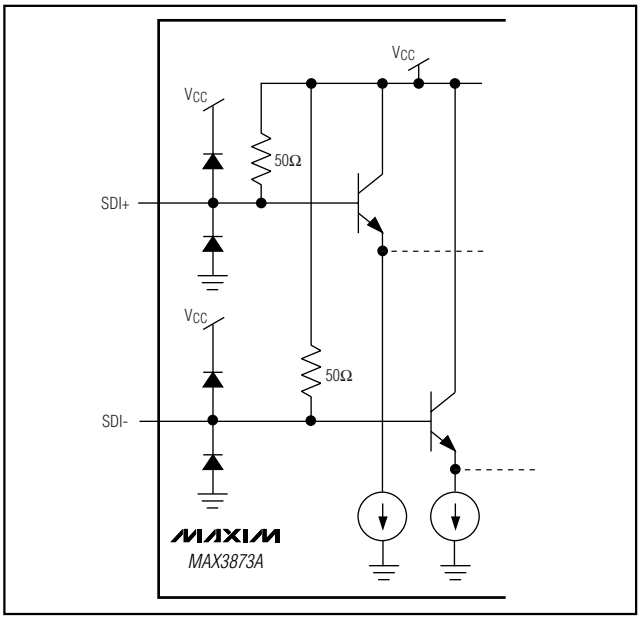

Figure 9. CML Input Model

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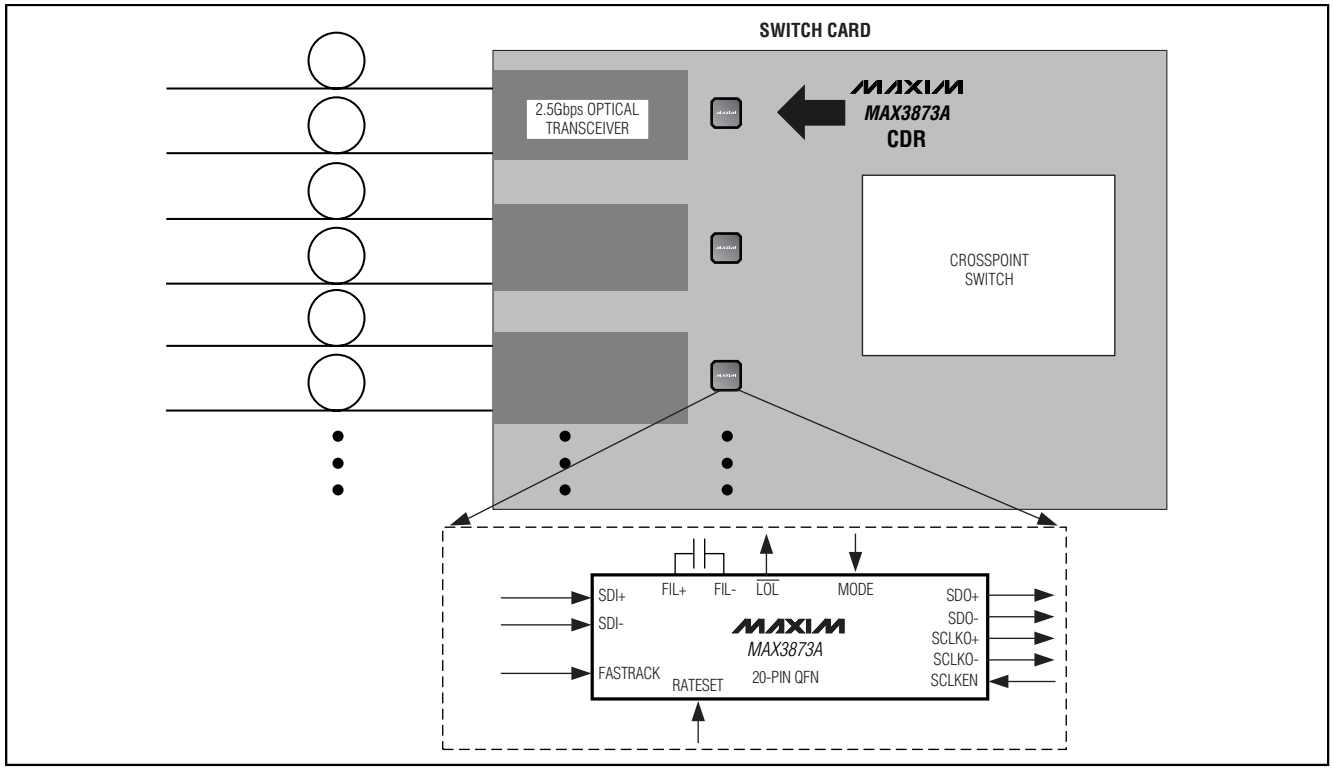
Typical Application Circuit



Chip Information

TRANSISTOR COUNT: 2028

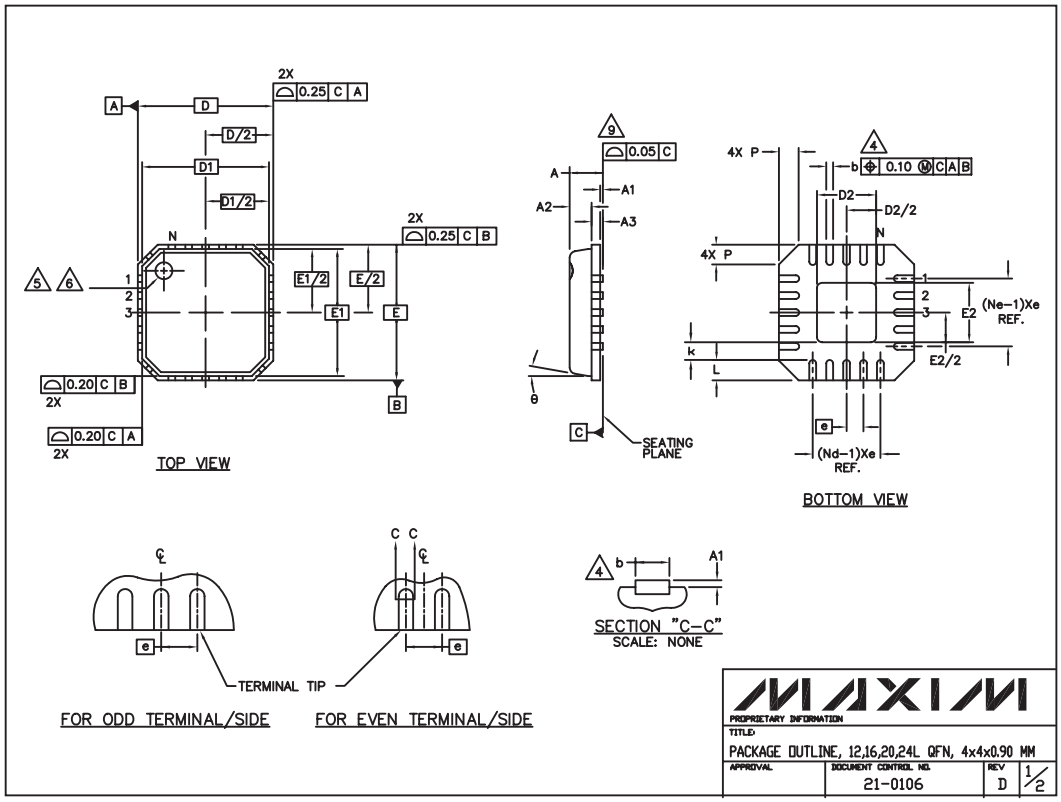
PROCESS: SiGe BiCMOS

Low-Power, Compact 2.5Gbps or 2.7Gbps Clock-Recovery and Data-Retiming IC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



Low-Power, Compact 2.5Gbps or 2.7Gbps Clock-Recovery and Data-Retiming IC

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	0.80	0.00	0.65	0.80	0.00	0.65	0.80	0.00	0.65	0.80
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
D1	3.75 BSC			3.75 BSC			3.75 BSC			3.75 BSC		
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E1	3.75 BSC			3.75 BSC			3.75 BSC			3.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.50	0.60	0.75	0.50	0.60	0.75	0.50	0.60	0.75	0.30	0.40	0.55
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°	–	12°	0°	–	12°	0°	–	12°	0°	–	12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1244-2	1.95	2.10	2.25	1.95	2.10	2.25
G1644-1	1.95	2.10	2.25	1.95	2.10	2.25
G2044-3	1.95	2.10	2.25	1.95	2.10	2.25
G2044-4	1.55	1.70	1.85	1.55	1.70	1.85
G2444-1	1.95	2.10	2.25	1.95	2.10	2.25
G2444-2	2.45	2.60	2.75	2.45	2.60	2.75

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21 0106	REV D	2/2