FUJITSU SEMICONDUCTOR

FR50
32-BIT MICROCONTROLLER
MB91F364G
Short specification

Release 4.2 05-Aug-2002
Fujitsu Ref. AEQ32091A

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FUJITSU

Revision History

Revision	Date	Name	Item
1.0	07-May-2001	ALan	First Release
1.2	10-Sep-2001	Br	add 1 more UART channel, remove 48 bits for time base timer, remove IRDA option from SIO
1.5	26-Oct-2001	JF	Pin assignment updated after pinout meeting
1.6	6-Nov-2001	Br	Update with regard to optional features
1.7	8-Nov-2001	JF	Pinout changed for better ADC supply
1.8	2-Dec-2001	Br	Add pinlist, add LED port in diagram, add IO map and vector table, add some references to the MB91360 hardware manual, add pinning in flash memory mode
2.0	07-Dec-2001	JF	Interrupt table: Resource numbers removed; BDSUENA (BDSU enable) at addr. 0x01FF; Port R and Port P[3:2] changed to type "A"; I2C pad drawing added
2.2	20-Dec-2001	JF	LIN-UART chapter added
2.3	16-Jan-2002	JF	DAC added, outputs at pins 117 + 118
2.4	21-Jan-2002	JF	Flash mode pin table changed (A[20] added)
2.6	27-Jan-2002	JF	Added "Flash Memory CPU Access" section I/O map: Initial values of FMCS and FMWT changed
2.7	12-Mar-2002	JF	LIN-UART registers renamed: SCR0 --> SCR5 SCR1 --> SCR6 and so on, to disinguish from old UART reg's
2.9	04-Apr-2002	JF	LIN-UART section: All user-relevant data added
3.0	14-Jun-2002	JF	DAC port behaviour added
3.2	08-July-2002	JF	Block structure updated (BDSU under eval.)
4.1	25-July-2002	JF	Pin 64 changed to VSS (must NOT be connected in first engineering samples)
4.2	05-Aug-2002	JF	IO-Map: OCS23 register entry added

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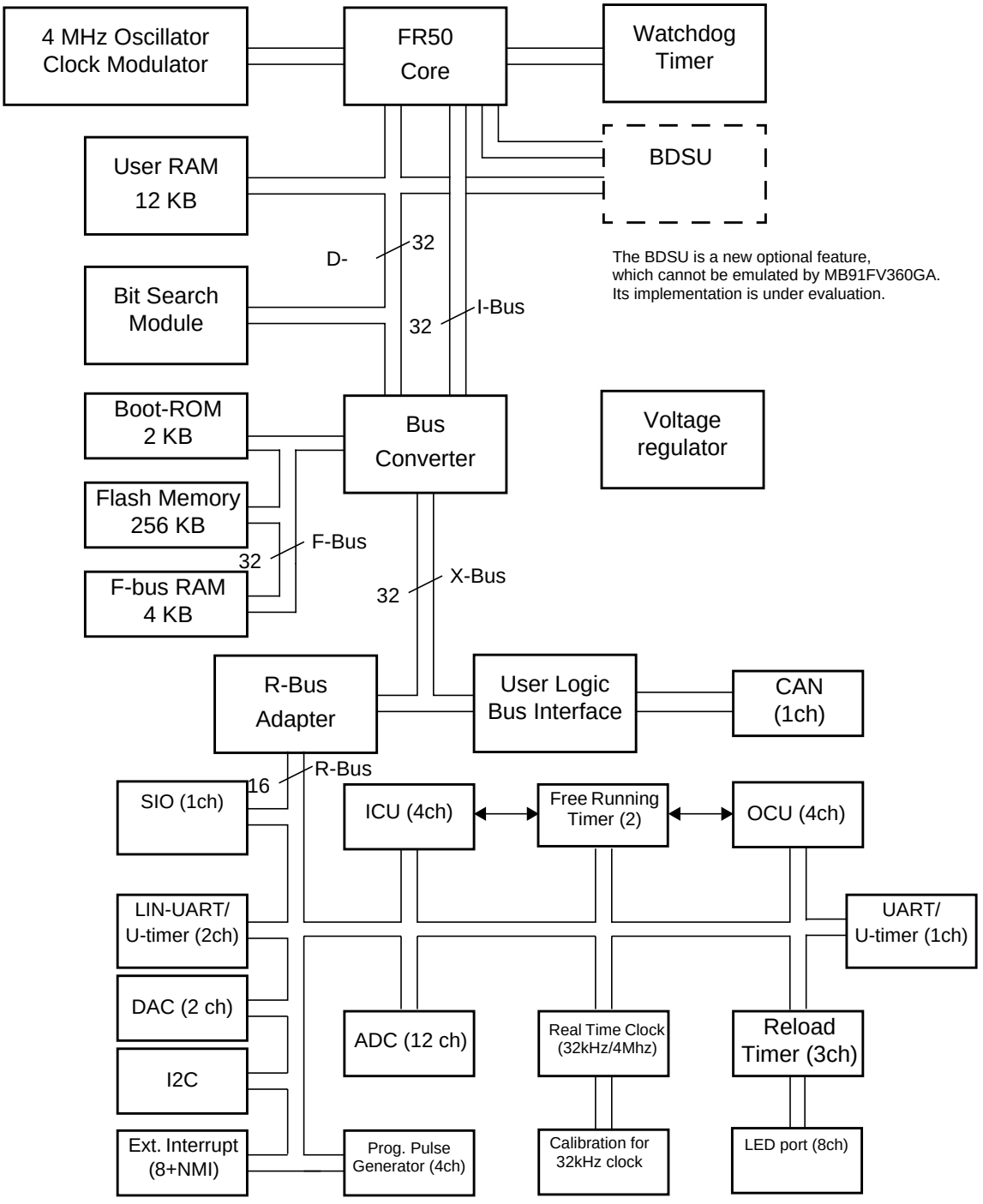
1 MB91F364G Overview

1.1 MB91F364G Block Structure



LIN-UART is a new feature which cannot be emulated by MB91FV360GA.
The correct functionality cannot be guaranteed until evaluation has been carried out..

1.2 Core Functionality

Function	Feature	Remarks
FR50 Core	32-bit Fujitsu RISC Core FR30 software compatible	
BDSU (optional)	Background debug support unit Features see BDSU spec.	This is a new optional module which cannot be emulated by MB91FV360GA. The implementation of this feature is under evaluation.
Clock module (clock control, clock divider, PLLs)	Setting of frequencies for CPU and peripherals Low power consumption modes: RTC mode: only the **R**eal **T**ime **C**lock and the oscillator are active (= STOP mode and bit 0 of STCR is set to 0) STOP mode: all internal circuits and the oscillation circuits are halted	initial value for oscillation stabilization time in mode MD="000": 32 ms at 4 MHz oscillation clock. Time starts after release of INITX
Watchdog	adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles)	
User RAM 12 kB	RAM for user data	see remark below table
F-bus RAM 4 kB	RAM for data and code	see remark below table
Flash Memory 256 kB	sector architecture: sector 0: 64 kB | sector 5: 64 kB sector 1: 32 kB | sector 6: 32 kB sector 2: 8 kB | sector 7: 8 kB sector 3: 8 kB | sector 8: 8 kB sector 4: 16 kB | sector 9: 16 kB | | V V 16 bit 16 bit write access is 16 bit wide, read access can be 16 or 32 bit wide	Minimum 10000 program/erase cycles Minimum 10 years data retention Net read cycle time to the memory: 40 ns. For overall access time see MB91360 Hardware Manual. located on F-Bus The last two addresses of this flash memory 0FFFF8H and 0FFFFCH overlap with the fixed reset and fixed mode vectors. Writing to these addresses is not possible.
Boot ROM 2 kB		
Interrupt Controller	1 non-maskable ext. interrupt channel, 8 external interrupt channels, 38 internal interrupts, 16 programmable priority levels	

Bit Search Module	Searches a word for the position of the first “1” and “0” change bit, starting from the MSB. Performs the search in 1 cycle.	
Fixed Reset Vector	Hardwired reset and mode vector	code starts at 0F:4000_H
Voltage Regulator	Generates internal voltage of 3.3 V	supply from an external regulator is also under consideration

Remark:

Set bit 9 (SYNCR) of TBCR to 1 to enable the synchronization of the reset signal; a reset will be generated only after all bus accesses have been done. This avoids that erroneous data are written into the RAMs during reset.

1.3 Features

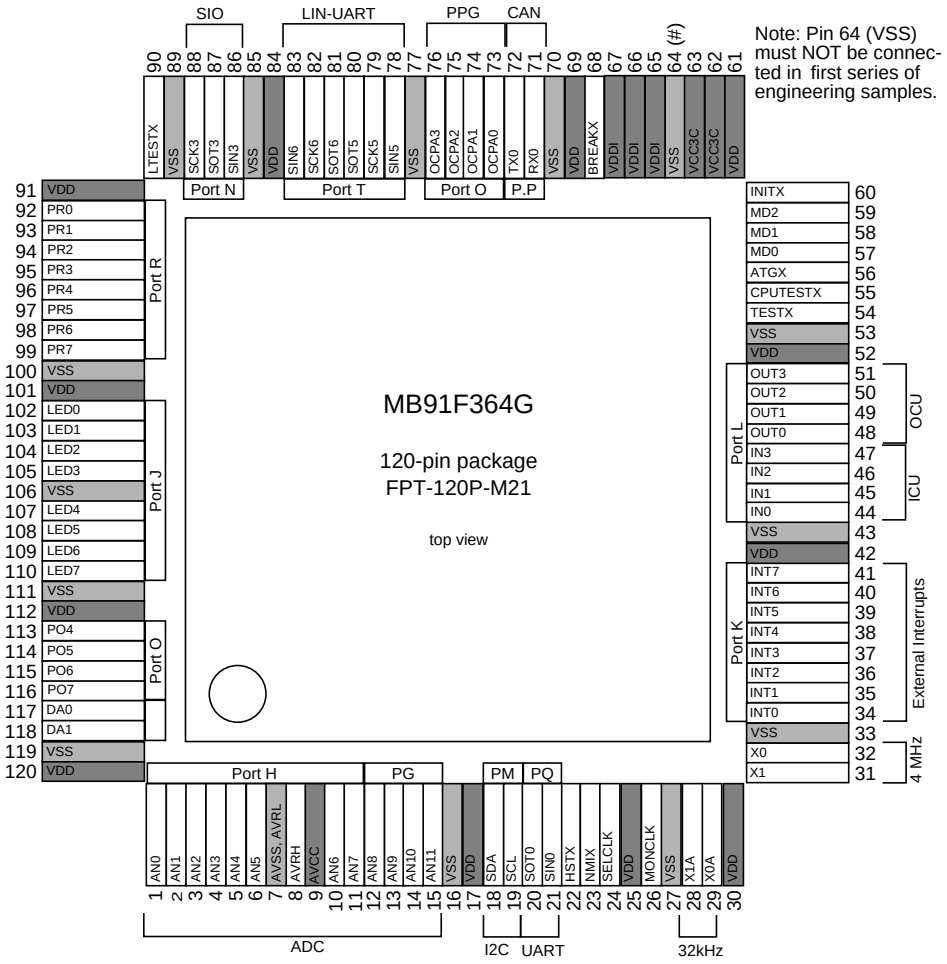
Function	Feature	Remarks
PPG (4 channels)	16-bit PWM Timer 16 bit down counter, cycle and duty setting registers interrupt at triggering, cycle or duty match can be triggered by software or reload timer PWM operation and one-shot operation Clock disable internal prescaler allows $f_{RES}/1$, $f_{RES}/4$, $f_{RES}/16$, $f_{RES}/64$ as counter clock	 required frequencies are 90-300 Hz
ADC (12 channels)	successive approximation, internal sample and hold circuit 10-bit resolution, 5 V operation, program selectable analogue input channels: single conversion mode continuous conversion mode stop conversion mode activation by software or external trigger can be selected Prescaling is done internally Clock disable	Maximum allowed frequency for digital part of ADC is 32 MHz
DAC (2 channels)	R-2R D/A converter 10-bit resolution, 5 V operation Clock disable	
Basic Interval Timer (3 channels)	16-bit reload timer, includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$)	
External Interrupt (8 channels)	can be programmed to be edge sensitive or level sensitive interrupt mask and request pending bits per channel	
Non-maskable Interrupt (NMI) (1 channel)	highest priority of all interrupts	

CAN (1 channel)	conforms to CAN specification version 2.0 A and B automatic re-transmission in case of error automatic transmission responding to remote frame prioritized 16 message buffer for data and IDs supports multiple messages flexible configuration of acceptance filtering: full bit compare / full bit mask / two partial bit masks supports up to 1 Mb/s Clock Disable	The CAN module is internally connected to CS7X, appropriate settings are automatically done during startup when running the BootROM code.
I^2C for standard and fast mode	master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I^2C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing) includes clock divider functionality Clock disable	SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of CLKP. Communication on the I2C bus between other connected devices is not possible if MB91F364G is switched off.
16-bit Input Capture (ICU) (4 channels)	rising edge, falling edge or rising & falling edge sensitive two 16-bit capture registers signals an interrupt at external event Clock disable	
16-bit Output Compare OCU (4 channels)	signals an interrupt when a match with of 16-bit IO timer occurs an output signal can be generated Clock disable	
Free running Timer (2 channels for ICU and OCU modules)	16-bit free running timer, signals an interrupt when overflow or match with compare register_0 includes prescaler ($f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^6$) timer data register has R/W access Clock disable	

Serial IO SIO Synchronous Serial Interface (1 channel) + SIO-Prescaler (1 channel)	Serial IO transfer can be started from MSB or LSB supports internal clock synchronized transfer and external clock synchronized transfer prescaler for shift clock allows: $f_{RES}/3$, $f_{RES}/4$, $f_{RES}/5$, $f_{RES}/6$, $f_{RES}/7$, $f_{RES}/8$ Clock disable	supports positive and negative clock edge synchronization
UART with LIN option (optional) (2 channels) Baudrate Generator (1 per UART)	serial I/O port for performing synchronous and asynchronous (start-stop synchronization) communication full duplex, double buffering supports multi-processor mode special features for LIN-bus systems variable data length (7/8 bit) 1 or 2 stop bits error detection function (parity, framing, overrun) interrupt function NRZ type transfer format baud rate generated by Baudrate Generator 15-bit timer to generate the required UART clock: $f_{RES}/2^1,\ldots,\sim f_{RES}/2^{15}$ Clock disable	This is a new module which cannot be emulated by MB91FV360GA. The correct functionality cannot be guaranteed until evaluation has been carried out. polarity of the port signals for receive and transmit is programmable

UART (1 channel)	serial I/O port for performing asynchronous (start-stop synchronization) communication full duplex, double buffering supports multi-processor mode variable data length (7/8 bit) 1 or 2 stop bits error detection function (parity, framing, overrun) interrupt function NRZ type transfer format	polarity of the port signals for receive and transmit is programmable
U-Timer (1 channel)	baud rate generated by U-Timer 16-bit timer to generate the required UART clock: $f_{RES}/2^5$,...,~$f_{RES}/2^{21}$ (asynchr. mode) Clock disable	
Real Time Clock (RTC) (Watch Timer)	facility to correct oscillation deviation read/write accessible second/minute/hour registers can signal interrupts every second/minute/hour/day internal clock divider and prescaler provide exact 1s clock based on a 4 MHz or a 32 kHz clock input Clock disable	prescaler value for 4 MHz is $1E847F_H$ prescaler value for 32 kHz is $04000F_H$
Sub-clock/Calibration 32 KHz	RTC module can be clocked either from 32kHz quartz or from 4 MHz quartz. Dynamic switching is not allowed. Additionally, a calibration of the RTC timer in 32 kHz operation, based on the more accurate 4 MHz clock timing, is possible.	
LED Port (8 channels)	allows to source 14 mA at Vdd-0.8 V and sink 24 mA at Vss+0.8 V respectively	
Clock modulator		

1.4 Pin Assignment



1.5 I/O Pins and Their Functions

Pin No	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
1	AN0	I/O	PH0	B	ADC input 0
2	AN1	I/O	PH1	B	ADC input 1
3	AN2	I/O	PH2	B	ADC input 2
4	AN3	I/O	PH3	B	ADC input 3
5	AN4	I/O	PH4	B	ADC input 4
6	AN5	I/O	PH5	B	ADC input 5
7	AVSS, AVRL				AVSS, analog reference low
8	AVRH			R	analog reference high
9	AVCC				AVCC
10	AN6	I/O	PH6	B	ADC input 6
11	AN7	I/O	PH7	B	ADC input 7
12	AN8	I/O	PG0	B	ADC input 8
13	AN9	I/O	PG1	B	ADC input 9
14	AN10	I/O	PG2	B	ADC input 10
15	AN11	I/O	PG3	B	ADC input 11
16	VSS				
17	VDD				
18	SDA	I/O	PM2	YA	I2C SDA
19	SCL	I/O	PM3	YA	I2C SCL
20	SOT0	I/O	PQ1	A	UART 0 SOT
21	SIN0	I/O	PQ0	A	UART 0 SIN
22	HSTX	I		F	hardware standby
23	NMIX	I		E	non maskable interrupt
24	SELCLK	I		F	select RTC clock
25	VDD				
26	MONCLK	O		QB	modulated clock output
27	VSS				

Pin No	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
28	X1A	O		I	32 kHz oscillator pin
29	X0A	I		I	32 kHz oscillator pin
30	VDD				
31	X1	O		H	4 MHz oscillator pin
32	X0	I		H	4 MHz oscillator pin
33	VSS				
34	INT0	I/O	PK0	B	external interrupt 0
35	INT1	I/O	PK1	B	external interrupt 1
36	INT2	I/O	PK2	B	external interrupt 2
37	INT3	I/O	PK3	B	external interrupt 3
38	INT4	I/O	PK4	B	external interrupt 4
39	INT5	I/O	PK5	B	external interrupt 5
40	INT6	I/O	PK6	B	external interrupt 6
41	INT7	I/O	PK7	B	external interrupt 7
42	VDD				
43	VSS				
44	IN0	I/O	PL0	B	ICU input 0 (see note 1)
45	IN1	I/O	PL1	B	ICU input 1 (see note 1)
46	IN2	I/O	PL2	B	ICU input 2 (see note 1)
47	IN3	I/O	PL3	B	ICU input 3 (see note 1)
48	OUT0	I/O	PL4	B	OCU output 0
49	OUT1	I/O	PL5	B	OCU output 1
50	OUT2	I/O	PL6	B	OCU output 2
51	OUT3	I/O	PL7	B	OCU output 3
52	VDD				
53	VSS				
54	TESTX	I		E	test input
55	CPUTESTX	I		E	test input
56	ATGX	I/O	PI3	A	ADC trigger
57	MD0	I		T	mode pin 0

Pin No	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
58	MD1	I		T	mode pin 1
59	MD2	I		T	mode pin 2
60	INITX	I		U	inital pin
61	VDD				
62	VCC3C				pins for regulator capacitance or for external supply of core voltage
63	VCC3C				
64	VSS (#)				**Don't connect to VSS in first ES series ! Leave open! See note 3**
65	VDDI				separate core supply
66	VDDI				
67	VDDI				
68	BREAKX	I	BREAKX	E	BDSU break pin
69	VDD				
70	VSS				
71	RX0	I/O	PP1	Q	CAN RX
72	TX0	I/O	PP0	Q	CAN TX
73	OCPA0	I/O	PO0	A	PPG output 0
74	OCPA1	I/O	PO1	A	PPG output 1
75	OCPA2	I/O	PO2	A	PPG output 2
76	OCPA3	I/O	PO3	A	PPG output 3
77	VSS				
78	SIN5	I/O	PT0	A	LIN-UART 5 SIN
79	SCK5	I/O	PT1	A	LIN UART 5 SCK
80	SOT5	I/O	PT2	A	LIN UART 5 SOT
81	SOT6	I/O	PT3	A	LIN UART 6 SOT
82	SCK6	I/O	PT4	A	LIN UART 6 SCK
83	SIN6	I/O	PT5	A	LIN UART 6 SIN
84	VDD				
85	VSS				

Pin No	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
86	SIN3	I/O	PN3	A	SIO SIN
87	SOT3	I/O	PN4	A	SIO SOT
88	SCK3	I/O	PN5	A	SIO SCK
89	VSS				
90	LTESTX	I	LTESTX	E	test pin
91	VDD				
92	PR0	I/O	PR0	A	port R 0
93	PR1	I/O	PR1	A	port R 1
94	PR2	I/O	PR2	A	port R 2
95	PR3	I/O	PR3	A	port R 3
96	PR4	I/O	PR4	A	port R 4
97	PR5	I/O	PR5	A	port R 5
98	PR6	I/O	PR6	A	port R 6
99	PR7	I/O	PR7	A	port R 7
100	VSS				
101	VDD				
102	LED0	I/O	PJ0	J	LED port 0
103	LED1	I/O	PJ1	J	LED port 1
104	LED2	I/O	PJ2	J	LED port 2
105	LED3	I/O	PJ3	J	LED port 3
106	VSS				
107	LED4	I/O	PJ4	J	LED port 4
108	LED5	I/O	PJ5	J	LED port 5
109	LED6	I/O	PJ6	J	LED port 6
110	LED7	I/O	PJ7	J	LED port 7
111	VSS				
112	VDD				
113	PO4	I/O	PO4	A	port O 4
114	PO5	I/O	PO5	A	port O 5
115	PO6	I/O	PO6	A	port O 6

Pin No	Pin Name	I/O	General Purpose IO Port	Circuit Type	Function
116	PO7	I/O	PO7	A	port O 7
117	DA0	O		C	See note 2
118	DA1	O		C	See note 2
119	VSS				
120	VDD				

Note 1: If the port L function register bits are cleared, the ICU input lines are connected with the LSYNC outputs of the LIN-UARTs.
Please refer to section **7.4 Baud Rate Detection Using the ICUs**.

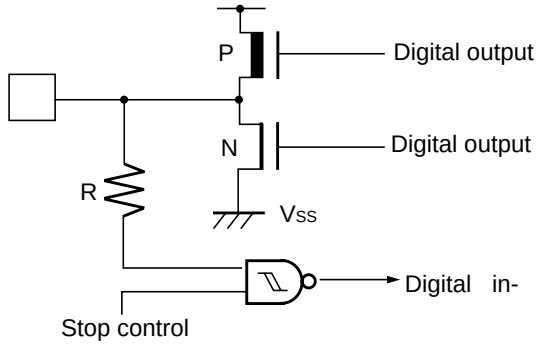
Note 2: The pins DA1 and DA0 are also used for digital test functions. To ensure proper system function, always write ’0’ to port P data direction register DDRP[3:2] and port P function register PFRP[3:2].

Note 3: Pin 064 (VSS) will be available after redesign. In the first ES series, this pin must be left open.

Circuit Type	Description
A	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, STOP control
B	I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control
C	Analog output
E	CMOS Schmitt-Trigger Input, 50K Pull-up
F	CMOS Schmitt-Trigger Input
H	4 MHz Oscillator Pin
I	32 kHz Oscillator Pin
J	I/O, IOH=14 mA / IOL = 24 mA, CMOS Automotive Schmitt-Trigger Input, STOP control (LED)
Q	I/O, IOH=4 mA / IOL=4 mA, CMOS Input, STOP control
QB	O, IOH=8 mA / IOL=8 mA, STOP control
R	AVRH Input
T	CMOS Input, can withstand V_{ID} for flash programming
U	CMOS Schmitt-Trigger Input, 50K Pull-up, 3.3 V and 5 V inputs to core
YA	I/O, IOH=3mA / IOL=3mA (I2C), CMOS Schmitt Trigger Input, STOP control

1.6 I/O Circuit Types

The new I/O circuit type YA is described below. For the other types please refer to the MB91360 Hardware Manua

Type	Circuit type	Remarks
Note: Symbols used in circuit types (Common to all circuit diagrams) P: P channel transistor N: N channel transistor R: Diffusion resistor		
YA		• I/O CMOS Schmitt-Trigger Input, STOP control , IOH = 3 mA, IOL = 3 mA, in I^2C mode operating as open drain outputs

2 Flash Memory Mode of MB91F364G

To enter the flash memory mode set mode pins MD0 to MD2 to “111”. In this mode, the pins correspond to those of the MBM29LV400C standard flash memory as shown in the following table.

MB91F364G				MBM29LV400C
Pin number	**Normal function**	**Flash Memory mode**	**Function in Flash Memory mode**	
1	AN0	ATDIN[a]	Access Signal ATD	
2	AN1	BYTEX	switch 8/16 bit mode	$\overline{BYTE}$
34 to 41	INT0 to INT7	DQ8 to DQ15	Data input/output	DQ8 to DQ15
44 to 47	IN0 to IN3	DQ0 to DQ3	Data input/output	DQ0 to DQ3
48 to 51	OUT0 to OUT3	DQ4 to DQ7	Data input/output	DQ4 to DQ7
54	TESTX	OEX	Output Enable	$\overline{OE}$
55	CPUTESTX	CEX	Chip Enable	$\overline{CE}$
56	ATGX	RY/BYX	Ready/Busy output	RY/$\overline{BY}$
57	MD0	HVDA9	High Volt. A9 [c]	A9 (V_{ID})
58	MD1	HVDR5	High Volt. RESET [c]	$\overline{RESET}$ (V_{ID})
59	MD2	HVDOE	High Volt. OE [c]	$\overline{OE}$ (VID)
60	INITX	RSTX	Hardware Reset	$\overline{RESET}$
90	LTESTX	EQIN[a]	Access Signal EQ	
92 to 99	PR0 to PR7	AQ0 to AQ7	Address input	A0 to A7
102 to 105	LED0 to LED3	AQ8 to AQ11	Address input	A8 to A11
107 to 110	LED4 to LED7	AQ12 to AQ15	Address input	A12 to A15
113 to 115	PO4 to PO6	AQ16 to AQ18	Address input	A16 to A18
116	PO7	WEX	Write Enable	$\overline{WE}$
117	PP2	AQ 20	Address input	A 20
118	PP3	TSTX [b]	Flash Test	

a.Pins 1 and 90 must be pulled low in Flash Memory Mode
c.Functionality as described in the Data Sheet of MBM29LV400C.
b.Pin 118 must be pulled high in Flash Memory Mode.

AVRH must be tight to a high level. All other Pins can be left open during Flash Memory Mode.

3 Flash Memory CPU access

This section overwrites parts of the chapter **31 Flash Memory** in hardware manual. The flash interface of MB91F364G has changed initialisation of control registers. With operation initialization reset (RST), the flash control registers are set to guarantee flash access at 64 MHz CPU clock operation.

3.1 Flash Control Status Register (FMCS)

The initial value of bit FACCEN is 0 now, fast access is enabled.

address	bit 7	bit6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00007000_H	**FACCEN**	----	----	RDYEG	RDY	RDYI	WE	LPM
access	R/W	R/W	R/W	R	R	R/W	R/W	R/W
initial value	**0**	1	1	0	X	0	0	0
value after Boot ROM	0	1	1	0	X	0	0	0

Bit 7: FACCEN: FACC Output Enable

Fast Flash Macro (used in MB91F364G):

0: Synchronous read access using ATDIN and EQIN signals - recommended setting

1: Asynchronous read access

The other bits of FMCS match the HW manual.

3.2 Flash Wait Control Register (FMWT)

The initial value of bit FAC0 is 1 now, the length of FACC low pulse and ATDIN high pulse is 1 CLKB cycle.

address	bit 7	bit6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00007004_H	----	----	FAC1	**FAC0**	EQINH	WTC2	WTC1	WTC0
access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value		0	0	**1**	0	0	1	1
value after Boot ROM Fast Flash Macro		0	0	1	0	0	1	1

Bits 5,4: Fast Flash Macro : These bits control the length of the high pulse for the ATDIN signal.
The changed initial value of FAC1=0 and FAC0=1 set FACC/ATDIN length to 1 CLKB cycle.
The other bits of FMWT match the HW manual.

4 Power-on Sequence

see MB91360 Hardware Manual

5 Handling of Unused Input Pins

see MB91360 Hardware Manual

6 Emulation Device

6.1 Overview

Besides for the UART with LIN option and for the support for background debugging MB91FV360GA can be used as emulation device for MB91F364G.

7 LIN-UART

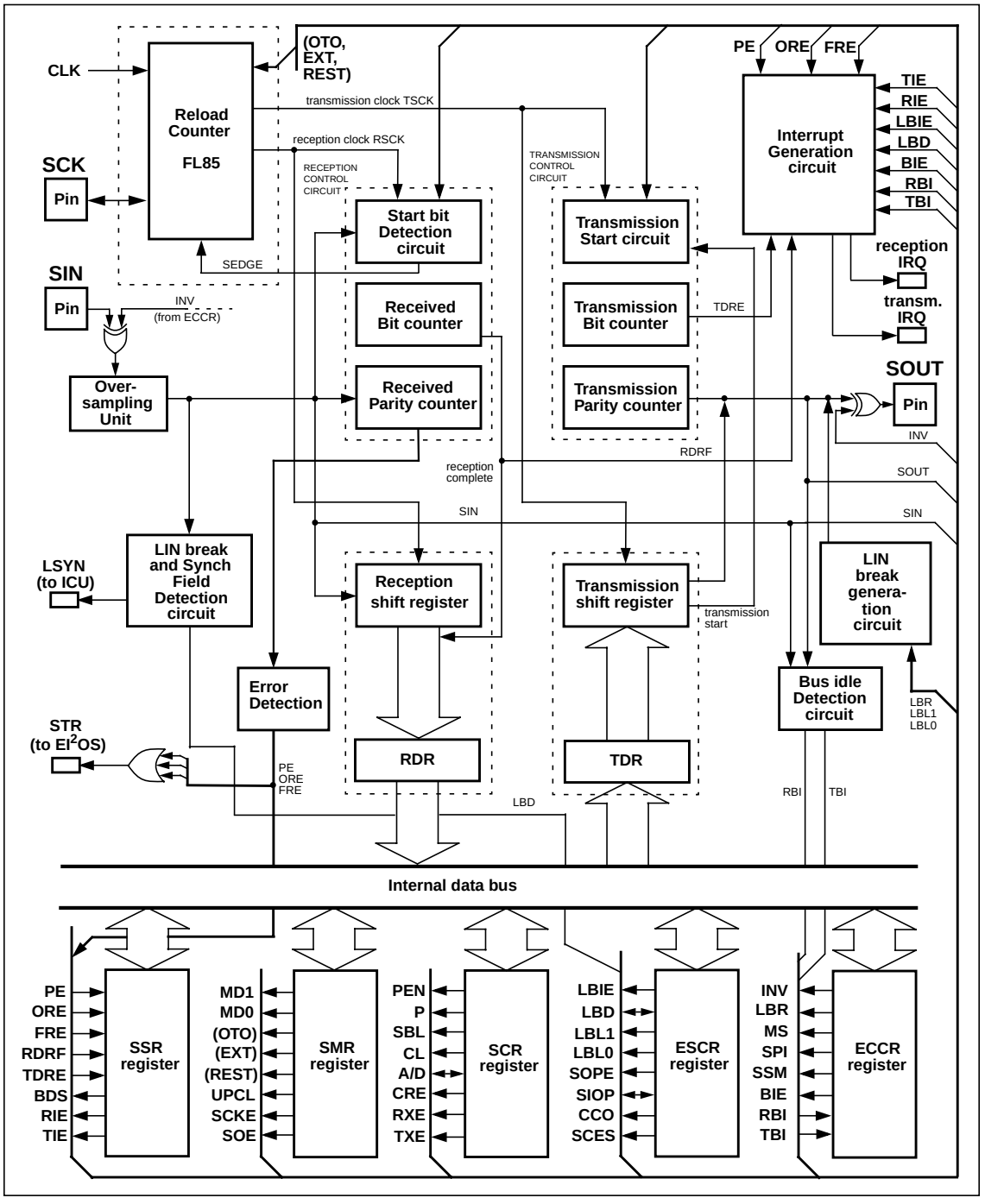
7.1 Overview

The UART (Universal [A]synchronous Receiver and Transmitter) with LIN (Local Interconnect Network) - Function is a general-purpose serial data communication interface for performing synchronous or asynchronous communication with external devices. The UART provides bidirectional communication function (normal mode), master-slave communication function (multiprocessor mode in master systems), and special features for LIN-bus systems (working both as master or slave device).

This UART is similar to older UART modules but not software compatible.

Item	Function
Data buffer	Full-duplex
Serial Input	5 times oversampling in asynchronous mode
Transfer mode	- Clock synchronous (start-stop synchronization and start-stop-bit-option) - Clock asynchronous (using start-, stop-bits)
Baud rate	- A dedicated baud rate generator is provided, which consists of a 15-bit-reload counter - An external clock can be input and also be adjusted by the reload counter
Data length	- 7 bits (not in synchronous or LIN mode) - 8 bits
Signal mode	Non-return to zero (NRZ) and return to zero (RZ)
Start bit timing	Clock synchronization to the falling edge of the start bit in asynchronous mode
Reception error detection	- Framing error - Overrun error - Parity error
Interrupt request	- Reception interrupt (reception complete, reception error detect) - Transmission interrupt (transmission complete) - Bus-Idle interrupt (belongs to reception interrupt) - LIN-Sync-break interrupt (belongs to rcp. interrupt)
Master-slave communication function (multiprocessor mode)	One-to-n communication (one master to n slaves) can be performed (This function is supported both for master and slave system).
Synchronous mode	Function as Master- or Slave-UART
Transceiving wires	Direct access possible
LIN bus options	- Operation as master device - Operation as slave device - Generation of LIN-Sync-break - Detection of LIN-Sync-break - Detection of start/stop edges in LIN-Sync-field connected to ICU
Synchronous serial clock	The synchronous serial clock can be output continuously on the SCK pin for synchronous communication with start & stop bits
Clock delay option	Special synchronous Clock Mode for delaying clock (useful for SPI)

7.2 Block Diagram



7.3 Registers

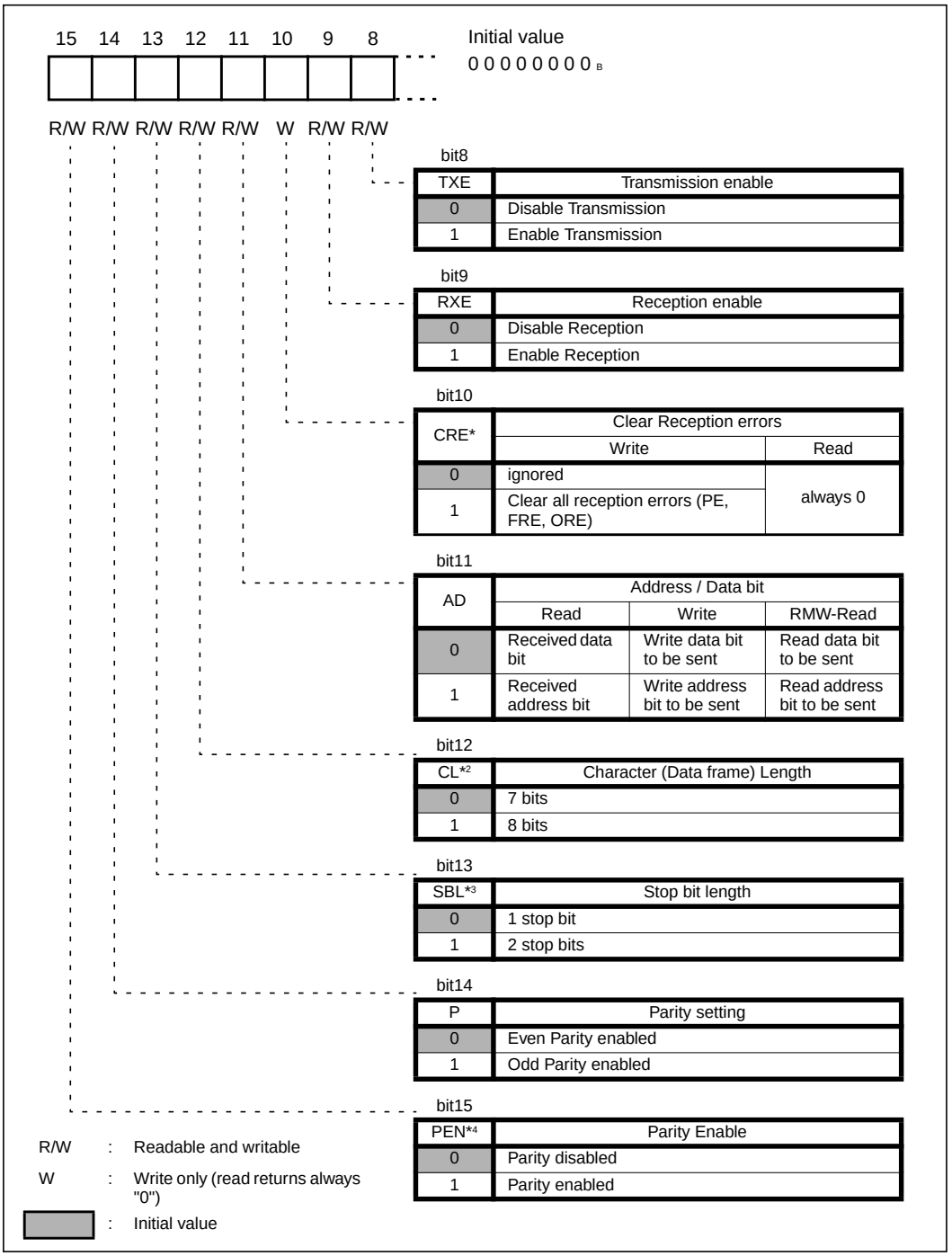
7.3.1 Register Addresses

MB91F364G containes 2 LIN-UARTS named "UART5" and "UART6".
UART5 is connected with the pins SIN5, SCK5, SOT5.
UART6 is connected with the pins SIN6, SCK6, SOT6.
The registers are nammed accordingly in the I/O map and have the following addresses:

UART5 Address:	+0	+1
0198_H	SCR5 (Serial Control Register)	SMR5 (Serial Mode Register)
$019A_H$	SSR5 (Serial Status Register)	RDR/TDR5 (Rx, Tx Data Register)
0198_H	ESCR5 (Extended Status/Control R.)	ECCR5 (Extended Comm. Contr. R.)
0198_H	*BGR15 (Baud Rate Generator R. 1)*	*BGR05 (Baud Rate Generator R. 0)*

UART6 Address:	+0	+1
$01A0_H$	SCR6 (Serial Control Register)	SMR6 (Serial Mode Register)
$01A2_H$	SSR6 (Serial Status Register)	RDR/TDR6 (Rx, Tx Data Register)
$01A4_H$	ESCR6 (Extended Status/Control R.)	ECCR6 (Extended Comm. Contr. R.)
$01A6_H$	*BGR16 (Baud Rate Generator R. 1)*	*BGR06 (Baud Rate Generator R. 0)*

7.3.2 Serial Control Register (SCR)



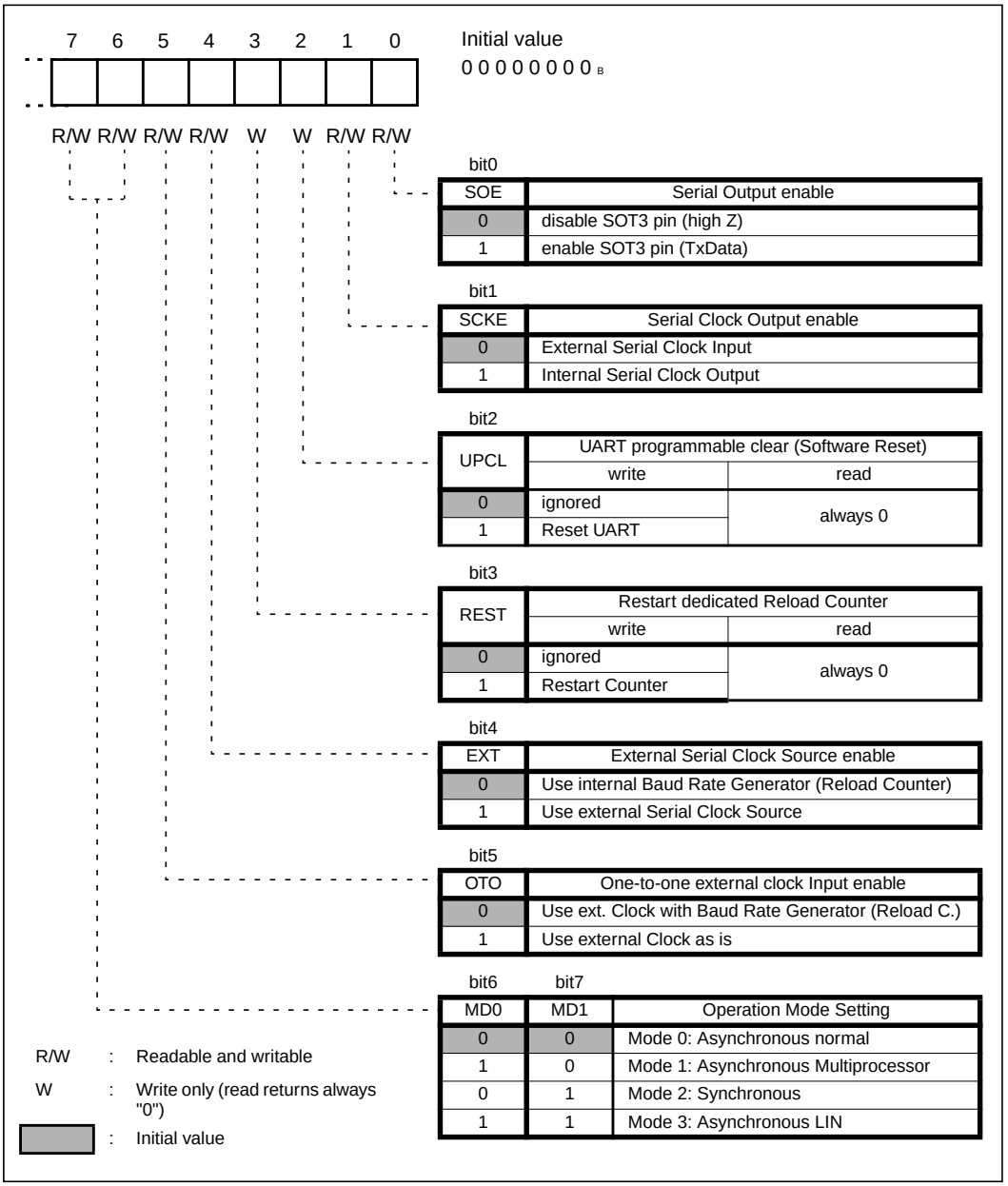
* Clearing the reception errors resets the reception finite state machine, so that it is ready to detect a new startbit (resp. a new data frame in mode 2) then.

*2 Character length is fixed to 8 bits in mode 2 and mode 3 (LIN), setting it to "0" in these modes has no effect

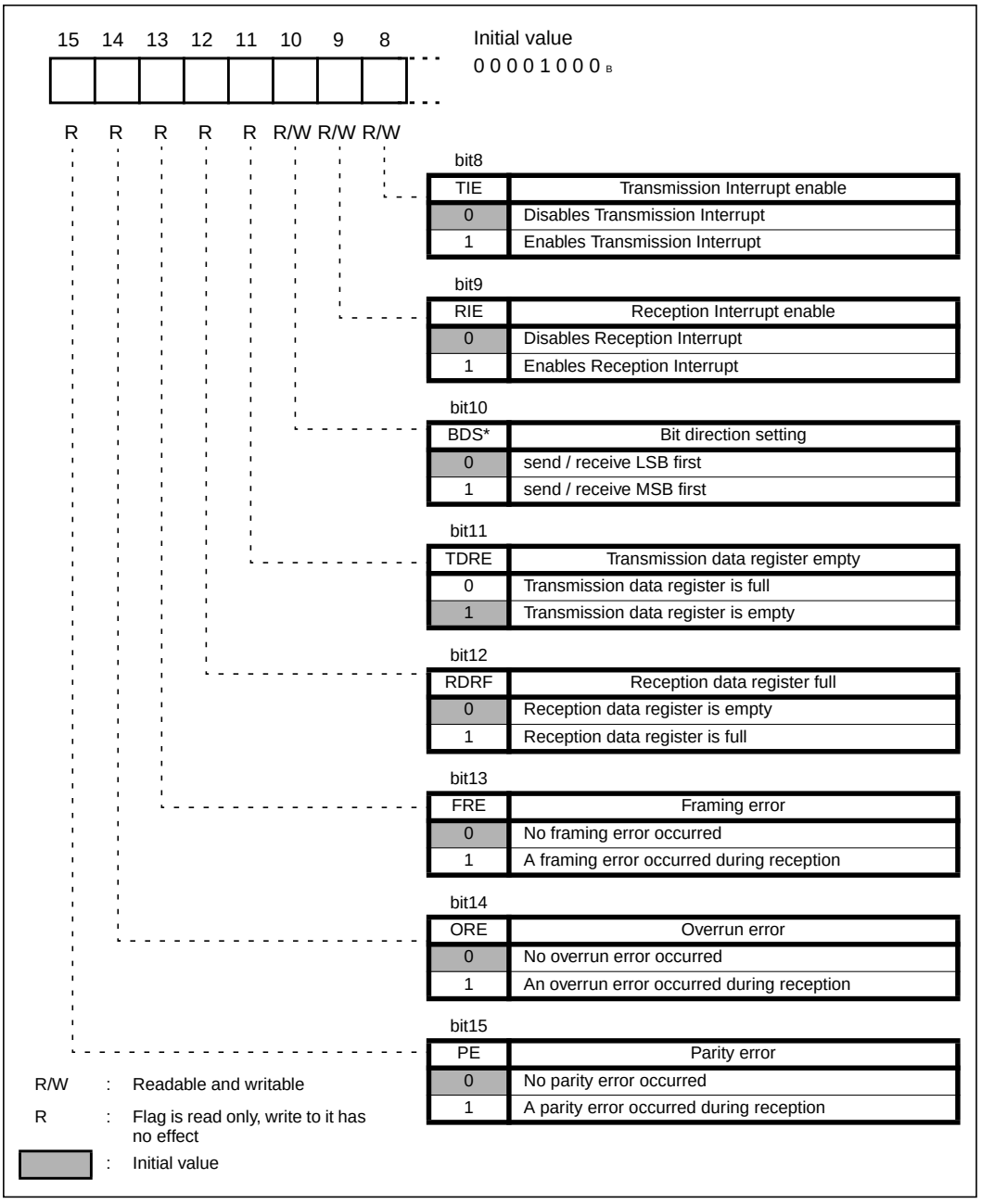
*3 Stop bit length is fixed to 1 in mode 3 (LIN), setting it to "1" in this mode has no effect

*4 Parity is only provided in mode 0 or in mode 2 if SSM is enabled. Setting it to "1" in all other cases has no effect

7.3.3 Serial Mode Register (SMR)

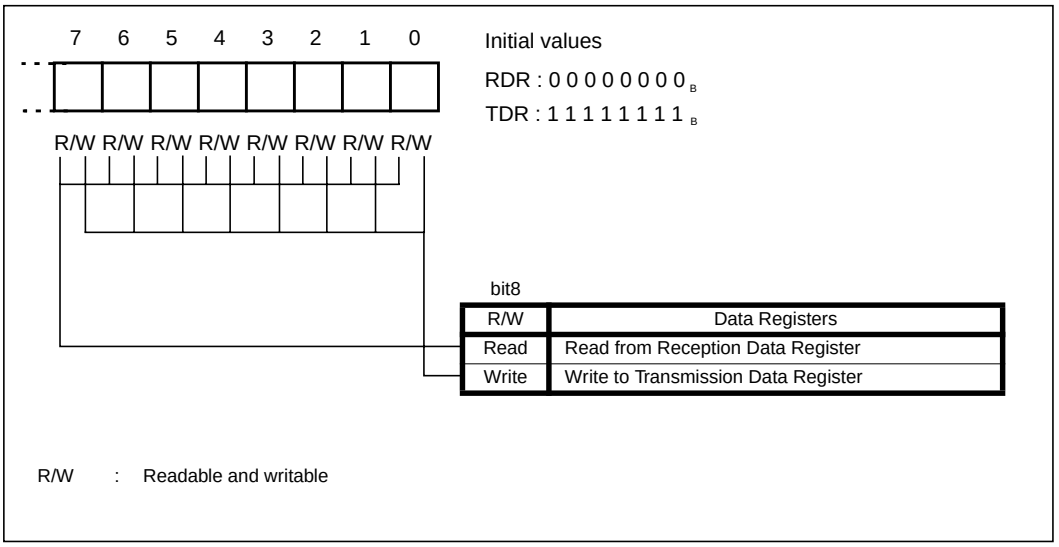


7.3.4 Serial Status Register (SSR)

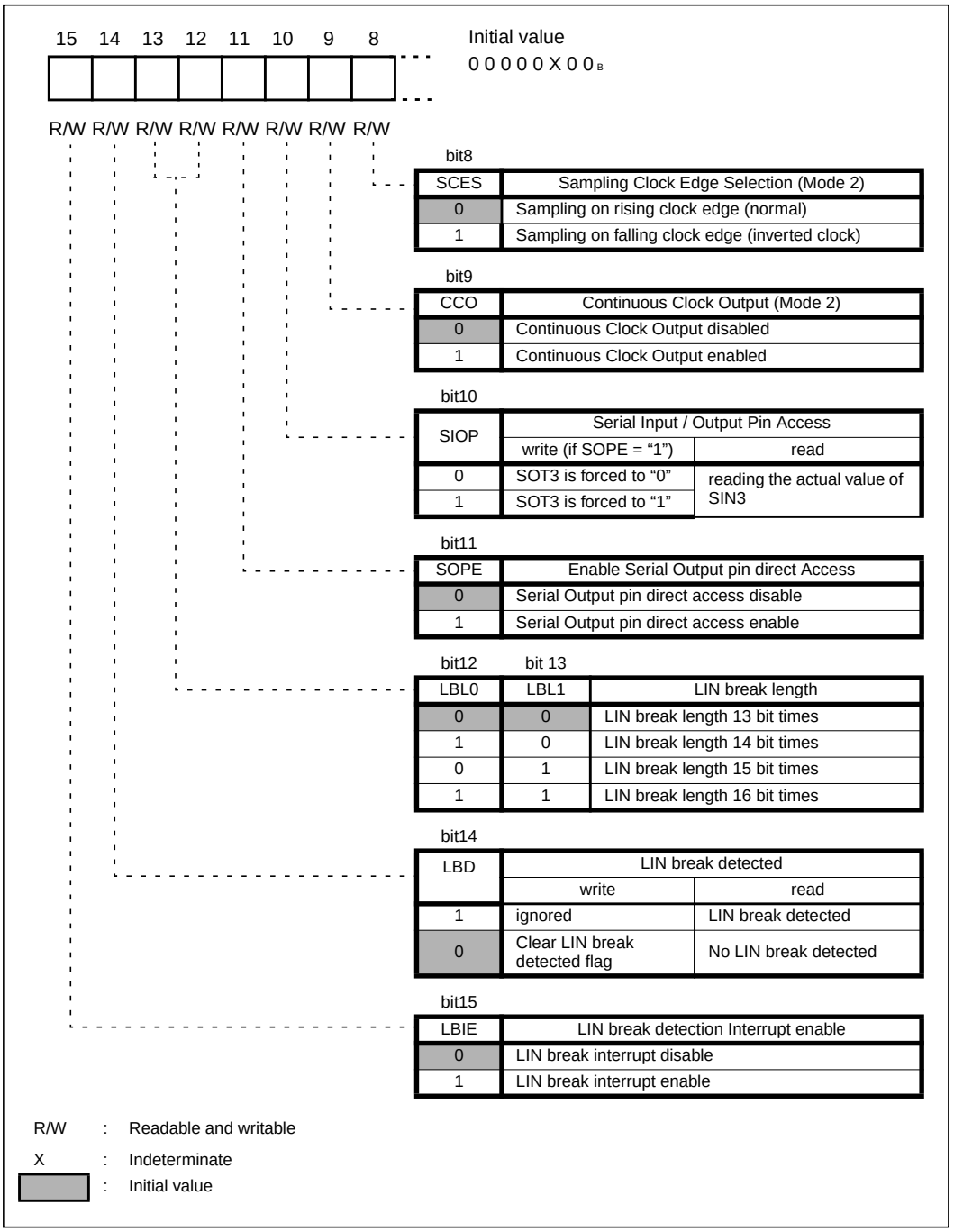


* BDS is fixed to "0" in mode 3 (LIN), setting it to "1" in this mode has no effect

7.3.5 Reception Data Register (RDR) and Transmission Data Register (TDR)



7.3.6 Extended Status/Control Register (ESCR)



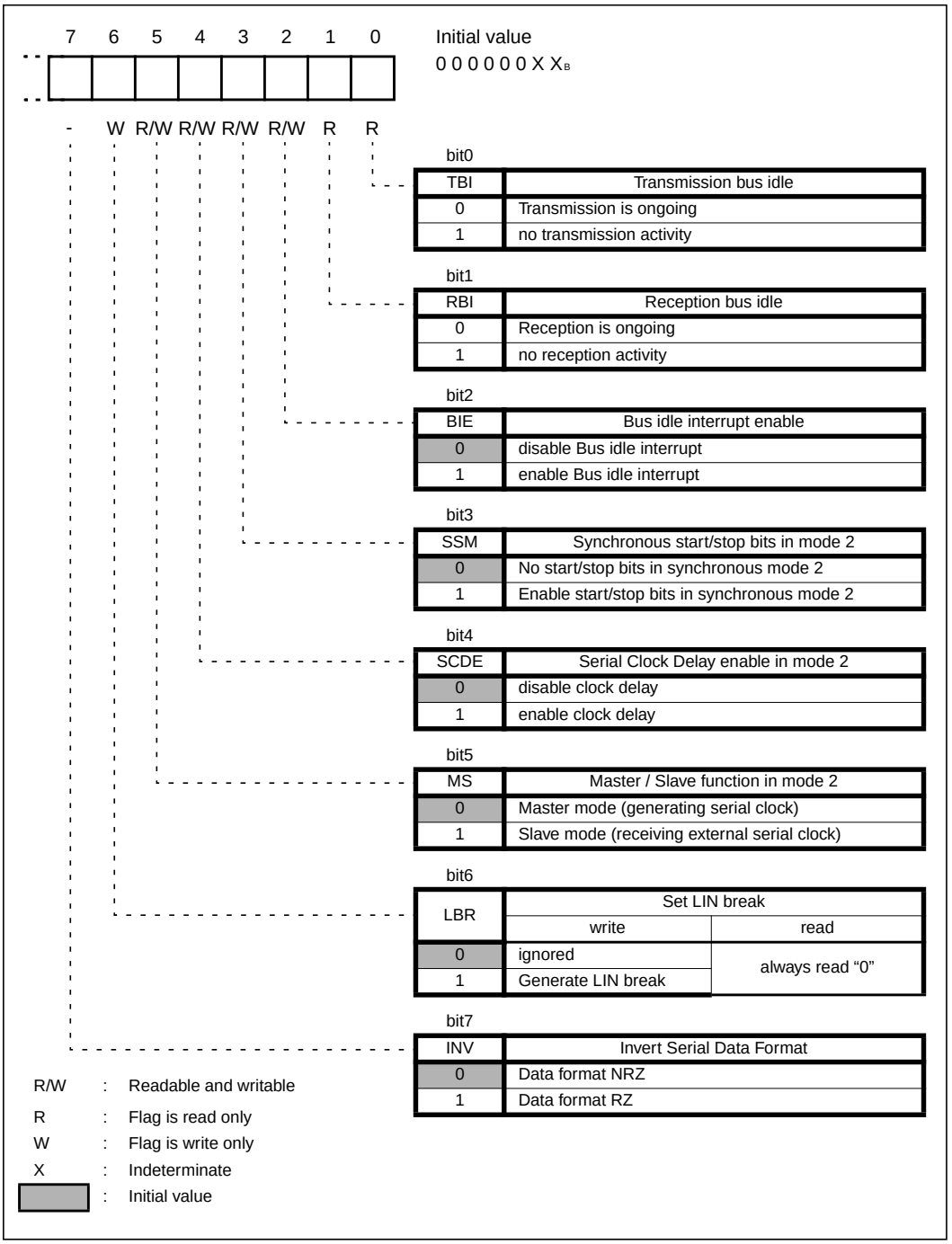
* Description of the interaction of SOP and SIOP:

SOPE	SIOP	Writing to SIOP	Reading from SIOP
0	R	has no effect	returns current value of SIN
1	R/W	write "0" or "1" to SOUT	returns current value of SIN

"1" is the initial value of SIOP, if enabling SOPE.

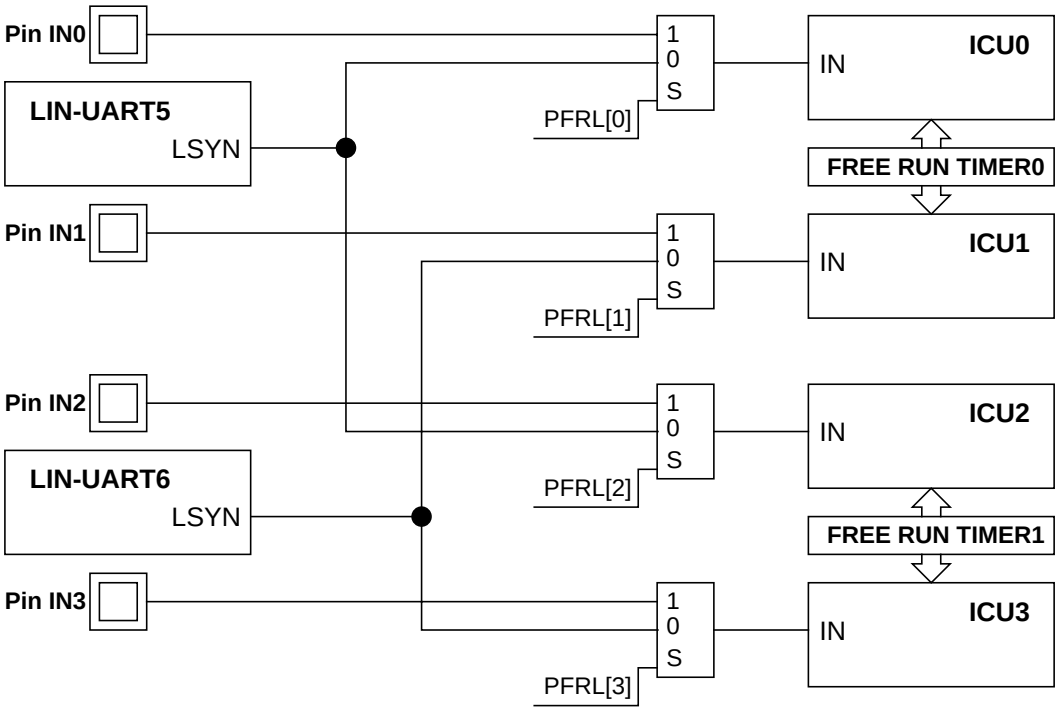
If a Read-Modify-Write cycle is active, the SIOP flag returns the value of the Serial Output pin (SOUT) in the read cycle.

7.3.7 Extended Communication Control Register (ECCR)



7.4 Baud Rate Detection Using the ICU's

The LIN-UARTs provide the signal LSYN that can be connected to the ICU so that LSYN's pulse length can be measured to derive the baud rate. The connection of the LSYN signals to the ICUs is controlled by the Port L function register PFRL (address 0415_H), bits PFRL[3:0]:



If the PFR bit is set, the ICU is connected to its input pin IN.
If the PFR bit is cleared, the pin IN is in port mode (PortL[3:0]), and the LIN-UARTs are connected to the ICU. The user has to take into account that:

- ICU0 and ICU1 share one free running timer (prescaler), ICU2 and ICU3 share the other one.
- The free running timers can be cleared by enabling this function in OCU0/OCU2 !

7.5 Operation modes

The LIN-UART operates in four different modes, which are determined by the MD0- and the MD1-bit of the Serial mode control register (SMCR). Mode 0 and 2 are used for bidirectional serial communication, mode 1 for master/slave communication and mode 3 for LIN master/slave communication.

Operation mode		Data length		Synchroniza-tion of mode	Length of stop bit	data bit direction*
		parity disabled	parity enabled			
0	normal mode	7 or 8		asynchronous	1 or 2	L/M
1	multiprocessor	7 or 8 + 1**	-	asynchronous	1 or 2	L/M
2	normal mode	8		synchronous	0, 1 or 2	L/M
3	LIN mode	8	-	asynchronous	1	L

* means the data bit transfer format: LSB or MSB first

** "+1" means the indicator bit of the address/data selection in the multiprocessor mode, instead of parity.

Note: Mode 1 operation is now supported both for master or slave operation of the UART in a master-slave connection system. In Mode 3 the UART function is locked to 8N1-Format, LSB first.

If the mode is changed, the UART cuts off all possible transmission or reception and awaits then new action.

The MD1 and MD0 bit of the Serial Mode Register (SMR) determine the operation mode of the UART as shown in the following table:

MD1	MD0	Mode	Description
0	0	0	Asynchronous (normal mode)
0	1	1	Asynchronous (multiprocessor mode)
1	0	2	Synchronous (normal mode)
1	1	3	Asynchronous (LIN mode)

7.5.1 Operation in asynchronous mode (Operation modes 0 and 1)

Transfer data format:

Generally each data transfer in the asynchronous mode operation begins with the start bit (low-level on bus) and ends with at least one stop bit (high-level). The direction of the bit stream (LSB first or MSB first) is determined by the BDS-Bit of the Serial Status Register (SSR). The parity bit (if enabled) is always placed between the last data bit and the (first) stop bit.

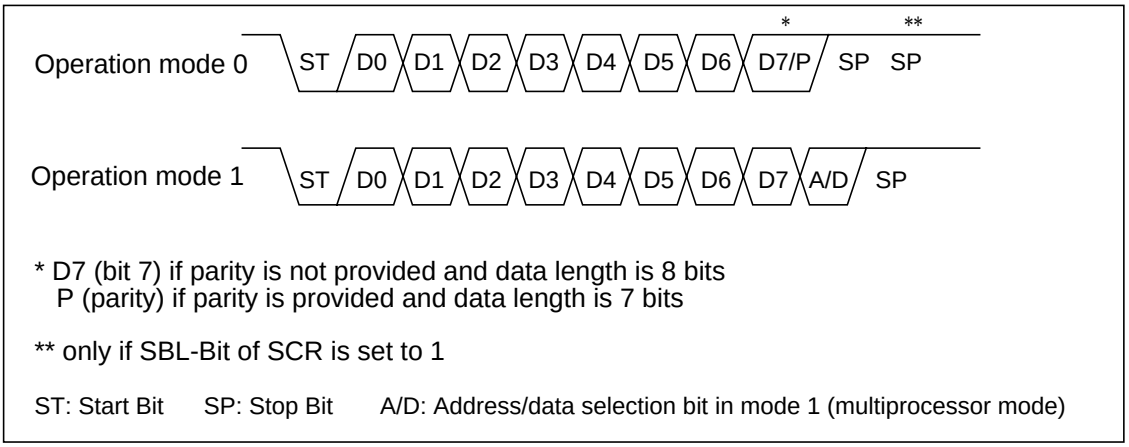
In operation mode 0 the length of the data frame can be 7 or 8 bits, with or without parity, and 1 or 2 stop bits.

In operation mode 1 the length of the data frame can be 7 or 8 bits with a following address-/data-selection bit instead of a parity bit. 1 or 2 stop bits can be selected.

The calculation formula for the bit length of a transfer frame is:

Length = 1 + d + p + s

(d = number of data bits [7 or 8], p = parity [0 or 1], s = number of stop bits [1 or 2])



Note: If BDS-Bit of the Serial Status Register (SSR) is set to "1", then the bit stream processes as: D7, D6, ... , D1, D0, (P).

During Reception both stop bits are detected, if selected. But the Reception data register full (RDRF) flag will go "1" at the first stop bit, but the bus idle flag (RBI of ECCR) goes "1" after the second stop bit if no further start bit is detected. (The second stop bit belongs to "bus activity", although it is just mark level.)

Transmission Operation:

If the Transmission Data Register Empty (TDRE) flag bit of the Serial Status Register (SSR) is "1", transmission data is allowed to be written to the Transmission Data Register (TDR). When data is written, the TDRE flag goes "0". If the transmission operation is enabled by the TXE-Bit ("1") of the Serial Control Register (SCR), the Data is written next to the transmission shift register and the transmission starts at the next clock cycle of the serial clock, beginning with the start bit. Thereby the TDRE flag goes "1", so that new data can be written to the TDR.

If transmission interrupt is enabled (TIE = 1), the interrupt is simply generated by the TDRE flag. Note, that the initial value of the TDRE flag is "1", so that in this case if TIE is set to "1" an interrupt will occur immediately.

Reception Operation:

Reception operation is performed every time it is enabled by the Reception Enable (RXE) flag bit of the SCR. If a start bit is detected, a data frame is received according to the format specified by the SCR. By occurring errors, the corresponding error flags are set (PE, ORE, FRE). However after the reception of the data frame the data is transferred from the serial shift register to the Receive Data Register (RDR) and the Receive Data Register Full (RDRF) flag bit of the SSR is set. The data then has to be read by the CPU. By doing so, the RDRF flag is cleared. If reception interrupt is enabled (RIE = 1), the interrupt is simply generated by the RDRF.

Note: Only when the RDRF flag bit is set the Reception Data Register (RDR) contains valid data.

Stop Bit, Error Detection, and Parity:

For transmission, 1 or 2 stop bits can be selected. During reception, if selected, both stop bits are checked, to set the reception bus idle (RBI) flag of the ECCR correctly not until after the second stop bit.

In mode 0 parity, overrun, and framing error can detected.

In mode 1, overrun and framing error can be detected. Parity is not provided.

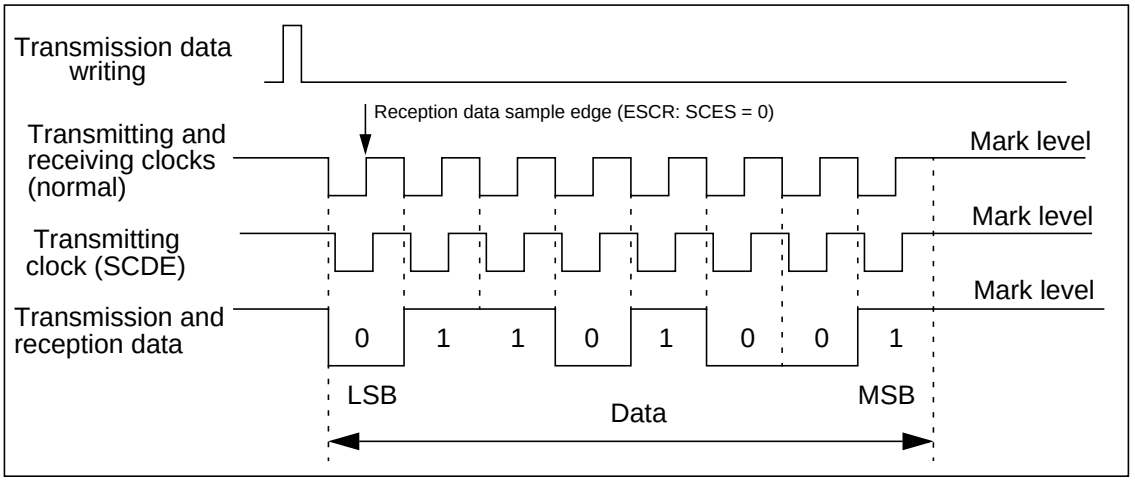
By setting the Parity Enable (PEN) bit of the Serial Control Register (SCR) the UART provides parity calculation (during transmission) and parity detection and check (during reception) in mode 0 (and mode 2 if the SSM bit of the ECCR is set).

Even parity is set, if the P flag bit of the SCR is cleared, odd parity if the flag bit is set.

7.5.2 Operation in Synchronous Mode (Mode 2)

Transfer data format:

In the synchronous mode, 8-bit data is transferred with no start or stop bits if the SSM bit of the Extended Communication Control Register (ECCR) is 0. To the data format in mode 2 belongs a special clock signal. The figure below illustrates the data format during a transmission in the synchronous operation mode.



Clock Supply:

In clock synchronous mode (I/O extended serial), the number of the transmission and reception bits has to be equal to the number of clock cycles. Note, that if start/stop bits communication is enabled, the number of clock cycles has to match with the quantity for the additional start and stop bit(s).

If the internal clock (dedicated reload counter) is selected, the data receiving synchronous clock is generated automatically if data is transmitted.

If external clock is selected, be sure, that the transmission side of the Transmission Data Register contains data and then clock cycles for each bit to sent have to be generated and supplied from outside. The mark level ("H") must be retained before transmission starts and after it is complete.

Setting the SCDE bit of ECCR delays the transmitting clock signal about 50 ns to make sure, that the transmission data is valid and stable at any falling clock edge. (Necessary, if the receiving device samples the data at rising or falling clock edge).

If the Serial Clock Edge Select (SCES) bit of the ESCR is set, the UART's clock is inverted and thus samples the reception data at the *falling* clock edge. In this case be sure, that the serial data is valid at the falling serial clock edge.

Error Detection:

If no Start/Stop bits are selected (ECCR: SSM = 0) only overrun errors are detected.

Communication:

For initialization the synchronous mode following settings have to be done:

Braud Rate Generator Registers (BGR0/1):
Set the desired reload value for the dedicated Baud Rate Reload Counter

Serial Mode Control Register (SMR):
MD1, MD0: "10b" (Mode 2)
SCKE: "1" for dedicated Baud Rate Reload Counter
"0" for external clock input
SOE: "1" for transmission; "0" for reception

Serial Control Register (SCR):
RXE, TXE: one of these flag bit is set to "1"
PEN: no parity provided - Value: don't care
P, SBL, A/D: no parity, no stop bit(s), no Address/Data selection - Value: don't care
CL: automatically fixed to 8-bit data - Value: don't care
CRE: "1" (the error flag is cleared for initialization, possible transmission or reception will cut off)

Serial Status Register (SSR):
BDS: "0" for LSB first, "1" for MSB first
RIE: "1" if interrupts are used; "0" if not
TIE: "1" if interrupts are used; "0" if not

Extended Communication Register (ECCR):
SSM: "0" if no start/stop bits are desired (normal); "1" for adding start/stop bits (special)
MS: "0" for master mode (UART generates the serial clock); "1" for slave mode (UART receives serial clock from the master device)

To start the communication, write data into the Transmission Data Register (TDR).
To receive data, disable the Serial Output Enable (SOE) bit of the SMR and write dummy data to TDR.

Note: Because of the bidirectional function of the SCK pin, transmission and reception *at the same time* is *not* possible!

7.5.3 Operation with LIN Function (mode 3)

The UART can be used either for LIN-Master devices or LIN-Slave devices. For this LIN function a special mode (3) is provided. Setting the UART to mode 3, configure the data format to 8N1-LSB-first format.

UART as LIN master:

In LIN master mode the master determines the baud rate of the whole sub bus, i. e. the slaves have to synchronize to the master. Therefore nothing special baud rate settings have to be done.

Writing a "1" into the LBR bit of the Extended Status/Communication Register (ECCR) generates a 13 - 16 bit times low-level on the SOUT pin, which is the LIN synchronization break and the start of a LIN message. Thereby the TDRE flag of the Serial Status Register (SSR) goes "0" and is reset to "1" after the break, and generates a transmission interrupt for the CPU (if TIE of SSR is "1").

The length of the Synchronization break to be sent can be determined by the LBL1/0 bits of the ESCR as follows:

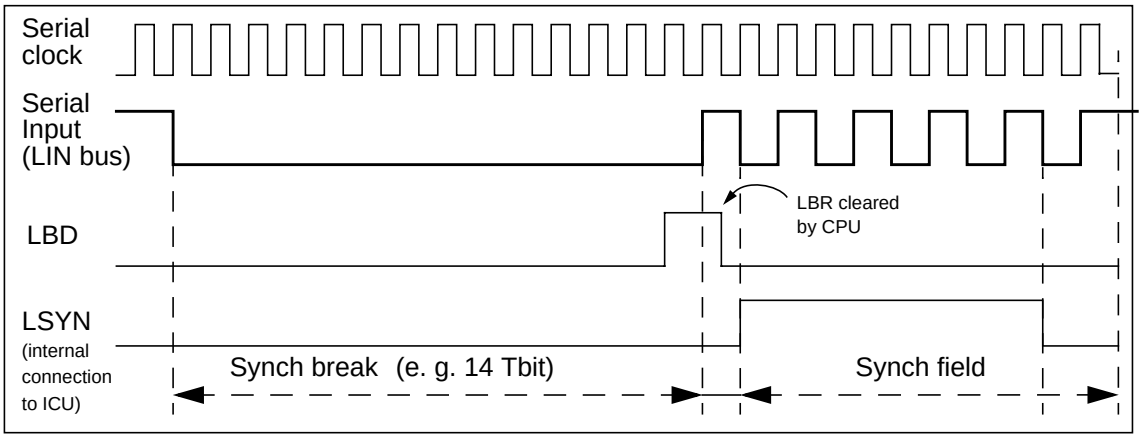
LBL1	LBL0	Length of Break
0	0	13 Bit times
0	1	14 Bit times
1	0	15 Bit times
1	1	16 Bit times

The Synch Field can be sent as a simple 0x55-Byte after the LIN break. To prevent a transmission interrupt, the 0x55 can be written to the TDR just after writing the "1" to the LBR bit, although the TDRE flag is "0". The internal transmission shifter waits until the LIN break has finished and shifts then the TDR value out. In this case no interrupt is generated after the LIN break and before the start bit.

UART as LIN slave:

In LIN slave mode the UART has to synchronize to the master’s baud rate. If Reception is disabled (RXE = 0) but LIN break Interrupt is enabled (LBIE = 1) the UART will generate an reception interrupt, if a synchronization break of the LIN master is detected, and indicates it with the LBD flag of the ESCR. Writing a "0" to this bit clears the interrupt. The next goal is to analyze the baud rate of the LIN master. The first falling edge of the Synch Field is detected by the UART. The UART signals it then to the Input Capture Unit (ICU) via a rising edge of the internal LSYN connection. The fifth falling edge resets the LSYN signal. The time in which the LSYN signal was "1" is then the actual baud rate of the LIN master multiplied by 8.

The figure below shows a typical start of a LIN message frame and the behavior of the UART:



7.5.4 Direct Access to Serial Bus Operation

The UART provides the ability for the Programmer to access directly to serial input or output pin. The software can always monitor the incoming serial data by reading the SIOP bit of the ESCR. If setting the Serial Output Pin direct access Enable (SOPE) bit of the ESCR the software can force the SOUT pin to a desired value. Note, that this access is only possible, if the transmission shift register is empty (i. e. no transmission activity).

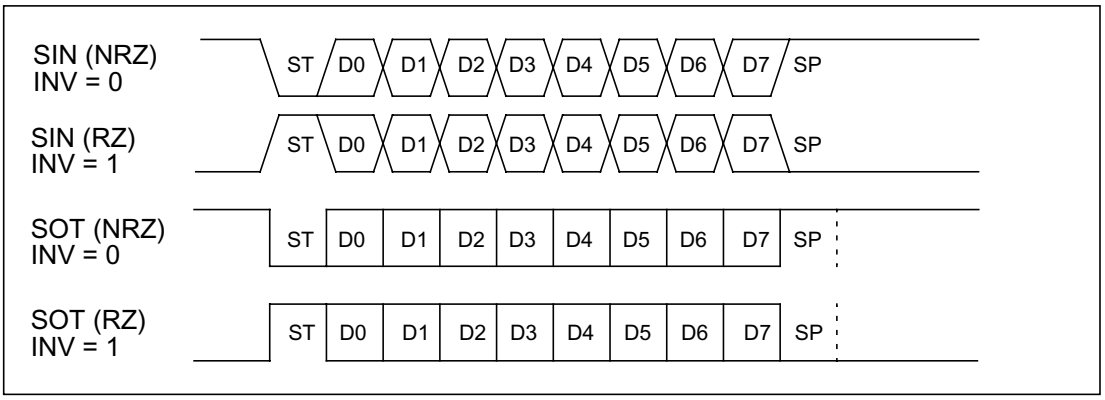
In LIN mode this function can be used for "reading back the own transmission" and used for error handling if something is physically wrong with the single-wire LIN-bus.

Note: Write the desired value to the SIOP pin **before** enabling the output pin access, to prevent undesired peaks.

7.5.5 Data Format setting

The INV bit of the Extended Communication Control Register (ECCR) inverts the serial data, if it is set to "1". This means that the signal mode is "return to zero" (RZ). Otherwise the signal mode for SIN and SOT ist "non return to zero" (NRZ, initial value).

The following graphic illustrates the two settings for INV:



Note, that the INV bit can be set in all operation modes, including LIN mode 3.

7.5.6 Register / Flag bits summary

In the UART FL84 the settings of the Register bits, which affect the transmission and reception behavior are depending on the current determined mode. Thus, trying to set a senseless value to a flag bit (e. g. Parity enable in LIN mode 3) does not affect the UART behavior. Reading from this pretended wrong set bit returns nevertheless the correct value.

The following table illustrates all possible setting for all UART modes:

Mode	Parity	Stop bit length	Byte length	A/D bit	Bit direc-tion	SCES	SCDE	SSM	INV
0	none, odd or even	1 or 2	7 or 8	-	LSB or MSB first	-	-	-	yes
1	-			yes		-	-	-	
2 (SSM = 0)	-	-	8	-		yes	yes	0	
2 (SSM = 1)	none, odd or even	1 or 2		-		yes	yes	1	
3 (LIN)	-	1		-	LSB first	-	-	-	

7.6 UART Interrupts

The UART uses both reception and transmission interrupts. For the following causes an interrupt can be generated:

- Receive data is transferred to the Reception Data Register (RDR), or a reception error occurs.
- Transmission data is transferred from the Transmission Data Register (TDR) to the transmission shift register.
- A LIN-synch break is detected
- bus idle is detected

The following table shows the interrupt control bits and causes of the interrupt:

Reception/ transmission/ ICU	Interrupt request flag bit	Flag Register	Operation mode				Interrupt cause	Interrupt cause enable bit	When Interrupt request flag bit is cleared
			0	1	2	3			
Reception	RDRF	SSR	x	x	x	x	receive data is written to RDR	SSR / RIE	Receive data is read
	ORE	SSR	x	x	x	x	Overrun error		"1" is written to clear rec. error bit (SSR/CRE)
	FRE	SSR	x	x	*	x	Framing error		
	PE	SSR	x		*		Parity error		
	LBR	ESCR	x			x	LIN synch break detected	ESCR / LBIE	"0" is written to ESCR/LBD
	TBI & RBI	ESCR	x	x	x	x	no bus activity	ECCR / BIE	Receive data / Send data
Transmission	TDRE	SSR	x	x	x	x	Empty transmission register	SSR / TIE	Transfer data is written
Input Capture Unit	ICP0	ICS01	x			x	1st falling edge of LIN synch field	ICS01/ ICE0	disable ICE0 temporary
	ICP0	ICS01	x			x	5th falling edge of LIN synch field	ICS01/ ICE0	disable ICE0

x = used / supported * = only available if SSM is set to "1"

7.6.1 Reception Interrupt

If one of the following events occurs in reception mode, the corresponding flag bit of the Serial Status Register (SSR) is set to "1":

- Data reception is complete, i. e. the received data was transferred from the serial input shift register to the Reception Data Register (RDR): **RDRF**
- Overrun error, i. e. RDRF = 1 and RDR was not read by the CPU: **ORE**
- Framing error, i. e. A stop bit was expected, but a "0"-bit was received: **FRE**
- Parity error, i. e. a wrong parity bit was detected: **PE**

If at least one of these flag bits above go "1" and the reception interrupt is enabled (SSR: RIE = 1), a reception interrupt request is generated.

If the Reception Data Register (RDR) is read, the RDRF flag is automatically cleared to "0". Note that this is the *only* way to reset the RDRF flag. The error flags are cleared to "0", if a "1" is written to the Clear Reception Error (CRE) flag bit of the Serial Control Register (SCR). The RDR contains only valid data if the RDRF flag is "1" and no error bits are set.

Note, that the CRE flag is "write only" and by writing a "1" to it, it is internally held to "1" for one CPU clock cycle.

7.6.2 Transmission Interrupt

If transmission data is transferred from the Transmission Data Register (TDR) to the transfer shift register (this happens, if the shift register is empty), the Transmission Data Register Empty (TDRE) flag bit of the Serial Status Register (SSR) is set to "1". In this case an interrupt request is generated, if the Transmission Interrupt Enable (TIE) bit of the SSR was set to "1" before.

Note, that the initial value of the TDRE (after hardware or software reset) is "1". So an interrupt is generated immediately then, if the TIE flag is set to "1". Also note, that the *only* way to reset the TDRE flag is writing data to the RDR.

7.6.3 LIN Synchronization Break Interrupt

This paragraph is only relevant, if the UART operates in mode 0 or 3.

If the bus (serial input) goes "0" (dominant) for more than 13 bit times, the LIN Break Detected (LBD) flag bit of the Extended Status/Control Register (ESCR) is set to "1". Note, that in this case after 9 bit times the reception error flags are set to "1", therefore the RIE flag has to set to "0" or the RXE flag has to set to "0", if only a LIN synch break detect is desired. In the other case a reception error interrupt would be generated first, and the interrupt handler routine has then to wait for LBD = 1.

The interrupt and the LBD flag are cleared after writing a "1" to the LBD flag. This makes it sure, that the CPU has detected the LIN synch break, because of the following procedure of adjusting the serial clock to the LIN master.

7.6.4 LIN Synchronization Field Edge Detection Interrupts

This paragraph is only relevant, if the UART operates in mode 0 or 3 as a LIN slave. After a LIN break detection the next falling edge of the reception bus is indicated by the UART. Simultaneously the internal LSYN signal (which is connected to the ICU) is set to "1". The LSYN signal is reset to "0" after the fifth falling edge of the LIN Synchronization Field. In both cases the ICU generates an interrupt, if "both edge detection" is enabled. The difference of the ICU counter values is then the serial clock multiplied by 8. Dividing it by 8 results in the new detected and calculated baud rate for the dedicated reload counter (FL85). There is no need to restart the reload counter, because it is automatically reset if a falling edge of a start bit is detected (SEDGE).

7.6.5 Bus Idle Interrupt

If there is no reception activity on the SIN pin, the RBI flag bit of the ECCR goes "1". The TBI flag bit respectively goes "1", when no data is transmitted. If the Bus Idle Interrupt Enable bit (BIE) of the ECCR is set and **both** bus idle flag bits (TBI **and** RBI) are "1", an interrupt is generated.

Note: The TBI flag goes also "0" if there is no bus activity, but a "0" is written to the SIOP bit, if SOPE is "1".

7.6.6 Software Reset

In case of malfunction of the UART there is the possibility to reset only the UART instead of resetting the whole MCU. The Software Reset/UART Programmable Clear (UPCL) bit (no. 2) in the SMR provides such function. Writing a "1" into this bit, resets the UART immediately. There is no need to reset this bit to "0", because one clock reset-"high"-level is generated automatically.

Note, that possible transmission or reception will cut off. The register values are saved, but the clock of the dedicated reload counter (FL85) is restarted.

The programmer should be careful with this function. It is recommended, that any write commands to the UART's SMR should masked with "0xfb" before to prevent accidentally lost of data.

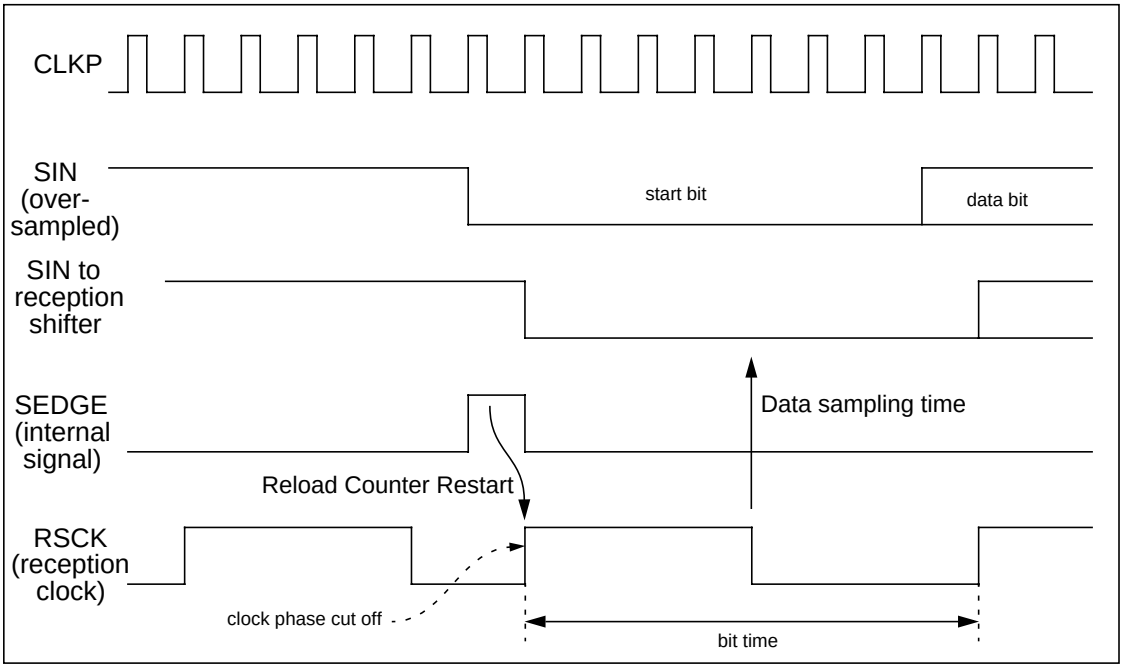
An alternative to resetting the UART state without restarting the reload counter (FL85) is to disable the reception (RXE = 0) or transmission (TXE = 0) function temporary. The reception and/or the transmission control circuits will "reset" internally.

Another alternative is changing the UART's operation mode temporary. This will have the same effect.

To reset the Reception Finite State Machine only, simply write a "1" to the CRE bit of the SCR.

7.7 Clock Synchronization

In asynchronous mode the UART detects a falling edge of a start bit and generates a signal (SEDGE) to restart the baud rate reload counter (FL85). This ensures that the serial data is sampled in the middle of the bit time.

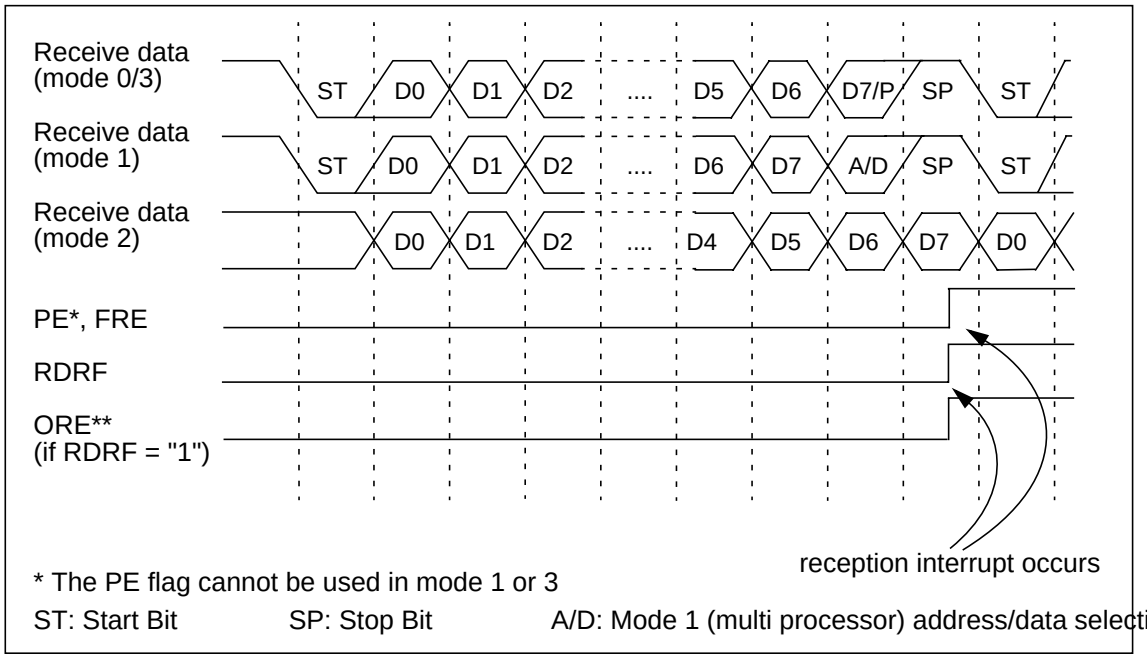


7.8 Interrupt Generation and Flag Set Timing

7.8.1 Reception Interrupt and Flags

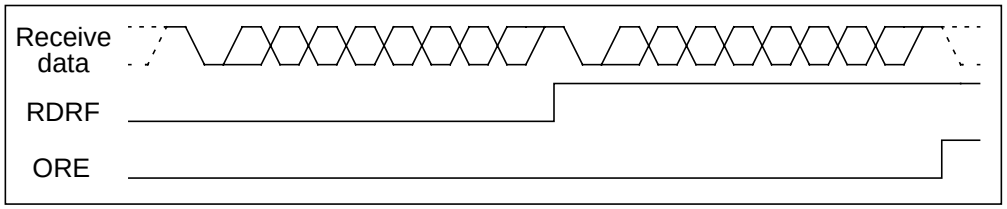
Generally a reception interrupt is generated, if the received data is complete (RDRF = 1) or reception errors have occurred (PE, ORE, or FRE) and the Reception Interrupt Enable (RIE) flag bit of the Serial Status Register (SSR) was set to "1". These interrupts are generated if the first stop bit is detected in mode 0 or 1 (except parity error), or the last data bit was read in mode 2.

Note: If a reception error has occurred, the Reception Data Register (RDR) contains invalid data in each mode.



Note: The example above shows not all possible reception options for mode 0 and 3. Here it is: "7p1" and "8N1" (p = "E" or "O").

**ORE only occurs, if the reception data is not read by the CPU (RDRF = 1) and another data frame is read:

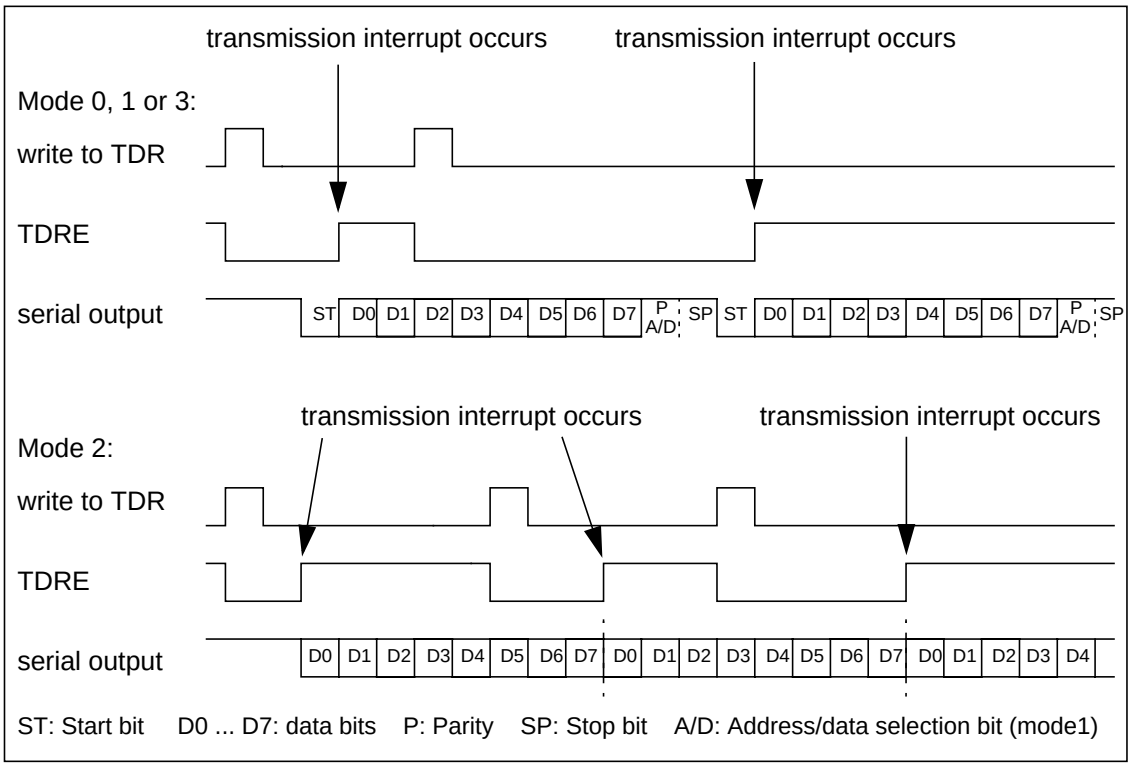


7.8.2 Transmission Interrupt and Flags

A transmission interrupt is generated, when the next data to be send is ready to be written to the Transmission Data Register (TDR), i. e. the TDR is empty, and the transmission interrupt is enabled by setting the Transmission Interrupt Enable (TIE) bit of the Serial Status Register (SSR) to "1".

The Transmission Data Register Empty (TDRE) flag bit of the SSR indicates an empty TDR. Because the TDRE bit is "read only", it only can cleared by writing data into the TDR.

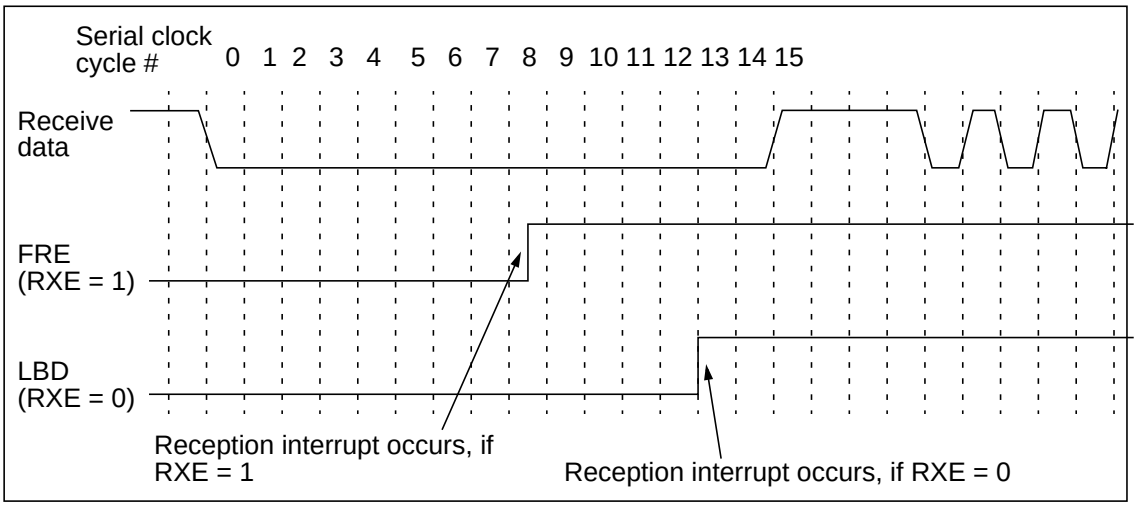
The following figure demonstrates the transmission operation and flag set timing for the three modes of the UART:



Note: The example above shows not all possible transmission options for mode 0. Here it is: "8p1" (p = "E" or "O"). Parity is not provided in mode 3.

7.8.3 LIN Synch Break Detection Interrupt and Flags

If a LIN synchronization break is detected in the slave mode, the LIN Break Detected (LBD) Flag of the ESCR is set to "1". This causes an interrupt, if the LIN Break Interrupt Enable (LBIE) flag bit is set.



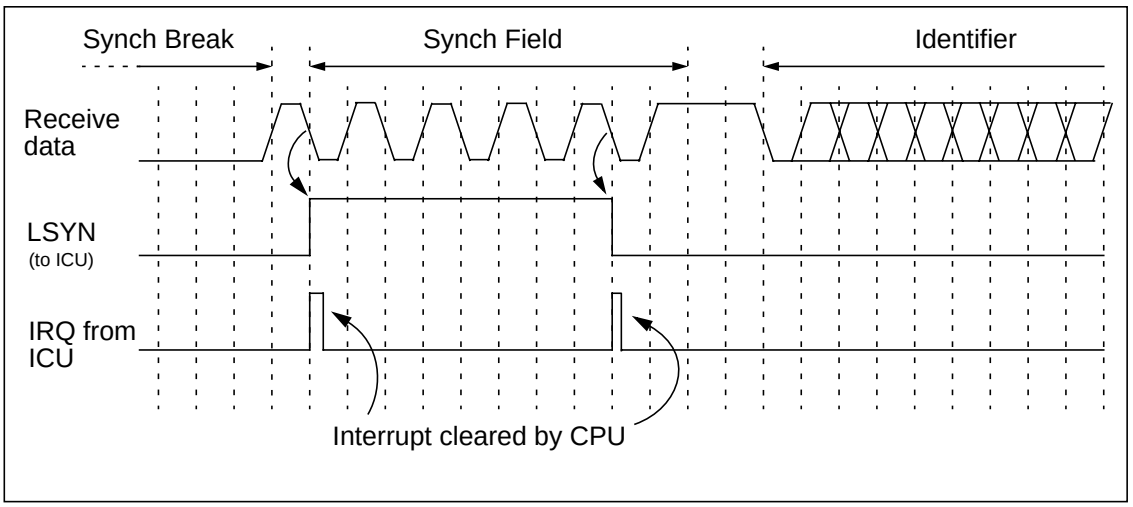
The figure above demonstrates the LIN synch break detection and flag set timing.

Note, that if reception is enabled (RXE = 1) and reception interrupt is enabled (RIE = 1) the Reception Data Framing Error (FRE) flag bit of the SSR will cause an reception interrupt 5 bit times ("8N1") earlier than the LIN break interrupt, so it is recommended to turn off RXE, if a LIN break is expected.

LBD is only supported in operation mode 0 and 3.

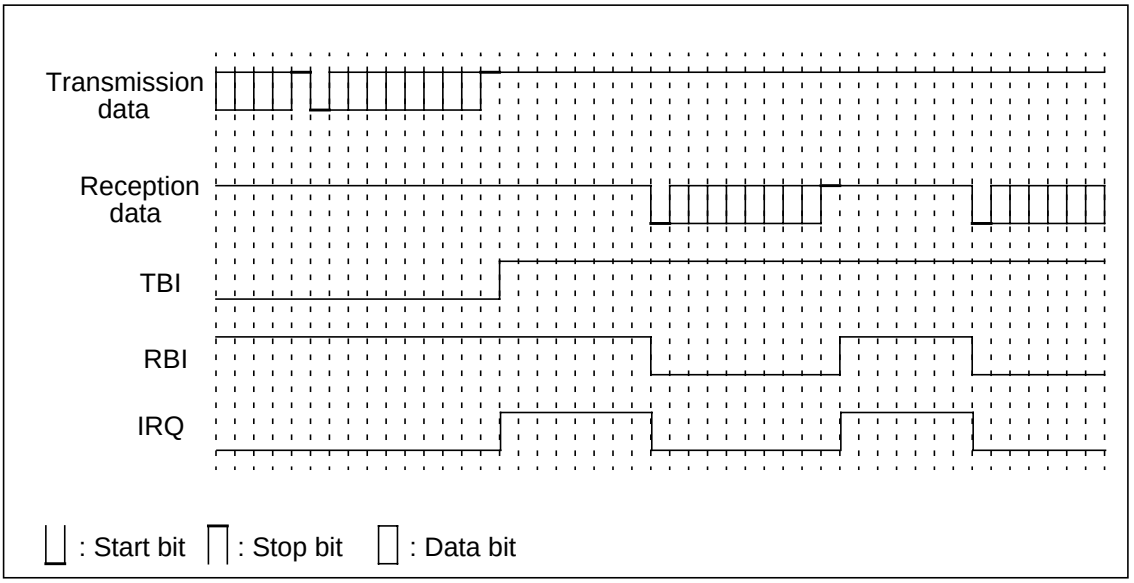
7.8.4 LIN Synch Field Detection Interrupt and Flags

After a LIN synch break detection the next falling edge on the serial input (SIN) sets the LSYN signal, which is internally connected to the Input Capture Unit (ICU). The fifth falling edge resets the LSYN signal. Therefore the ICU has to set to "both edge detection". The value of the ICU counter register after the first Interrupt has to be stored. The value after the second interrupt minus the first value is then the serial clock time multiplied by 8.



7.8.5 Bus Idle Interrupt and Flags

If both the serial input shift register and the serial output register are empty a bus idle interrupt is generated, if the Bus Idle Interrupt Enable (BIE) bit of the ECCR is set. The following figure illustrates the bus idle interrupt generation and the flag set timing:

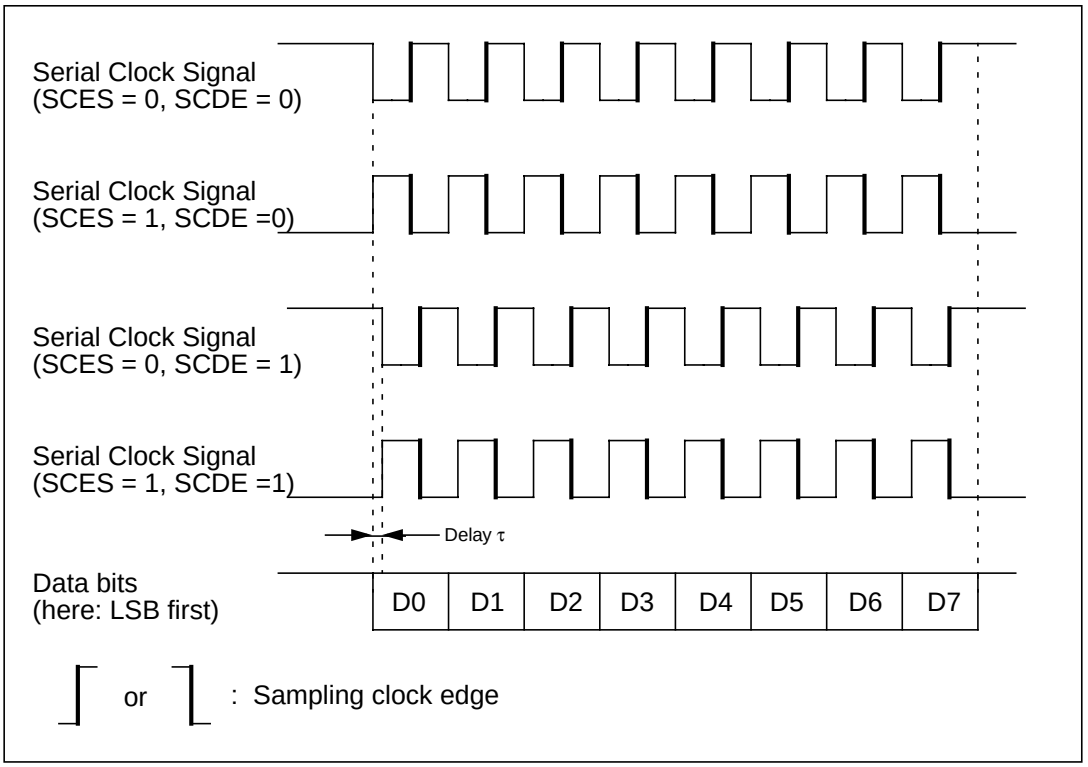


Note, the RBI flag goes also "1" if there is reception activity (reception bus is "0") but reception is disabled (RXE = 0). This is also valid if transmission is disabled (TXE = 0), but SOPE is "1" and writing "0" to SIOP.

7.9 Special features

7.9.1 Sampling Clock Edge Selection and clock delay

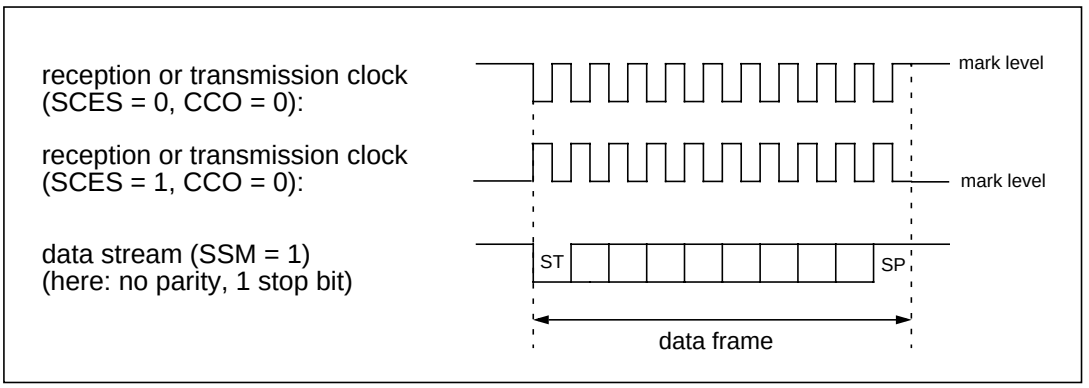
The Sampling Clock Edge Selection bit (SCES) of the ESCR determine in mode 2 the time when a reception bit is sampled to the reception shift register. This bit also inverts the generated clock signal, if the UART is in master mode 2. Setting the SCDE bit of the ECCR delays the clock signal for approx. 40 - 62 ns (depending on the MCU clock speed). The following figure illustrates this:



$$\tau = \frac{1}{\phi} \qquad \phi = \text{MCU clock cycle}$$

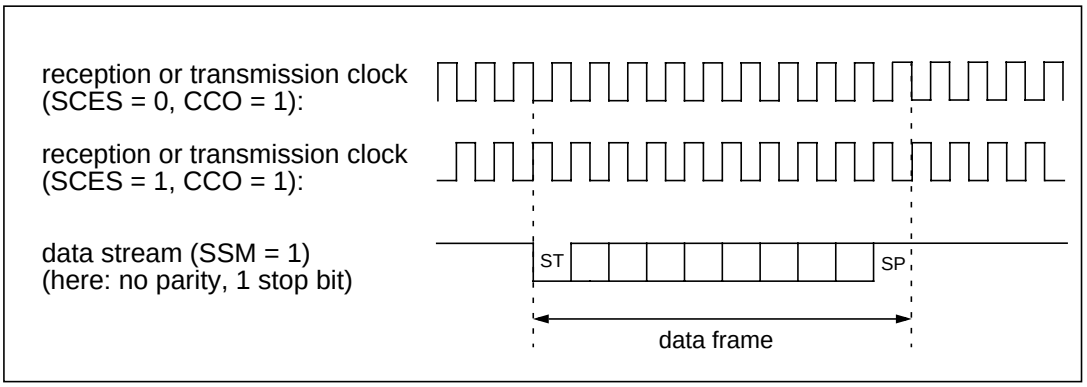
7.9.2 Synchronous Start-Stop-Bit-Mode

In synchronous operation mode 2 the SSM bit of the ECCR adds start-, stop-, and (if enabled) a parity bit to the data stream like in mode 0. Therefore all additional bits are clocked too:



7.9.3 Continuous serial clock output enable

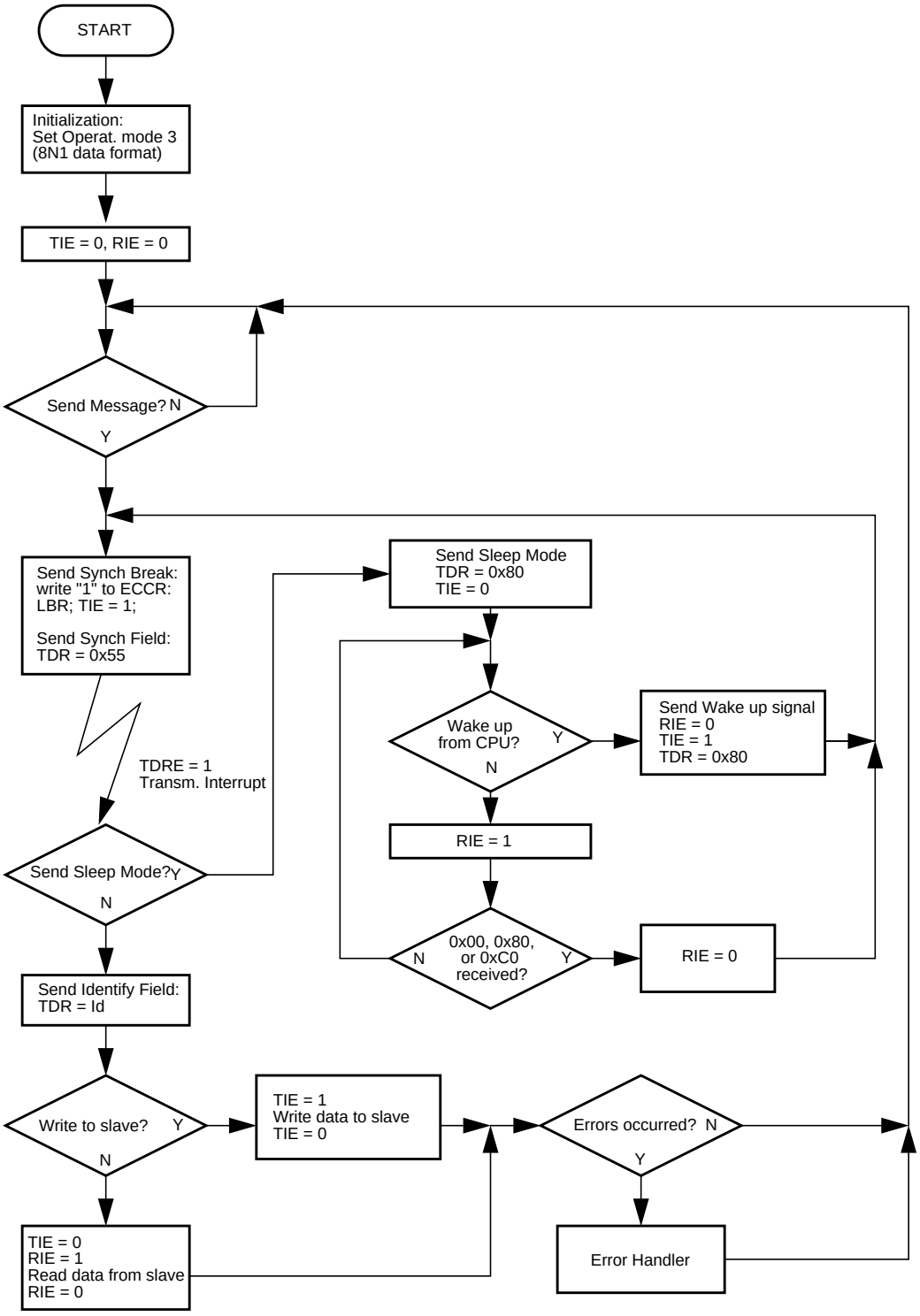
If the CCO bit of the ESCR is set and the UART is in mode 2, the serial clock is output directly to the SCK pin, synchronized to the shifter clocks. This is useful when using start stop bits in synchronous mode.



7.10 LIN Communication Function

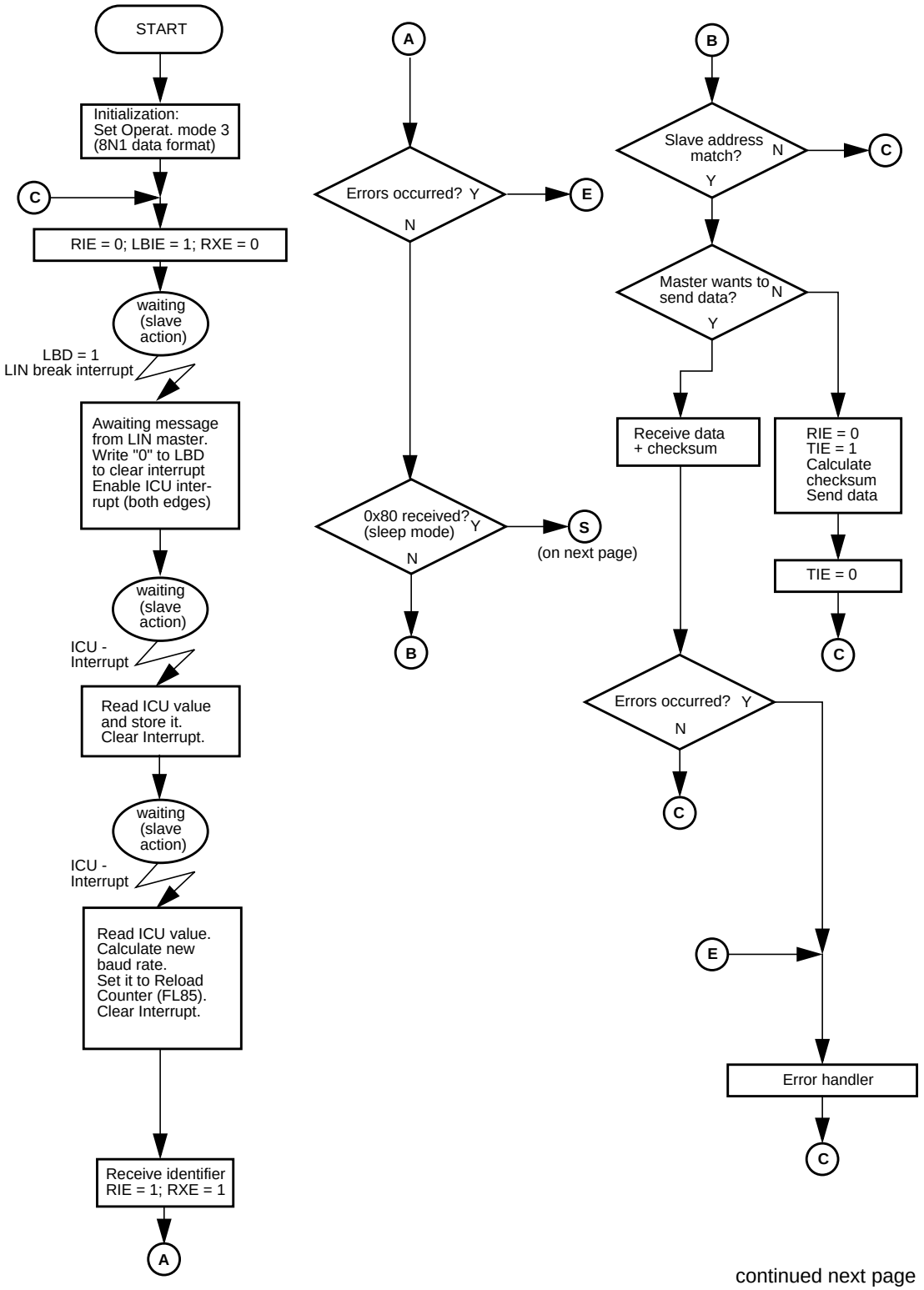
7.10.1 UART as Master device

The following flowchart example demonstrate how to process with a LIN bus system, if the UART acts as the bus master device:



7.10.2 UART as slave device

The following flowchart example demonstrate how to process with a LIN bus system, if the UART acts as a slave device:



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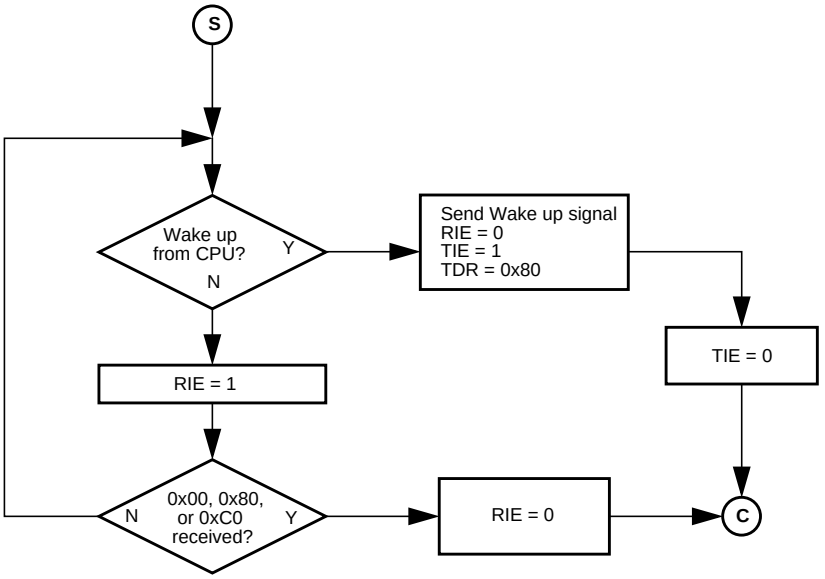

7.11 Summary of the Changes to previous UARTs

- Additional Extended Status/Control Register (ESCR), which provides:
  - — Special LIN features with Interrupt Generation
  - — Direct Access to the Serial Input / Output Pins (SIN, SOUT)
  - — Reception Sampling Clock Edge Selection (SCES) (Clock inversion)
  - — Continuos Serial Clock Output for mode 2 with start/stop bits
- Additional Extended Communication Control Register (ECCR), which provides:
  - — Reception Sampling Clock Edge Selection (SCES) (Clock inversion)
  - — SPI-Mode bit (SCDE; Delaying the Serial Clock Output)
  - — Start-Stop-Bit-Option in synchronous mode (SSM)
  - — Master **and** Slave communication in synchronous mode 2 (MS)
  - — Bus idle interrupt generation with two separate flag bits for Transmission Idle and Reception Idle
- Changes in the Serial Mode Register (SMR):
  - — A new mode (3) is added for LIN-slave function and for fixing the data format to "8N1", LSB first
  - — Clock Select bits were removed and replaced with control bits for the reload counter (see extra specification for details)
- Communication Prescaler Control Register (CPCR) was removed and replaced with two registers for the reload counter (BGR1, BGR0)
- Master **and** Slave function in Multiprocessor Mode (mode 1) is now provided

- Flag bits which belong to transmission/reception format always return "correct" values. For example: If the programmer tries to set the Parity flag in mode 3 (LIN), the PEN flag nevertheless will return a "0"

  Exceptions: In mode 1 the parity flag is always set (used to send / receive the AD bit).
  In mode 2 the parity flag can be set but is sent or received only if SSM is "1"
- Now also the second stop bit is checked during reception, if SBL is "1"
- UART provides a fife time oversampling in asynchronous mode
- UART generates a SEDGE (Start bit falling Edge detection) signal for the dedicated Baud Rate Generator to synchronize the Reception Clock to the incoming data
- UART provides hence version 2.0 NRZ **and** RZ signal mode.
- RMW functionallity of the AD bit provided for CPU bit manipulation instructions.

This UART is not software compatible to older UART modules

8 Electrical specification

8.1 Absolute Maximum Ratings

see MB91360 Hardware Manual

8.2 Operating Conditions

Parameter	Symbol	min.	typ.	max.	Unit	Condition
Operating temperature	Ta	-40		85	°C	
Supply voltage - Digital supply - Core supply	 VDD VDDC	 4.75 3.1	 5 3.3	 5.25 3.5	 V V	 int. regulator used int. regulator not used (under investigation!)

For the other parameters see MB91360 Hardware Manual

8.3 Clock Settings

The maximum allowed core clock (CLKB) frequency setting is 32 MHz. For settings of the others clocks see MB91360 Hardware Manual.

8.4 Clock Modulator Settings

T.B.D.

9 Package

The package FPT-120P-M21 will be used for MB91F364G.

The thermal resistance of this package is 30 degr. C/W when used on a muli-layer board with separate power and ground planes.

Thermal resistance [degr. C/W]			
theta-ja (junction to ambient)			theta-jc (junction to case)
0 m/s	1 m/s	3 m/s	
30	27	25	5

The maximum allowed ambient temperature is 85 degr. C, the maximum allowed junction temperature is 125 degr.C. Under these conditions a maximum power consumption of (125 degr. C - 85 degr. C) / 30 C/W = 1.33 W is allowed. The user must make sure that the maximum ambient temperature is not exceeded.

For other details about the package see Fujitsu Semiconductor Package Data Book.

Appendix A I/O Map

Version 1.4, 2000/03/13

Table A lists the addresses for the registers used by the internal peripheral functions of the MB91FV360G.

- How to Read the I/O Map

Address	Register				Internal peripheral
	+0	+1	+2	+3	
000014_H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] ----XXXX	—	Port data register

Read/write attribute
Register initial value after a reset (bit initial values)
"1": initial value "1", "0": initial value "0",
"x": initial value "X" (indeterminate),
"—" indicates non-existent bits
Register name (The register in column 1 is at location 4n, the register in column 2 at 4n+1, and so on.)
Location of far left of register (+0). +1, +2, and +3 each increment the location by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Precautions:

- Do not use RMW instructions on registers containing write-only (W) bits.

RMW instructions(RMW:read-modify-write)

```
AND   Rj, @Ri      OR    Rj, @Ri      EOR   Rj, @Ri
ANDH  Rj, @Ri      ORH   Rj, @Ri      EORH  Rj, @Ri
ANDB  Rj, @Ri      ORB   Rj, @Ri      EORB  Rj, @Ri
BANDL #u4, @Ri     BORL  #u4, @Ri     BEORL #u4, @Ri
BANDH #u4, @Ri     BORH  #u4, @Ri     BEORH #u4, @Ri
```

- The data in reserved areas and areas marked "—" is indeterminate. Do not use those areas !

Address	Register				Block
	+0	+1	+2	+3	
000000_H - $00000C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000010_H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] X - - - X - - -	PDRJ [R/W] XXXXXXXX	R-bus Port Data Register
000014_H	PDRK [R/W] XXXXXXXX	PDRL [R/W] XXXXXXXX	PDRM [R/W] - - - - XXXX	PDRN [R/W] - - XXXXXX	
000018_H	PDRO [R/W] XXXXXXXX	PDRP [R/W] - - XXXXX	PDRQ [R/W] - - XXXXX	PDRR [R/W] XXXXXXXX	
$00001C_H$	PDRS [R/W] XXXXXXXX	PDRT --XXXXXX			
000020_H | $00003C_H$					Reserved
000040_H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	CLKR2 [R/W] - - - - - 000	reserved	DLYI/I-unit RTC
000048_H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
$00004C_H$	_____		TMCSR0 [R/W] - - - - 0000 - - - 00000		
000050_H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054_H	_____		TMCSR1 [R/W] - - - - 0000 - - - 00000		
000058_H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
$00005C_H$	_____		TMCSR2 [R/W] - - - - 0000 - - - 00000		
000060_H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00 - - 0 - 0 -	UART0
000064_H	ULS0 [R/W] - - - - 0000	--------	--------	--------	
000068_H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] - - - - - - - -	UTIMC0 [R/W] 0 - - - 0 - 01	U-TIMER 0
$00006C_H$ - 000080_H	Reserved				
000084_H	SMCS0 [R/W] 00000010 - - - - 00-0		SES0 [R/W] - - - - - - 00	SDR0 [R/W] 00000000	SIO 0
000088_H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00008C_H$	CDCR0 [R/W] 0 - - - 1111	Reserved	Reserved	Reserved	SIO 0 Prescaler
000090_H - 000098_H	Reserved				
$00009C_H$	ADMD [R/W,W] - - - X0000	ADCH [R/W] 00000000		ADCS [R/W,W] 0000 - - 00	A/D Converter
$0000A0_H$	ADCD [R/W] 000000XX XXXXXXXX			ADBL [R/W] - - - - - - - 0	
$0000A4_H$		DACR [R/W] - - - - - 000	DADR0 [R/W] - - - - - - XX XXXXXXXX		DAC
$0000A8_H$	DADR1 [R/W] - - - - - - XX XXXXXXXX			DDBL [R/W] - - - - - - - 0	
$0000AC_H$	IOTDBL0 [R/W] - - - - - 000	ICS01 [R/W] 00000000	IOTDBL1 [R/W] - - - - - 000	ICS23 [R/W] 00000000	Input Capture 0,1,2,3
$0000B0_H$	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
$0000B4_H$	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$0000B8_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Com- pare 0,1,2.3
$0000BC_H$	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
$0000C0_H$	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
$0000C4_H$					Reserved
$0000C8_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		_____	TCCS0 [R/W] - 0000000	Free Running Counter 0 for ICU/OCU
$0000CC_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		_____	TCCS1 [R/W] - 0000000	Free Running Counter 1 for ICU/OCU
$0000D0_H$ - $0000F0_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0000F4_H$		WTDBL [R/W] - - - - - - - 0	WTCR [R/W] 00000000 000 - 0000		Real Time Clock (WatchTimer)
$0000F8_H$		WTBR [R/W] - - XXXXXX XXXXXXXX XXXXXXXX			
$0000FC_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000		
000100_H - 000114_H	Reserved				
000118_H	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] - - - 00000	GCN20 [R/W] - - - - 0000	PWM Control 0
$00011C_H$	Reserved				
000120_H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124_H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	
000128_H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
$00012C_H$	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130_H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134_H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138_H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
$00013C_H$	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140_H - 000160_H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000164_H	CMCR [R/W] 11111111 0000000		CMPR [R/W] ----1001 1---0001		Clock Modulation
000168_H	CMLS0 [R/W] 01110111 1111111		CMLS1 [R/W] 01110111 1111111		
$00016C_H$	CMLS2 [R/W] 01110111 1111111		CMLS3 [R/W] 01110111 1111111		
000170_H	CMLT0 [R/W] -----100 00000010		CMLT1 [R/W] 11110100 00000010		
000174_H	CMLT2 [R/W] -----100 00000010		CMLT3 [R/W] -----100 00000010		
000178_H	CMAC [R/W] 11111111 1111111		CMTS [R/W] --000001 01111111		
$00017C_H$	Reserved				
000180_H					
000184_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] - - - - - - 00	ITBAL [R/W] 00000000	I2C
000188_H	ITMKH [R/W] 00 - - - - 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	
$00018C_H$	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2 [R/W] - - - - - - - 0	
000190_H	CUCR [R/W] -------- ---0--00		CUTD [R/W] 10000000 00000000		Calibration Unit of 32kHz oscillator
000194_H	CUTR1 [R] -------- 00000000		CUTR2 [R] 00000000 00000000		
000198_H	SCR5 [R/W,W] 00000000	SMR5 [R/W,W] 00000000	SSR5 [R/W,R] 00001000	RDR5/TDR5 [R/W] 00000000	LIN UART0
$00019C_H$	ESCR5 [R/W} 00000X00	ECCR5 [R/W,R,W] -00000XX	BGR15 [R/W] -0000000	BGR05 [R/W] 00000000	
$0001A0_H$	SCR6 [R/W,W] 00000000	SMR6 [R/W,W] 00000000	SSR6 [R/W,R] 00001000	RDR6/TDR6 [R/W] 00000000	LIN UART1
$0001A4_H$	ESCR6 [R/W} 00000X00	ECCR6 [R/W,R,W] -00000XX	BGR16 [R/W] -0000000	BGR06 [R/W] 00000000	
$0001A8_H$ | $0001F8_H$	Reserved				
$0001FC_H$			F362MD [R/W] 00000000	SFR [R/W] -------0 SFR_BDEN	F362 Mode, Special Function Register (BDSU enable)

Address	Register				Block
	+0	+1	+2	+3	
000200_H | $0003EC_H$	_____				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H	DDRG [R/W] 00000000	DDRH [R/W] 00000000	DDRI [R/W] ----0---	DDRJ [R/W] 00000000	R-bus Port Direction Register
000404_H	DDRK [R/W] 00000000	DDRL [R/W] 00000000	DDRM [R/W] ----0000	DDRN [R/W] --000000	
000408_H	DDRO [R/W] 00000000	DDRP [R/W] ----0000	DDRQ [R/W] --000000	DDRR [R/W] 00000000	
$00040C_H$	DDRS [R/W] 00000000	DDRT [R7W] --000000			
000410_H	PFRG [R/W] 00000000	PFRH [R/W] 00000000	PFRI [R/W] ----0---	PFRJ [R/W] 00000000	R-bus Port Function Register
000414_H	PFRK [R/W] 00000000	PFRL [R/W] 00000000	PFRM [R/W] ----0000	PFRN [R/W] --000000	
000418_H	PFRO [R/W] 00000000	PFRP [R/W] 00000000	PFRQ [R/W] --000000	PFRR [R/W] 00000000	
$00041C_H$	PFRS [R/W] 00000000	PFRT [R/W] --000000			
000420_H | $00043C_H$	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H | $00047C_H$	_____				
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] X0000X00	CTBR [W] XXXXXXXX	Clock Control unit
000484_H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H | $00063C_H$	_____				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000640_H	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit Note: only use registers required for the controlling of the CS7X area and to avoid overlapping CSnX areas, other registers have no funcion
000644_H	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648_H	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
$00064C_H$	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650_H	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654_H	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658_H	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		
$00065C_H$	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660_H	AMD0 [R/W] -00XX111	AMD1 [R/W] -XXXXXXX	AMD2 [R/W] --XXXXXX	AMD3 [R/W] --XXXXXX	
000664_H	AMD4 [R/W] --XXXXXX	AMD5 [R/W] --XXXXXX	AMD6 [R/W] -XXXXXXX	AMD7 [R/W] -XXXXXXX	
000668_H	CSE 11000011	_____	_____	_____	
$00066C_H$	_____		_____		
000670_H	CHE 11111111	_____	_____		
000674_H | $0007F8_H$	_____				Reserved
$0007FC_H$	_____	MODR [W] XXXXXXXX	_____	_____	Mode Register

Address	Register				Block
	+0	+1	+2	+3	
000800_H	BCTRL [R/W] 00000000 -0000000 00000000 00000000				BDSU
000804_H	BSTAT [R/W] 00000000 1---0000		--------	--------	
000808_H	BIA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00080C_H$	BIA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000810_H	BIA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000814_H	BIA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000818_H	BIAM0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00081C_H$	BIAM1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000820_H	BOA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000824_H	BOA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000828_H	BOAM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00082C_H$	BDT0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000830_H	BDT1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000834_H	BDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000840_H to $006FFC_H$	Reserved				
007000_H	FMCS [R/W] 0110X000	_____	_____	_____	Flash Memory Control Register
007004_H	FMWT [R/W] --010011	_____	_____	_____	

Address	Register				Block
	+0	+1	+2	+3	
007008_H | $03CFFC_H$	_____				Reserved
$03D000_H$ | $03FFFC_H$					User RAM 12 kB (D-Bus)
040000_H | $040FFC_H$					Fast RAM 4 kB (F-Bus)
041000_H | 0FEFFC	_____				Reserved
050000_H | $0507FC_H$					Boot ROM 2 kB (F-Bus)
050800_H | $0BFFFC_H$	_____				reserved
$0C0000_H$ | 0DFFFC	Sector 0 64 KB		Sector 5 64 KB		Flash Memory 256 K on F-Bus
$0E0000_H$ | 0EFFFC	Sector 1 32 KB		Sector 6 32 KB		
$0F0000_H$ | $0F3FFC_H$	Sector 2 8 KB		Sector 7 8 KB		
$0F4000_H$ | $0F7FFC_H$	Sector 3 8 KB		Sector 8 8 KB		
$0F8000_H$ | $0FFFF4_H$	Sector 4 16 KB		Sector 9 16 KB		
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				Fixed Reset/Mode Vector
$0FFFFC_H$	FRV [R] $00\ 05\ 00\ 00_H$				

Write operations to address $0FFFF8_H$ and $0FFFFC_H$ are not possible. When reading these addresses, the values shown above will be read.

Address	Register				Block
	+0	+1	+2	+3	
100000_H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0 Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100004_H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
100008_H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
$10000C_H$	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
100010_H	CSR0 [R/W] 00000000 00000001			LEIR0 [R/W] 000-0000	
100014_H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
100018_H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
$10001C_H$	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
100020_H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100024_H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100028_H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10002C_H$ | 100048_H	GENERAL PURPOSE RAM [R/W]				
$10004C_H$	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100050_H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100054_H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100058_H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10005C_H$	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100060_H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100064_H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100068_H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 0
$10006C_H$	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100070_H	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100074_H	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100078_H	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10007C_H$	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100080_H	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100084_H	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100088_H	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
$10008C_H$	DLCR00 [R/W] -------- ----XXXX		DLCR10 [R/W] -------- ----XXXX		
100090_H	DLCR20 [R/W] -------- ----XXXX		DLCR30 [R/W] -------- ----XXXX		
100094_H	DLCR40 [R/W] -------- ----XXXX		DLCR50 [R/W] -------- ----XXXX		
100098_H	DLCR60 [R/W] -------- ----XXXX		DLCR70 [R/W] -------- ----XXXX		
$10009C_H$	DLCR80 [R/W] -------- ----XXXX		DLCR90 [R/W] -------- ----XXXX		
$1000A0_H$	DLCR100 [R/W] -------- ----XXXX		DLCR110 [R/W] -------- ----XXXX		
$1000A4_H$	DLCR120 [R/W] -------- ----XXXX		DLCR130 [R/W] -------- ----XXXX		
$1000A8_H$	DLCR140 [R/W] -------- ----XXXX		DLCR150 [R/W] -------- ----XXXX		
$1000AC_H$	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000B4_H$	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$1000BC_H$	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
$1000C4_H$	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000CC_H$	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000D4_H$	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000DC_H$	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000E4_H$	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000EC_H$	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000F4_H$	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$1000FC_H$	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100104_H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10010C_H$	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100114_H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10011C_H$	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100124_H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$10012C_H$	CREG0 [R/W] 00000000 00000110				

Appendix B Interrupt Vectors

This appendix lists the interrupt vector table.

The interrupt vector table lists the interrupt vectors and interrupt control registers assigned to each MB91360 interrupt.
MB91F364G has no DMA controller. Therefore, the RN column stays empty.

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN
Reset	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
System reserved	5	05	-	-	0x3E8	0x000FFFE8	
System reserved	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap *4	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap *4	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction *4	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break exception *4	10	0A	-	-	0x3D4	0x000FFFD4	
Operand break trap *4	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap *4	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt(tool)*4	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction exception	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	
External Interrupt 1	17	11	ICR01	0x441	0x3B8	0x000FFFB8	
External Interrupt 2	18	12	ICR02	0x442	0x3B4	0x000FFFB4	
External Interrupt 3	19	13	ICR03	0x443	0x3B0	0x000FFFB0	

External Interrupt 4	20	14	ICR04	0x444	0x3AC	0x000FFFAC	
External Interrupt 5	21	15	ICR05	0x445	0x3A8	0x000FFFA8	
External Interrupt 6	22	16	ICR06	0x446	0x3A4	0x000FFFA4	
External Interrupt 7	23	17	ICR07	0x447	0x3A0	0x000FFFA0	
Reload Timer 0	24	18	ICR08	0x448	0x39C	0x000FFF9C	
Reload Timer 1	25	19	ICR09	0x449	0x398	0x000FFF98	
Reload Timer 2	26	1A	ICR10	0x44A	0x394	0x000FFF94	
CAN 0 RX	27	1B	ICR11	0x44B	0x390	0x000FFF90	
CAN 0 TX/NS	28	1C	ICR12	0x44C	0x38C	0x000FFF8C	
Not used on MB91F364G	29	1D	ICR13	0x44D	0x388	0x000FFF88	
	30	1E	ICR14	0x44E	0x384	0x000FFF84	
	31	1F	ICR15	0x44F	0x380	0x000FFF80	
	32	20	ICR16	0x450	0x37C	0x000FFF7C	
	33	21	ICR17	0x451	0x378	0x000FFF78	
	34	22	ICR18	0x452	0x374	0x000FFF74	
PPG 0/1	35	23	ICR19	0x453	0x370	0x000FFF70	
PPG 2/3	36	24	ICR20	0x454	0x36C	0x000FFF6C	
Not used on MB91F364G	37	25	ICR21	0x455	0x368	0x000FFF68	
	38	26	ICR22	0x456	0x364	0x000FFF64	
	39	27	ICR23	0x457	0x360	0x000FFF60	
	40	28	ICR24	0x458	0x35C	0x000FFF5C	
	41	29	ICR25	0x459	0x358	0x000FFF58	
ICU 0/1	42	2A	ICR26	0x45A	0x354	0x000FFF54	
OCU 0/1	43	2B	ICR27	0x45B	0x350	0x000FFF50	
ICU 2/3	44	2C	ICR28	0x45C	0x34C	0x000FFF4C	
OCU 2/3	45	2D	ICR29	0x45D	0x348	0x000FFF48	
ADC	46	2E	ICR30	0x45E	0x344	0x000FFF44	
Timebase Overflow	47	2F	ICR31	0x45F	0x340	0x000FFF40	
Free Running Counter 0	48	30	ICR32	0x460	0x33C	0x000FFF3C	
Free Running Counter 1	49	31	ICR33	0x461	0x338	0x000FFF38	
SIO 0	50	32	ICR34	0x462	0x334	0x000FFF34	

Not used on MB91F364G	51	33	ICR35	0x463	0x330	0x000FFF30	
	52	34	ICR36	0x464	0x32C	0x000FFF2C	
UART 0 RX	53	35	ICR37	0x465	0x328	0x000FFF28	
UART 0 TX	54	36	ICR38	0x466	0x324	0x000FFF24	
LIN UART 0 RX	55	37	ICR39	0x467	0x320	0x000FFF20	
LIN UART 0 TX	56	38	ICR40	0x468	0x31C	0x000FFF1C	
LIN UART 1 RX	57	39	ICR41	0x469	0x318	0x000FFF18	
LIN UART 1 TX	58	3A	ICR42	0x46A	0x314	0x000FFF14	
I2C	59	3B	ICR43	0x46B	0x310	0x000FFF10	
Not used on MB91F364G	60	3C	ICR44	0x46C	0x30C	0x000FFF0C	
RTC (Watchtimer) / Calibration Unit	61	3D	ICR45	0x46D	0x308	0x000FFF08	
Not used on MB91F364G	62	3E	ICR46	0x46E	0x304	0x000FFF04	
Delayed interrupt activation bit	63	3F	ICR47	0x46F	0x300	0x000FFF00	
System reserved *3	64	40	-	-	0x2FC	0x000FFEFC	
System reserved *3	65	41	-	-	0x2F8	0x000FFEF8	
Security vector	66	42			0x2F4	0x000FFEF4	
System reserved	67	43	(ICR51)	0x473	0x2F0	0x000FFEF0	
System reserved	68	44	(ICR52)	0x474	0x2EC	0x000FFEEC	
System reserved	69	45	(ICR53)	0x475	0x2E8	0x000FFEE8	
System reserved	70	46	(ICR54)	0x476	0x2E4	0x000FFEE4	
System reserved	71	47	(ICR55)	0x477	0x2E0	0x000FFEE0	
System reserved	72	48	(ICR56)	0x478	0x2DC	0x000FFEDC	
System reserved	73	49	(ICR57)	0x479	0x2D8	0x000FFED8	
System reserved	74	4A	(ICR58)	0x47A	0x2D4	0x000FFED4	
System reserved	75	4B	(ICR59)	0x47B	0x2D0	0x000FFED0	
System reserved	76	4C	(ICR60)	0x47C	0x2CC	0x000FFECC	
System reserved	77	4D	(ICR61)	0x47D	0x2C8	0x000FFEC8	
System reserved	78	4E	(ICR62)	0x47E	0x2C4	0x000FFEC4	
System reserved	79	4F	(ICR63)	0x47F	0x2C0	0x000FFEC0	
Used by the INT instruction.	80 to 255	50 to FF	-	-	0x2BC to 0x000	0x000FFEBC to 0x000FFC00	

*1 The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
*2 The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset.After execution of the internal boot ROM TBR is set to 0_x00FFC00.
*3 Used by REALOS
*4 System reserved

Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.
Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

vctadr = TBR + vctofs

= TBR + ($3FC_H$ – 4 × vct)

vctadr : Vector address
vctofs : Vector offset
vct : Vector number