

## MM74HCT164

### 8-Bit Serial-in/Parallel-out Shift Register

#### General Description

The MM74HCT164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HCT logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

#### Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40  $\mu$ A maximum (74HCT Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

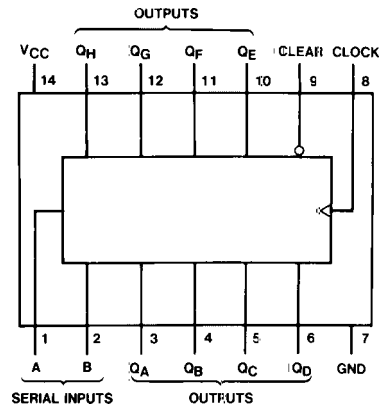
#### Ordering Code:

| Order Number | Package Number | Package Description                                                          |
|--------------|----------------|------------------------------------------------------------------------------|
| MM74HCT164M  | M14A           | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HCT164SJ | M14D           | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide                |
| MM74HCT164N  | N14A           | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

MM74HCT164 8-Bit Serial-in/Parallel-out Shift Register

## Connection Diagram



Top View

## Truth Table

| Inputs |       |   |   | Outputs         |                 |     |                 |
|--------|-------|---|---|-----------------|-----------------|-----|-----------------|
| Clear  | Clock | A | B | Q <sub>A</sub>  | Q <sub>B</sub>  | ... | Q <sub>H</sub>  |
| L      | X     | X | X | L               | L               |     | L               |
| H      | L     | X | X | Q <sub>AO</sub> | Q <sub>BO</sub> |     | Q <sub>HO</sub> |
| H      | ↑     | H | H | H               | Q <sub>An</sub> |     | Q <sub>Gn</sub> |
| H      | ↑     | L | X | L               | Q <sub>An</sub> |     | Q <sub>Gn</sub> |
| H      | ↑     | X | L | L               | Q <sub>An</sub> |     | Q <sub>Gn</sub> |

H = HIGH Level (steady state)

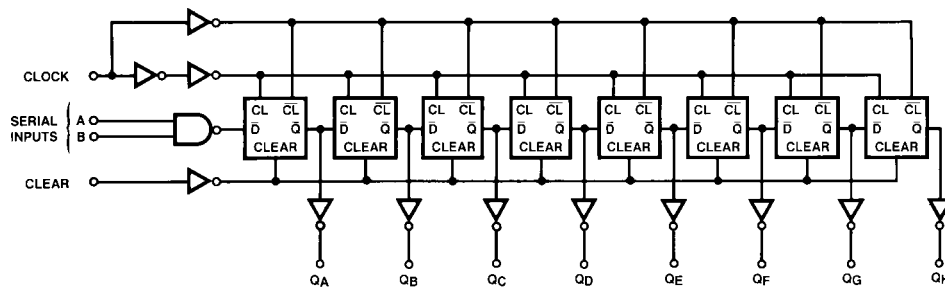
L = LOW Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from LOW-to-HIGH level.

Q<sub>AO</sub>, Q<sub>BO</sub>, Q<sub>HO</sub> = the level of Q<sub>A</sub>, Q<sub>B</sub>, or Q<sub>H</sub>, respectively, before the indicated steady state input conditions were established.Q<sub>An</sub>, Q<sub>Gn</sub> = The level of Q<sub>A</sub> or Q<sub>G</sub> before the most recent ↑ transition of the clock; indicated a one-bit shift.

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

(Note 2)

|                                                  |                       |
|--------------------------------------------------|-----------------------|
| Supply Voltage ( $V_{CC}$ )                      | -0.5 to +7.0V         |
| DC Input Voltage ( $V_{IN}$ )                    | -1.5 to $V_{CC}+1.5V$ |
| DC Output Voltage ( $V_{OUT}$ )                  | -0.5 to $V_{CC}+0.5V$ |
| Clamp Diode Current ( $I_{IK}, I_{OK}$ )         | $\pm 20$ mA           |
| DC Output Current, per pin ( $I_{OUT}$ )         | $\pm 25$ mA           |
| DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ ) | $\pm 50$ mA           |
| Storage Temperature Range ( $T_{STG}$ )          | -65°C to +150°C       |
| Power Dissipation ( $P_D$ )                      |                       |
| (Note 3)                                         | 600 mW                |
| S.O. Package Only                                | 500 mW                |
| Lead Temperature ( $T_L$ )                       |                       |
| (Soldering 10 seconds)                           | 260°C                 |

**Recommended Operating Conditions**

|                                                     | Min | Max      | Units |
|-----------------------------------------------------|-----|----------|-------|
| Supply Voltage ( $V_{CC}$ )                         | 4.5 | 5.5      | V     |
| DC Input or Output Voltage<br>( $V_{IN}, V_{OUT}$ ) | 0   | $V_{CC}$ | V     |
| Operating Temperature Range ( $T_A$ )               | -40 | +85      | °C    |
| Input Rise or Fall Times<br>( $t_r, t_f$ )          |     | 500      | ns    |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 2:** Unless otherwise specified all voltages are referenced to ground.**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** $V_{CC} = 5V \pm 10\%$  (unless otherwise specified)

| Symbol          | Parameter                         | Conditions                                                                                                                                                                                          | T <sub>A</sub> = 25°C         |                                       | T <sub>A</sub> = -40 to 85°C          | T <sub>A</sub> = -55 to 125°C       | Units |
|-----------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|---------------------------------------|---------------------------------------|-------------------------------------|-------|
|                 |                                   |                                                                                                                                                                                                     | Typ                           | Guaranteed Limits                     |                                       |                                     |       |
| V <sub>IH</sub> | Minimum HIGH Level Input Voltage  |                                                                                                                                                                                                     |                               | 2.0                                   | 2.0                                   | 2.0                                 | V     |
| V <sub>IL</sub> | Maximum LOW Level Input Voltage   |                                                                                                                                                                                                     |                               | 0.8                                   | 0.8                                   | 0.8                                 | V     |
| V <sub>OH</sub> | Minimum HIGH Level Output Voltage | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   = 20 μA<br> I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5V<br> I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5V | V <sub>CC</sub><br>4.2<br>5.2 | V <sub>CC</sub> - 0.1<br>3.98<br>4.98 | V <sub>CC</sub> - 0.1<br>3.84<br>4.84 | V <sub>CC</sub> - 0.1<br>3.7<br>4.7 | V     |
| V <sub>OL</sub> | Maximum LOW Level Voltage         | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>OUT</sub>   = 20 μA<br> I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5V<br> I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5V | 0<br>0.2<br>0.2               | 0.1<br>0.26<br>0.26                   | 0.1<br>0.33<br>0.33                   | 0.1<br>0.4<br>0.4                   | V     |
| I <sub>IN</sub> | Maximum Input Current             | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                                                                                                            |                               | ±0.1                                  | ±1.0                                  | ±1.0                                | μA    |
| I <sub>CC</sub> | Maximum Quiescent Supply Current  | V <sub>IN</sub> = V <sub>CC</sub> or GND<br>I <sub>OUT</sub> = 0 μA                                                                                                                                 |                               | 8.0                                   | 80                                    | 160                                 | μA    |
|                 |                                   | V <sub>IN</sub> = 2.4V or 0.4V (Note 4)                                                                                                                                                             |                               | 1.0                                   | 1.3                                   | 1.5                                 | mA    |

**Note 4:** This is measured per pin. All other inputs are held at  $V_{CC}$  ground.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$

| Symbol                | Parameter                                   | Conditions              | Typ | Guaranteed Limit | Units |
|-----------------------|---------------------------------------------|-------------------------|-----|------------------|-------|
| $f_{MAX}$             | Maximum Operating Frequency from Clock to Q | 50% Duty Cycle Clock    | 55  | 35               | MHz   |
| $t_{PHL}$ , $t_{PLH}$ | Maximum Propagation Delay Clock to Q        |                         | 17  | 27               | ns    |
| $t_{PHL}$             | Maximum Propagation Delay from Clear to Q   |                         | 23  | 38               | ns    |
| $t_{REM}$             | Minimum Removal Time, Clear to Clock        |                         | 3   | 6                | ns    |
| $t_S$                 | Minimum Set Up Time Data to Clock           | $t_H \geq 20\text{ ns}$ | 6   | 13               | ns    |
| $t_H$                 | Minimum Hold Time Clock to Data             | $t_S \geq 20\text{ ns}$ | 1.5 | 5                | ns    |
| $t_W$                 | Minimum Pulse Width Clock, Preset or Clear  |                         | 9   | 16               | ns    |

## AC Electrical Characteristics

$V_{CC} = 5.0V, \pm 10\%$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified)

| Symbol                | Parameter                                 | Conditions              | $T_A = 25^\circ C$ |     | $T_A = -40^\circ C \text{ to } 85^\circ C$ |     | $T_A = -55^\circ C \text{ to } 125^\circ C$ |     | Units |
|-----------------------|-------------------------------------------|-------------------------|--------------------|-----|--------------------------------------------|-----|---------------------------------------------|-----|-------|
|                       |                                           |                         | Typ                | Max | Min                                        | Max | Min                                         | Max |       |
| $f_{MAX}$             | Maximum Operating Frequency               | 50% Duty Cycle Clock    | 45                 | 30  |                                            | 25  |                                             | 22  | MHz   |
| $t_{PHL}$ , $t_{PLH}$ | Maximum Propagation Delay from Clock to Q |                         | 20                 | 30  |                                            | 38  |                                             | 45  | ns    |
| $t_{PHL}$             | Maximum Propagation Delay from Clear to Q |                         | 26                 | 41  |                                            | 51  |                                             | 61  | ns    |
| $t_{REM}$             | Minimum Removal Time Clear to Clock       |                         | 4                  | 8   |                                            | 10  |                                             | 14  | ns    |
| $t_S$                 | Minimum Setup Time Data to Clock          | $t_H \geq 20\text{ ns}$ | 7                  | 15  |                                            | 19  |                                             | 23  | ns    |
| $t_H$                 | Minimum Hold Time Clock to Data           | $t_S \geq 20\text{ ns}$ | 1.5                | 5   |                                            | 5   |                                             | 5   | ns    |
| $t_W$                 | Minimum Pulse Width Clock, or Clear       |                         | 10                 | 18  |                                            | 22  |                                             | 27  | ns    |
| $t_r$ , $t_f$         | Maximum Input Rise and Fall Time          |                         |                    | 500 |                                            | 500 |                                             | 500 | ns    |
| $t_{THL}$ , $t_{TLH}$ | Maximum Output Rise and Fall Time         |                         |                    | 15  |                                            | 19  |                                             | 22  | ns    |
| $C_{PD}$              | Power Dissipation Capacitance (Note 5)    | (per flip-flop)         | 160                |     |                                            |     |                                             |     | pF    |
| $C_{IN}$              | Maximum Input Capacitance                 |                         | 5                  | 10  |                                            | 10  |                                             | 10  | pF    |

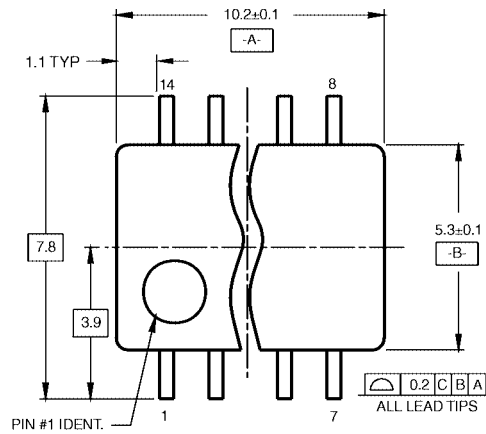
**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

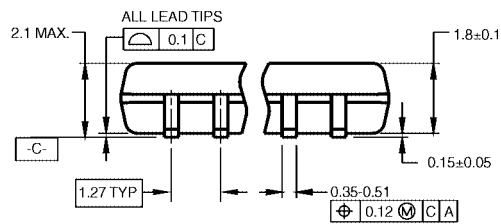


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



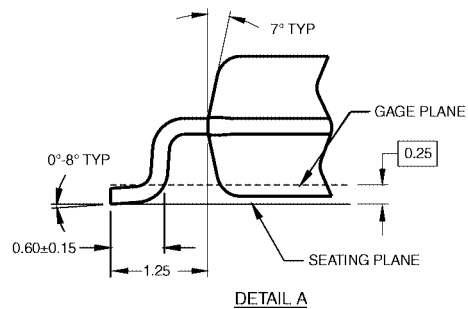
DIMENSIONS ARE IN MILLIMETERS



## NOTES:

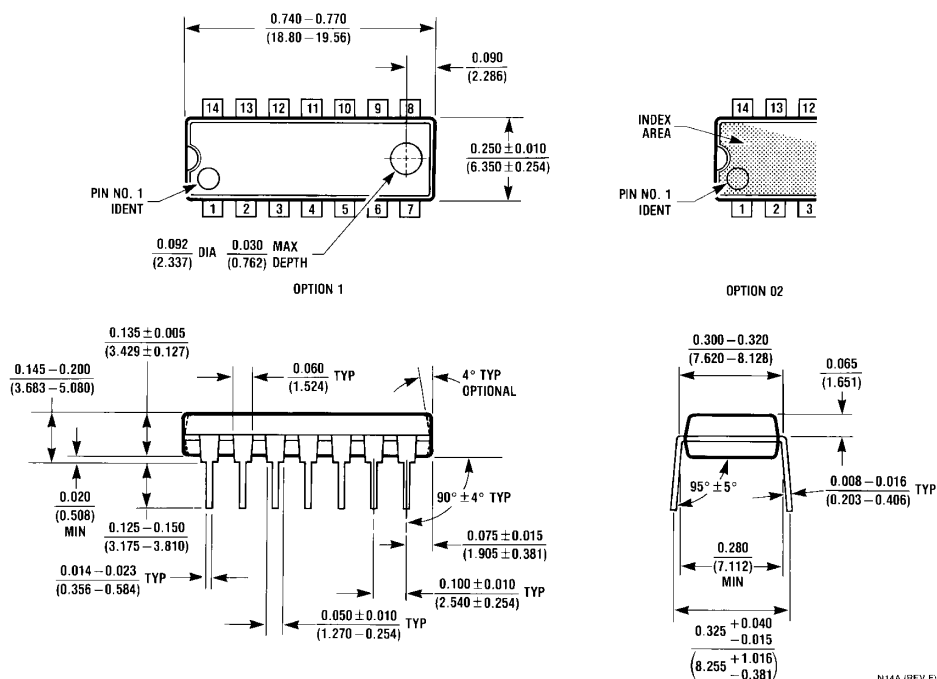
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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N14A

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