

□ MN103E010HRA, MN103E040HYB

Type	MN103E010HRA	MN103E040HYB
Command Cache	16 K-byte (4-way, set-associative)	
Data Cashe	16 K-byte (4-way, set-associative)	
SRAM Used by Both Instructions and Data	16 K-byte	
Package	BGA292-P-2727 *Lead-free	FLGA424-C-1717 *Lead-free
Minimum Instruction Execution Time	7.5 ns (at 1.8 V tolerance = ± 5%, 133 MHz)	
Interrupts	<ul style="list-style-type: none"> • XIRQ × 8 • NMI • Timer × 14 • DMAC × 4 • WDT • A/D • SIO × 6 • I²C × 2 • IrDA • Softmodem • Realtime clock • Asynchronous bus error 	
Timer Counter	<p>8-bit timer × 4 (all down counters)</p> <p>Cascade connection possible (usable as a 16/24/32-bit timer)</p> <p>Timer output possible (Duty = 1:1)</p> <p>Internal clock source or external clock source selectable</p> <p>Selectable as a serial interface clock</p> <p>16-bit timer × 7 (down counters)</p> <p>Cascade connection possible (usable as a 32-bit timer)</p> <p>Timer output possible (Duty = 1:1)</p> <p>Internal clock source or external clock source selectable</p> <p>Partially selectable as a serial interface clock</p> <p>16-bit timer × 1 (up counter)</p> <p>Internal clock source or external clock source selectable</p> <p>Input capture function (rising edge, falling edges, or both selectable)</p> <p>PWM generating function (compare/capture register × 2 contained)</p> <p>Watchdog timer × 1</p>	
DMA Contoroller	<p>Number of channels: 4</p> <p>Transfer unit: 1/2/4/16 byte</p> <p>Maximum number of bytes transferred: 1Mbyte</p> <p>Start factor: External request, interrupt, software</p> <p>Transfer mode: 2-bus cycle transfer</p> <p>Transfer mode: Batch transfer, intermittent transfer</p> <p>Addressing mode:</p> <p>Source/destination each fixed, increment/decrement specification possible</p> <p>Increment/decrement automatically executed according to the transfer unit</p>	
Serial Interface	<p>UART/synchronous (co-used) × 2-ch.</p> <p>UART (with CTS control) × 1-ch.</p>	
I/O Pins	I/O	34 • Common use : 33
FPU (floating point unit)	<ul style="list-style-type: none"> • Data types complying with the IEEE754 standard supported • Round to the nearest mode complying with the IEEE754 standard supported • 32 single-precision floating point operation registers (FS0-FS31) These can also be referenced as 16 double-precision floating point operation registers (FD0-FD30) • Floating point operation exceptions (5 types) and floating point unload instruction exceptions complying with the IEEE754 standard supported 	
Memory Management Function	<p>32-entry full-associative TLB loaded (instructions/data separated from each other)</p> <p>Address conversion by paging (page size: 1 K-byte, 4 K-byte, 128 K-byte, 4 M-byte variable)</p>	
On-chip Bus Controller	Concurrent access from three types of master devices to four types of slave devices possible	

System Bus Interface	External memory space allocation to 8 banks possible The external interface can use the built-in memory, RAM, ROM, SDRAM interfaces
Memory Bus Interface	SDRAM directly connected interface contained
Soft Modem Interface	<ul style="list-style-type: none"> Interface with an external AFE (analog front end) Output data parallel-serial conversion, input data serial-parallel conversion Send/receive FIFO contained (16-bit width, 16 steps) NCU control via the parallel IO port EYE-pattern output
Real-time Clock	<ul style="list-style-type: none"> Clock/calendar function Interrupt: periodic, alarm, update ended BCD/binary accommodated Leap year automatic correcting function 24-hour/12-hour selectable Daylight saving time mode accommodated
A/D Converter	<ul style="list-style-type: none"> 10-bit charge re-distribution mode (error: +4LSB) Number of channels: 8-channel
IrDA Interface	<ul style="list-style-type: none"> IrDA 1.0 SIR (-115.2 Kb/s, half-duplex) IrDA 1.1 MIR (0.576, 1.152 Mb/s, half-duplex) IrDA 1.1 FIR (4.0 Mbp/s, half-duplex) UART (-1.5 Mbp/s, full-duplex) 48 MHz clock input (baud rate generating function contained)
I²C Interface	2 ports Master-slave interface (multi-master supported) 3.3 V interface (open drain output)

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	I _{DD18A}	VDD18 = 1.8 V ; VDD33, PVDD, AVDD, RVDD = 3.3 V fOSC = 33.33 MHz (core 133 MHz) ; FRQS[1:0] = 0.0 ; Output open	-	-	460	mA
Supply current at stopping	I _{DD18D}	VDD18 = 1.89 V ; VDD33, PVDD, AVDD, RVDD = 3.465 V fOSC = Stop ; FRQS[1:0] = 0.0 ; Output open ; Tj = 70°C	-	-	50	mA

(Ta = -20°C to +70°C)

A/D conversion performance

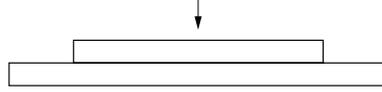
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution			-	-	10	Bit
A/D conversion relative error		VREFH = 3.3 V	-	-	±4	LSB
A/D conversion differential non-linear error		Conversion reference clock = 4.166 MHz	-	-	±4	LSB
A/D conversion time			2.6	-	-	µs

(Ta = -20°C to +70°C, AVDD = 3.3 V ± 0.165 V, AVSS = 0 V)

See the next page for pin assignment and support tool.

Pin Assignment

Perspective



ND	XSWE1	XSCS6	XSCS2	XSCS1	SD29	SD27	VDD18	SD21	SD19	SD14	VDD18	SD6	SD1	CLK48	PIO1[3]	PIO1[1]	PIO1[0]	ND	21			
	XSWE3	SD31	XSCS7	SD30	XSAS	SD23	SD22	SD17	SD16	SD9	SD8	SD3	SD4	PIO5[1]	PIO5[2]	PIO1[4]	PIO1[2]	ND	20			
RCLKI	XSCS3	XSWE0	XSWE2	XSCS0	XSCS4	SD28	SD25	SD24	SD18	VDD33	SD15	SD11	SD10	VDD33	PIO0[7]	PIO5[0]	AN1	AN3	AN7	VREFH	19	
RCLKO	PIO2[0]	PWROK	ND	ND	ND	SD26	SD20	SD13	SD12	SD7	SD2	SD0	SD5	PIO0[1]	ND	ND	ND	AN5	PIO0[5]	AVSS	18	
RVDD	PIO2[4]	PIO2[2]	ND	ND	ND	ND	AN6	AN0	AN2	17												
TCPOUT	PIO2[3]	XSDK	ND	ND	ND	ND	PIO0[3]	XIRQ7	AN4	16												
PVDD	SSZ0	XSBG	VDD33	ND	ND	ND	ND	XIRQ4	SBT2	PIO0[4]	AVDD	15										
PVSS	SA4	SA2	XSCS5	ND	ND	ND	ND	SBO0	XIRQ5	XNMI	XIRQ2	14										
OSCI	SA10	SA5	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	ND	SBO1	XIRQ0	PIO0[6]	PIO0[2]	13
OSCO	SA17	SA11	SA0	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	ND	VDD33	XRESET	PIO0[0]	XIRQ6	12
SYSCLK	SA18	SA12	XSRE	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	TRCST	VDD33	XIRQ3	VDD18	11	
PIO2[1]	SRXW	SSZ1	VDD33	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	SB11	SB12	SBO2	XIRQ1	10	
XSBR	SA1	SA3	SA14	ND	ND	ND	ND	VSS	VSS	VSS	VSS	VSS	ND	ND	ND	ND	PIO3[2]	PIO3[3]	XRSTOUT	VDD18	09	
VDD18	SA6	SA7	SA8	ND	ND	ND	ND	PIO3[0]	PIO3[1]	SBT0	SBT1	08										
SA9	SA13	SA15	SA22	ND	ND	ND	ND	TRST MOD	PIO4[0]	PIO4[2]	SBI0	07										
SA16	SA19	SA21	ND	ND	ND	ND	ND	PIO4[1]	PIO3[4]	TCK	06											
VDD18	SA23	VDD33	ND	ND	ND	ND	TRCD1	PIO4[3]	TDI	05												
SA27	SA26	SA24	ND	ND	ND	VDD33	VDD18	VDD33	VDD33	VDD33	VDD33	VDD18	TRCD2	TRCD7	ND	ND	ND	TRCD5	TMS	TDO	04	
SA29	SA31	SA25	SA20	SA28	MA4	MA1	MA7	MA13	MA11	MA12	XMBE0	MD9	MD4	MD12	MD1	MD15	TRCD4	TRCD0	EXTRG	TRCLK	03	
ND	SA30	MA3	MA5	MA0	MA8	MA14	XMCS1	SDCKE	XMWE	XCAS	MD6	MD10	MD11	MD2	MD14	TRCD3	TRCD6	ND	ND	ND	02	
	NP	MA2	MA6	MA10	MA9	XMCS0	XMRAS	SDCLK	XMBE1	MDK	MD7	MD8	MD5	SDCK1	MD3	MD13	MD0	ND	ND	ND	01	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	

FLGA424-C-1717 *Lead-free

- * ND has an electrode (pin) but N.C. is not guaranteed. Please design so as not to cause short circuit with other wiring on the user board.
- * The NDs on the four corners are the lands intended for reinforcement. You are required to connect them to the PCB.
- * NP (No pin.) has no electrode.

Pin Assignment(Continue)

Perspective

TRCD6	TRCD1	TDO	TRST MOD	PIO4[2]	PIO3[2]	SBI0	SBO1	SBT1	SBT2	XRST OUT	XIRQ1	XIRQ4	XIRQ5	PIO0[0]	PIO0[4]	AVDD	AN4	AVSS	VREFH	20			
TRCD3	EXTRG	TCK	PIO4[0]	PIO3[0]	PIO3[3]	SBO0	SBI1	SBI2	XIRQ0	XIRQ2	XNMI	XIRQ7	PIO0[2]	PIO0[6]	AN6	AN2	AN1	PIO1[2]	PIO5[0]	19			
TRCD7	TRCD4	TRCD0	TDI	TMS	PIO4[1]	PIO3[1]	PIO3[4]	SBT0	SBO2	XRESET	XIRQ3	XIRQ6	PIO0[1]	PIO0[5]	AN7	AN3	AN0	PIO1[1]	PIO5[2]	18			
MD0	TRCD2	TRCD5	VSS	VSS	PIO4[3]	VDD18	VDD33	VSS	VDD18	VDD33	VSS	PIO0[3]	VSS	PIO0[7]	AN5	PIO1[0]	PIO1[3]	PIO5[1]	CLK48	17			
MD13	TRC CLK	TRCST	VSS													VSS	PIO1[4]	SD3	SD0	16			
MD3	MD14	MD15	VSS													SD2	SD1	SD6	SD4	15			
sdcki	MD2	MD1	VDD33													VDD33	SD5	SD9	SD7	14			
MD5	MD11	MD12	VDD18	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SD8	SD12	SD10	13	
MD8	MD10	MD4	VDD33	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD18	SD11	SD15	SD13	12	
MD7	MD6	MD9	VSS	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33	SD14	SD17	SD16	11	
MDK	XMCAS	XMBE0	VDD33	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SD23	SD18	SD19	10	
XMBE1	XMWE	MA12	VSS	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD18	SD21	SD20	SD22	09	
SDCLK	SDCKE	MA11	VDD18	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SD25	SD24	SD26	08	
XMRAS	XMCE1	MA13	VDD33	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33	SD29	SD27	SD28	07	
XMCS0	MA14	MA7	VDD33	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	XSCS2	XSA5	SD30	SD31	06	
MA9	MA8	MA1	VSS	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	XSCS3	XSCS0	XSCS1	05	
MA10	MA0	MA4	VSS	VSS	SA22	VDD18	VDD33	VSS	VDD33	SA0	XSBR	XSRE	VDD18	VDD33	VSS	VSS	XSCS6	XSCS4	XSCS5	04			
MA6	MA5	SA31	SA26	SA23	SA19	SA16	SA13	SA9	SA10	SA1	XSBG	PIO2[4]	PIO2[3]	PIO2[0]	VSS	XSWE3	XSWE0	XSCS7	RCLKI	03			
MA2	MA3	SA28	SA25	SA21	SA18	SA15	SA12	SA8	SA6	SA2	SSZ0	SRXW	PIO2[2]	PIO2[1]	TCP OUT	PWROK	XSWE2	XSWE1	RCLKO	02			
SA30	SA29	SA27	SA24	SA20	SA17	SA14	SA11	SA7	SA5	SA4	SA3	SSZ1	XSDK	SYS CLK	OSCO	OSCI	PVSS	PVDD	RVDD	01			
				A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y

BGA292-P-2727 *Lead-free

Support Tool

- ROM Emulator PARTNER-ETII (KMC product)
- On-board Development Tools
 - PX-ODB103E-J (On-board debug unit)
 - PX-ODB-AMT-20 (Trace unit)
 - PARTNER-J (KMC product)

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