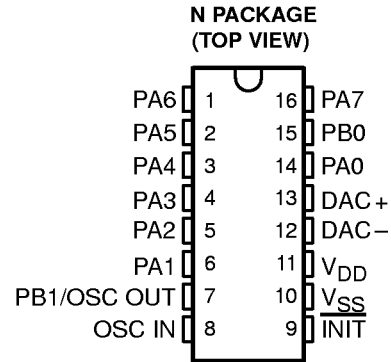


- Dual Programmable LPC-12 Speech Synthesizers
- Simultaneous LPC and PCM Waveforms
- 8-Bit Microprocessor with 61 instructions
- 32 Twelve-Bit Words and 224 Bytes of RAM
- 3.3V to 6.5V CMOS Technology for Low Power Dissipation
- Direct Speaker Drive Capability
- Mask Selectable Internal or External Clock
- Internal Clock Generator that Requires No External Components
- Two Software-Selectable Clock Speeds
- 10-kHz or 8-kHz Speech Sample Rate



description

The MSP50x3x family uses a revolutionary architecture to combine an 8-bit microprocessor, two speech synthesizers, ROM, RAM, and I/O in a low-cost single-chip system. The architecture uses the same arithmetic logic unit (ALU) for the two synthesizers and the microprocessor, thus reducing chip area and cost and enabling the microprocessor to do a multiply operation in 0.8 μ s. The MSP50x3x family features two independent channels of linear predictive coding (LPC), which synthesize high-quality speech at a low data rate. Pulse-code modulation (PCM) can produce music or sound effects. LPC and PCM can be added together to produce a composite result. For more information, see the MSP50x3x User's Guide (literature number SPSU006).

Table 1. MSP50x3x Family

DEVICE	AMOUNT OF ROM/PROM	FEATURES
MSP50C32	16K bytes mask ROM	9/10 I/O lines
MSP50C33	32K bytes mask ROM	9/10 I/O lines
MSP50C34	64K bytes mask ROM	9/10 I/O lines, 24 I/O lines in die form
MSP50P34	64K bytes PROM	9/10 I/O lines
MSP50C37	16K bytes mask ROM	18 I/O lines, A/D converter/analog amplifier
MSP50P37	16K bytes PROM	18 I/O lines, A/D converter/analog amplifier



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MSP50C32, MSP50C33, MSP50C34 MSP50P34, MSP50C37, MSP50P37 MIXED-SIGNAL PROCESSORS

SPSS019A – MAY 1997 – REVISED OCTOBER 1998

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{DD} (see Note 1)	–0.3 V to 8 V
Supply current, I_{DD} or I_{SS} (see Note 2)	100 mA
Input voltage range, V_I (see Note 1)	–0.3 V to $V_{DD} + 0.3$ V
Output voltage range, V_O (see Note 1)	–0.3 V to $V_{DD} + 0.3$ V
Storage temperature range	–30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground.

2. The total supply current includes the current out of all the I/O terminals and DAC terminals as well as the operating current of the device.

recommended operating conditions (MSP50C32, MSP50C33, MSP50x34)

			MAX	MAX	UNIT
V _{DD}	Supply voltage†		3.3	6.5	V
V _{IH}	High-level input voltage	V _{DD} = 3.3 V	2.5	3.3	V
		V _{DD} = 5 V	3.8	5	
		V _{DD} = 6 V	4.5	6	
V _{IL}	Low-level input voltage	V _{DD} = 3.3 V	0	0.65	V
		V _{DD} = 5 V	0	1	
		V _{DD} = 6 V	0	1.3	
T _A	Operating free-air temperature	Device functionality	0	70	°C
R _{speaker}	Minimum speaker impedance	Direct speaker drive using 2 pin push-pull DAC option	32		Ω

† Unless otherwise noted, all voltages are with respect to V_{SS} .

recommended operating conditions (MSP50x37)

			MIN	MAX	UNIT
V _{DD}	Supply voltage†		4	6.5	V
V _{IH}	High-level input voltage	V _{DD} = 4 V	3	4	V
		V _{DD} = 5 V	3.8	5	
		V _{DD} = 6 V	4.5	6	
V _{IL}	Low-level input voltage	V _{DD} = 4 V	0	1	V
		V _{DD} = 5 V	0	1.2	
		V _{DD} = 6 V	0	1.5	
	MUX input voltage	Reference voltage = 6.5 V	0	6.5	V
T _A	Operating free-air temperature	Device functionality	−10	70	°C
R _{speaker}	Minimum speaker impedance	Direct speaker drive using power amp	8		Ω



MSP50C32, MSP50C33, MSP50x34 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{T+}	Positive-going threshold voltage (INIT)	V _{DD} = 3.5 V	2			V
		V _{DD} = 6 V	3.4			
V _{T−}	Negative-going threshold voltage (INIT)	V _{DD} = 3.5 V	1.6			V
		V _{DD} = 6 V	2.3			
V _{hys}	Hysteresis (V _{T+} − V _{T−}) (INIT)	V _{DD} = 3.5 V	0.4			V
		V _{DD} = 6 V	1.1			
I _{lkg}	Input leakage current (except for OSC IN)		2			μA
I _{standby}	Standby current ($\overline{\text{INIT}}$ low, SETOFF)		10			μA
I _{DD} [†]	Supply current	V _{DD} = 3.3 V, V _{OH} = 2.75 V	2.1			mA
		V _{DD} = 5 V, V _{OH} = 4.5 V	3.1			
		V _{DD} = 6 V, V _{OH} = 5.5 V	4.5			
I _{OH}	High-level output current (PA, PB)	V _{DD} = 3.3 V, V _{OH} = 2.75 V	−4	−12	mA	
		V _{DD} = 5 V, V _{OH} = 4.5 V	−5	−14		
		V _{DD} = 6 V, V _{OH} = 5.5 V	−6	−15		
		V _{DD} = 3.3 V, V _{OH} = 2.2 V	−8	−20	mA	
		V _{DD} = 5 V, V _{OH} = 3.33 V	−14	−40		
		V _{DD} = 6 V, V _{OH} = 4 V	−20	−51		
I _{OL}	Low-level output current (PA, PB)	V _{DD} = 3.3 V, V _{OL} = 0.5 V	5	9	mA	
		V _{DD} = 5 V, V _{OL} = 0.5 V	5	9		
		V _{DD} = 6 V, V _{OL} = 0.5 V	5	9		
		V _{DD} = 3.3 V, V _{OL} = 1.1 V	10	19	mA	
		V _{DD} = 5 V, V _{OL} = 1.67 V	20	29		
		V _{DD} = 6 V, V _{OL} = 2 V	25	35		
I _{OH}	High-level output current (D/A)	V _{DD} = 3.3 V, V _{OH} = 2.75 V	−30	−50	mA	
		V _{DD} = 5 V, V _{OH} = 4.5 V	−35	−60		
		V _{DD} = 6 V, V _{OH} = 5.5 V	−40	−65		
		V _{DD} = 3.3 V, V _{OH} = 2.3 V	−50	−90	mA	
		V _{DD} = 5 V, V _{OH} = 4 V	−90	−140		
		V _{DD} = 6 V, V _{OH} = 5 V	−100	−150		
I _{OL}	Low-level output current (D/A)	V _{DD} = 3.3 V, V _{OL} = 0.5 V	50	80	mA	
		V _{DD} = 5 V, V _{OL} = 0.5 V	70	90		
		V _{DD} = 6 V, V _{OL} = 0.5 V	80	110		
		V _{DD} = 3.3 V, V _{OL} = 1 V	100	140	mA	
		V _{DD} = 5 V, V _{OL} = 1 V	140			
		V _{DD} = 6 V, V _{OL} = 1 V	150			
Pullup resistance		Resistors selected by software and connected between terminal and V _{DD}	10	20	50	kΩ
f _{osc(low)}	Oscillator frequency [‡]	V _{DD} = 5 V, T _A = 25°C, Target frequency = 15.36 MHz	14.89	15.36	15.86	MHz
f _{osc(high)}	Oscillator frequency [‡]	V _{DD} = 5 V, T _A = 25°C, Target frequency = 19.2 MHz	18.62	19.2	19.7	MHz

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The frequency of the internal clock has a temperature coefficient of approximately $-0.2\%/^{\circ}\text{C}$ and a V_{DD} coefficient of approximately $\pm 1\%/V$.

**MSP50C32, MSP50C33, MSP50C34
MSP50P34, MSP50C37, MSP50P37
MIXED-SIGNAL PROCESSORS**

SPSS019A – MAY 1997 – REVISED OCTOBER 1998

MSP50x37 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{T+}	Positive-going threshold voltage (INIT)	V _{DD} = 4.5 V	2.7			V
		V _{DD} = 6 V	3.65			
V _{T−}	Negative-going threshold voltage (INIT)	V _{DD} = 4.5 V	2.3			V
		V _{DD} = 6 V	3.15			
V _{hys}	Hysteresis (V _{T+} − V _{T−}) (INIT)	V _{DD} = 4.5 V	0.4			V
		V _{DD} = 6 V	0.5			
I _{lkg}	Input leakage current (except for OSC IN)		1			μA
I _{standby}	Standby current (<u>INIT</u> low, SETOFF)		10			μA
I _{DD} [†]	Supply current	Power amplifier is on	25			mA
		Power amplifier is off	10			
I _{OH}	High-level output current (PA, PB, PD)	V _{DD} = 4 V, V _{OH} = 3.5 V	−4	−6	mA	
		V _{DD} = 5 V, V _{OH} = 4.5 V	−5	−7.5		
		V _{DD} = 6 V, V _{OH} = 5.5 V	−6	−9.2		
		V _{DD} = 4 V, V _{OH} = 2.65 V	−8	−13	mA	
		V _{DD} = 5 V, V _{OH} = 3.33 V	−14	−20		
		V _{DD} = 6 V, V _{OH} = 4 V	−20	−29		
I _{OL}	Low-level output current (PA4 – PA7)	V _{DD} = 4 V, V _{OL} = 0.5 V	20	28	mA	
		V _{DD} = 5 V, V _{OL} = 0.5 V	26	34		
		V _{DD} = 6 V, V _{OL} = 0.5 V	30	39		
		V _{DD} = 4 V, V _{OL} = 1.33 V	40	54	mA	
		V _{DD} = 5 V, V _{OL} = 1.67 V	60	74		
		V _{DD} = 6 V, V _{OL} = 2 V	82	103		
I _{OL}	Low-level output current (PA0 – PA3, PB, PD))	V _{DD} = 4 V, V _{OL} = 0.5 V	10	17	mA	
		V _{DD} = 5 V, V _{OL} = 0.5 V	13	20		
		V _{DD} = 6 V, V _{OL} = 0.5 V	15	25		
		V _{DD} = 4 V, V _{OL} = 1.33 V	20	32	mA	
		V _{DD} = 5 V, V _{OL} = 1.67 V	30	52		
		V _{DD} = 6 V, V _{OL} = 2 V	41	71		
Pullup resistance		Resistors selected by software and connected between terminal and V _{DD}	15	30	60	kΩ
f _{osc(low)}	Oscillator frequency [‡]	V _{DD} = 5 V, T _A = 25°C, Target frequency = 15.36 MHz	14.89	15.36	15.82	MHz
f _{osc(high)}	Oscillator frequency [‡]	V _{DD} = 5 V, T _A = 25°C, Target frequency = 19.2 MHz	18.62	19.2	19.77	MHz

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The frequency of the internal clock has a temperature coefficient of approximately $-0.2\%/^{\circ}\text{C}$ and a V_{DD} coefficient of approximately $\pm 1.4\%/V$.

MSP50x37 Power Amplifier Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential output power	$V_{DD} = 5\text{ V}$, $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		500		mW
Bandwidth				3.5	kHz

MSP50x37 ADC Electrical Characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	MIN	TYP	MAX	UNIT
Linearity		± 0.5		LSB
Offset		± 1.5		LSB
Full scale error		± 1.5		LSB
Conversion time		40		Instructions

switching characteristics (MSP50C32, MSP50C33, MSP50x34)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r Rise time, PA, PB, D/A	$V_{DD} = 3.3\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		50		ns
t_f Fall time, PA, PB, D/A	$V_{DD} = 3.3\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		50		ns

switching characteristics (MSP50x37)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r Rise time, PA, PB, PD	$V_{DD} = 4\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		22		ns
t_f Fall time, PA, PB, PD	$V_{DD} = 4\text{ V}$, $C_L = 100\text{ pF}$, 10% to 90%		10		ns

MSP50C32, MSP50C33, MSP50C34
MSP50P34, MSP50C37, MSP50P37
MIXED-SIGNAL PROCESSORS

SPSS019A – MAY 1997 – REVISED OCTOBER 1998

timing requirements

		MIN	MAX	UNIT
Initialization				
t _{INIT}	INIT pulsed low while the MSP50x3x has power applied (see Figure 1)	1		μs
Wakeup				
t _{su(wakeup)}	Setup time prior to wakeup terminal negative transition (see Figure 2)	1		μs
External Interrupt				
t _{su(interrupt)}	Setup time prior to B1 terminal negative transition (see Figure 3)	f _{clock} = 15.36 MHz	1	μs
		f _{clock} = 19.2 MHz	1.5	
Writing (Slave Mode)				
t _{su1(B1)}	Setup time, B1 low before B0 goes low (see Figure 4)	20		ns
t _{su(d)}	Setup time, data valid before B0 goes high (see Figure 4)	100		ns
t _{h1(B1)}	Hold time, B1 low after B0 goes high (see Figure 4)	20		ns
t _{h(d)}	Hold time, data valid after B0 goes high (see Figure 4)	30		ns
t _w	Pulse duration, B0 low (see Figure 4)	100		ns
t _r	Rise time, B0 (see Figure 4)		50	ns
t _f	Fall time, B0 (see Figure 4)		50	ns
Reading (Slave Mode)				
t _{su2(B1)}	Setup time, B1 before B0 goes low (see Figure 5)	20		ns
t _{h2(B1)}	Hold time, B1 after B0 goes high (see Figure 5)	20		ns
t _{dis}	Output disable time, data valid after B0 goes high (see Figure 5)	0	30	ns
t _w	Pulse duration, B0 low (see Figure 5)	100		ns
t _r	Rise time, B0 (see Figure 5)		50	ns
t _f	Fall time, B0 (see Figure 5)		50	ns
t _d	Delay time for B0 low to data valid (see Figure 5)		50	ns

PARAMETER MEASUREMENT INFORMATION

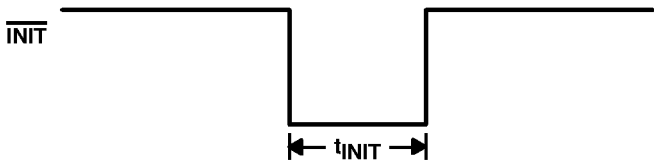


Figure 1. Initialization Timing Diagram

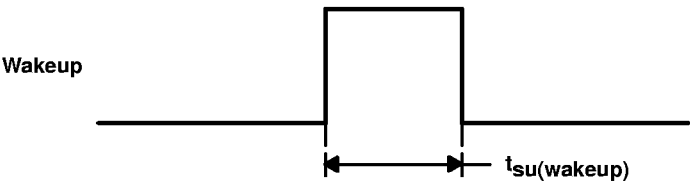


Figure 2. Wakeup Terminal Setup Timing Diagram

PARAMETER MEASUREMENT INFORMATION

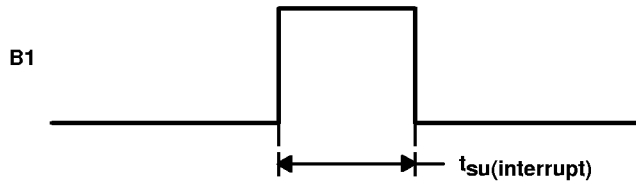


Figure 3. External Interrupt Terminal Setup Timing Diagram

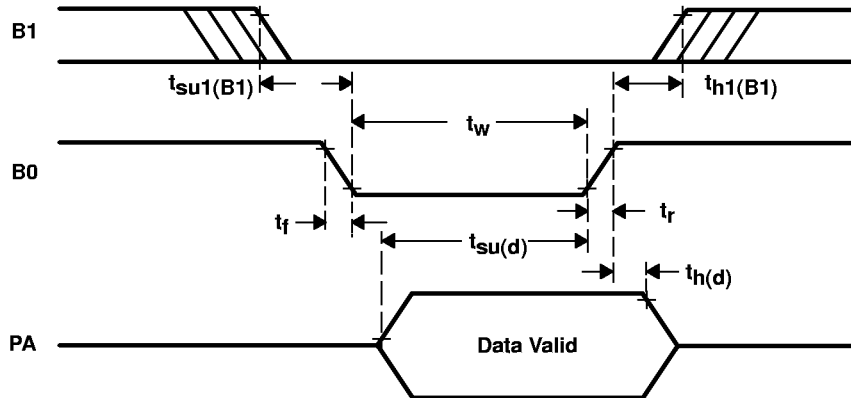


Figure 4. Write Timing Diagram (Slave Mode)

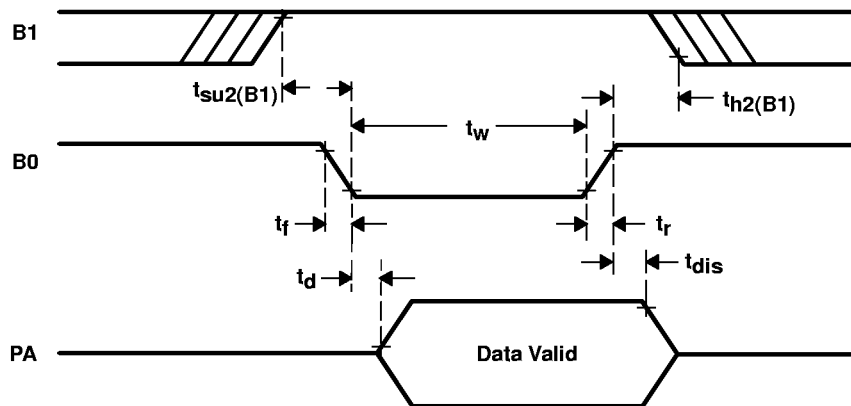


Figure 5. Read Timing Diagram (Slave Mode)

**MSP50C32, MSP50C33, MSP50C34
MSP50P34, MSP50C37, MSP50P37
MIXED-SIGNAL PROCESSORS**

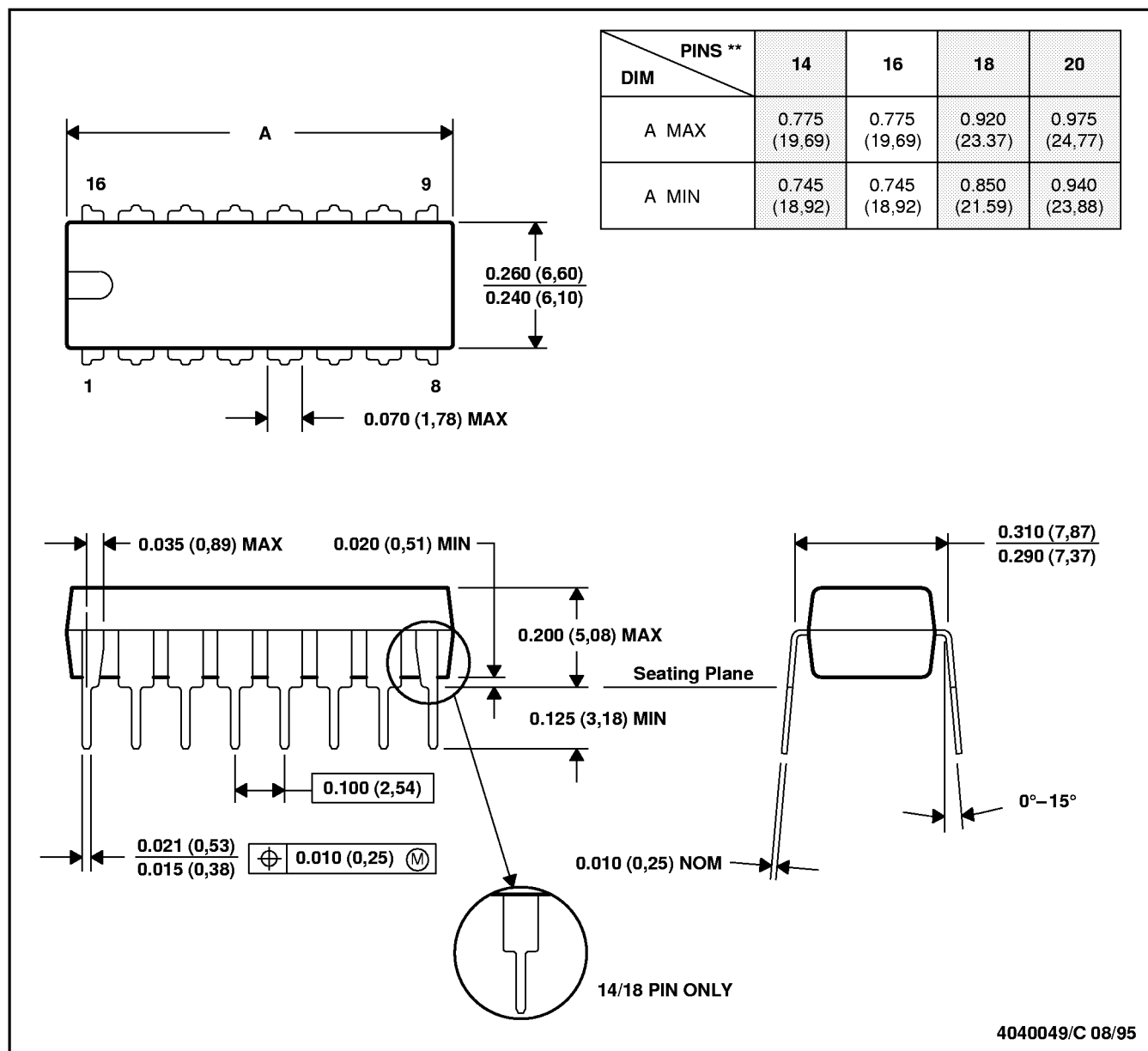
SPSS019A – MAY 1997 – REVISED OCTOBER 1998

MECHANICAL DATA

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

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