National Semiconductor

MILITARY DATA SHEET

MNDS7830-X REV 0A0

Original Creation Date: 01/18/96
Last Update Date: 12/20/96
Last Major Revision Date: 01/18/96

DUAL DIFFERENTIAL LINE DRIVER

General Description

The DS7830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50 Ohms to 500 Ohms. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Industry Part Number

DS7830

NS Part Numbers

DS7830J/883
DS7830W/883

Prime Die

DM7830

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

(Absolute Maximum Ratings)
(Note 1)

Vcc	7.0V
Input Voltage	5.5V
Storage Temperature	-65 C to +150 C
Lead Temperature	
Soldering, 4 seconds	260 C
Output Short Circuit Duration	
(125 C)	1 Second
Maximum Power Dissipation @ 25 C (Note 2)	
CerDip (J Pkg)	1442mW
CerPak (W Pkg)	943mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Derate CerDip (J) Pkg 9.6 mW/C above 25C. Derate CerPak (W) Pkg 6.3 mW/C above 25C.

Recommended Operating Conditions

Supply Voltage (Vcc)	
Min.	4.5V
Typ.	5.0V
Max.	5.5V
Temperature (TA) (Note 1)	
Min.	-55C
Typ.	+25C
Max.	+125C

Note 1: Power dissipation must be externally controlled at elevated temperatures.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh1	Logical "1" Output Voltage	Vcc= 4.5V, Iout=-0.8mA, Vin=2V/0.8V	2		2.4		V	1, 2, 3
Voh2	Logical "1" Output Voltage	Vcc= 4.5V, Iout=-40mA, Vin=2V/0.8V	2		1.8		V	1, 2, 3
Vol1	Logical "0" Output Voltage	Vcc= 4.5V, Iol= 32mA, Vin=0.8V/2V	2			0.4	V	1, 2, 3
Vol2	Logical "0" Output Voltage	Vcc= 4.5V, Iol= 40mA, Vin=0.8V/2V	2			0.5	V	1, 2, 3
Iih1	Logical "1" Input Current	Vcc=5.5V, Vih=2.4V	2			120	uA	1, 2, 3
Iih2	Logical "1" Input Current	Vcc=5.5V, Vih=5.5V	2			2	mA	1, 2, 3
Iil	Logical "0" Input Current	Vcc=5.5V, Vil= 0.4V	2			-4.8	mA	1, 2, 3
Ios(min)	Short Circuit Output Current	Vcc= 5V, Vout= 0V	2		-40		mA	1, 2
Ios(max)	Short Circuit Output Current	Vcc= 5V, Vout=0V	2			-120	mA	1, 2
Vic	Input Clamp Voltage	Vcc= 4.5V, Iin= -12mA	2			-1.5	V	1, 2, 3
Icc	Power Supply Current	Vcc= 5V, Vin= 5V (both drivers combined)	2			36	mA	1, 2, 3
Vih	LOgical "1" Input Voltage	Vcc= 4.5V	1, 2		2		V	1, 2, 3
Vil	Logical "0" Input Voltage	Vcc= 4.5V	1, 2			0.8	V	1, 2, 3

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V, RL=400 ohms, Cl=50pF or equivalent impedance provided by diode load. Tr = Tf = 10nS.

tPLH	Progationd Delay Time: AND/NAND				3	12	nS	9
tPHL	Propagation Delay Time: AND				3	18	nS	9
tPHL	Propagation Delay Time: NAND				1	8	nS	9
tPHL/tPLH	Differential Delay	Rl=100 Ohms	3			16	nS	9

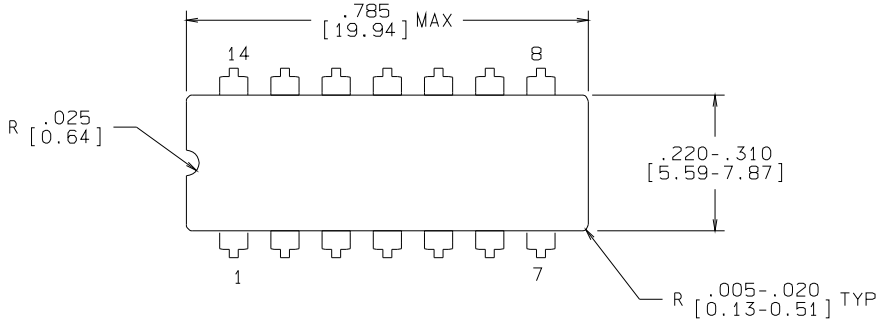
Note 1: Parameter tested go-no-go only.
Note 2: Subgroup 1 and 2: Power dissipation must be externally controlled at elevated temperatures.
Note 3: Guaranteed parameter not tested.

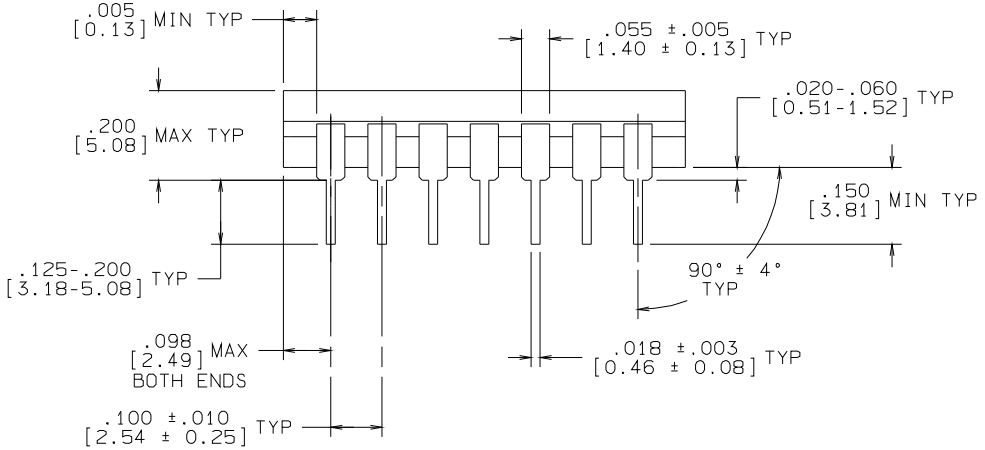
Graphics and Diagrams

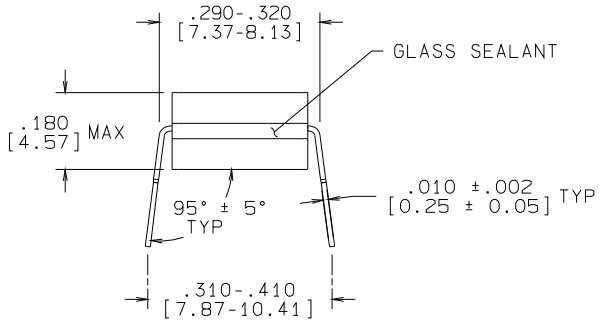
GRAPHICS#	DESCRIPTION
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W14BRN	CERPAC (W), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH [MM]

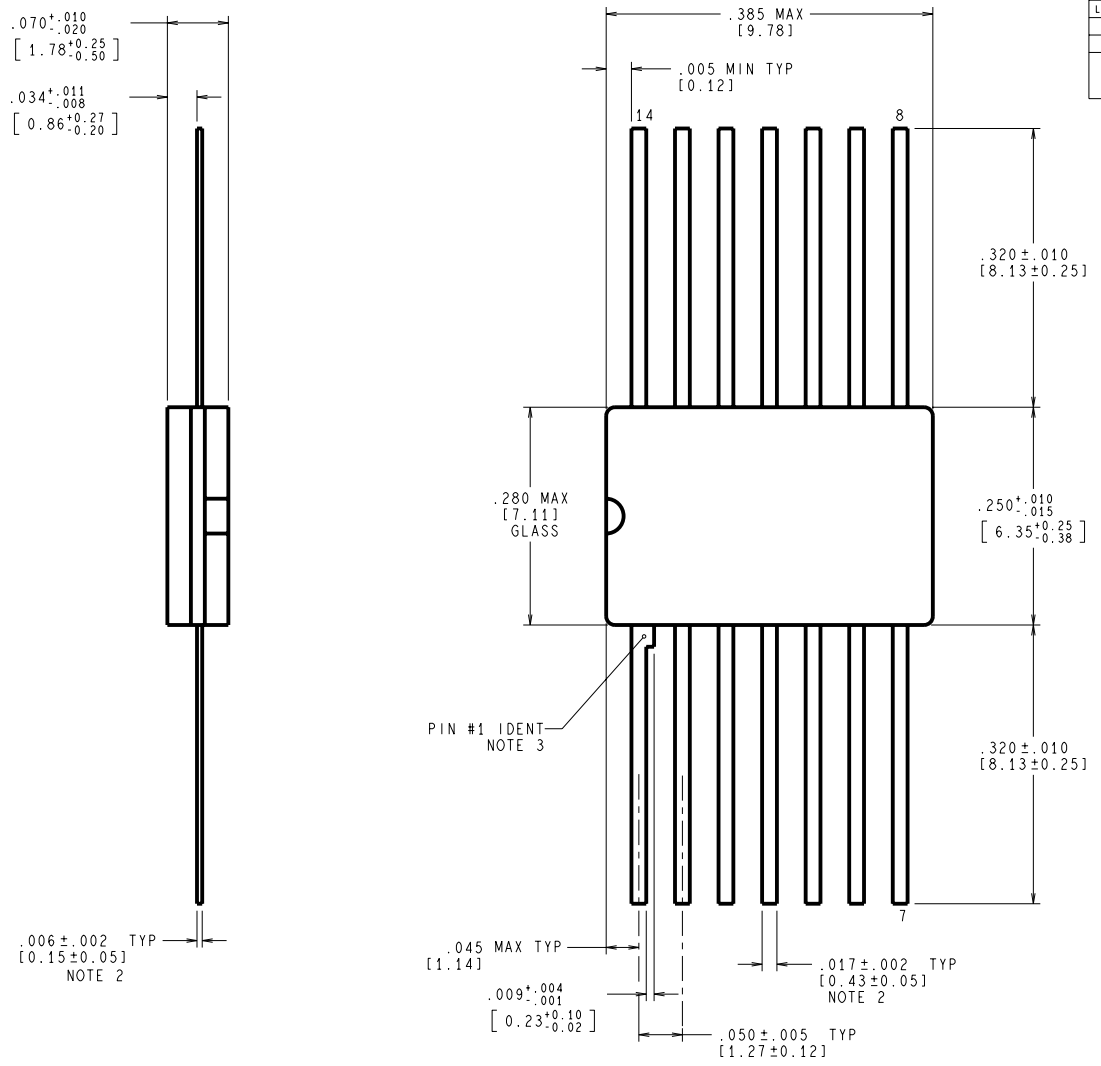
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1